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(57) Abstract :

Reversible computing became very important and a computing paradigm having its applications in low-power CMOS technologies and Quantum computing. These days, the majority of practical applications, such as train station displays, digital cameras, digital counters, and many more applications, use a seven-segment display decoder as one of the components. In the current technological era, digital circuits must have low power consumption. One notable technological advancement that is crucial to quantum computing is reversible logic gate technology. The quantum computers function at high speed and lower power consumption. In this work, a novel architecture of reversible logic implementation of BCD to 7-segment display decoder is proposed. This design intends to optimize the decoder in terms of the number of reversible gates, delay, garbage outputs, power and thus the complexity of the circuit reduces. Hence, this optimized design will significantly strengthen the performance of the 7-segment displays concerning speed and power utilization. The simulation and synthesis are carried out with the Xilinx Vivado Software and it was implemented on the NEXYS 4 DDR, a platform featuring the latest Artix FPGA.

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