Lab Code:18ECL33
PSPICE
Lab Manual

Department of Electronics & Communication Engineering

Bapatla Engineering College :: Bapatla

(Autonomous)

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Bapatla Engineering College :: Bapatla
(Autonomous)

Vision

- To build centers of excellence, impart high quality education and instill high standards of ethics and professionalism through strategic efforts of our dedicated staff, which allows the college to effectively adapt to the ever changing aspects of education.

- To empower the faculty and students with the knowledge, skills and innovative thinking to facilitate discovery in numerous existing and yet to be discovered fields of engineering, technology and interdisciplinary endeavors.

Mission

- Our Mission is to impart the quality education at par with global standards to the students from all over India and in particular those from the local and rural areas.

- We continuously try to maintain high standards so as to make them technologically competent and ethically strong individuals who shall be able to improve the quality of life and economy of our country.

Bapatla Engineering College :: Bapatla

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Department of Electronics and Communication Engineering

Vision

To produce globally competitive and socially responsible Electronics and Communication Engineering graduates to cater the ever changing needs of the society.

Mission

- To provide quality education in the domain of Electronics and Communication Engineering with advanced pedagogical methods.

- To provide self learning capabilities to enhance employability and entrepreneurial skills and to inculcate human values and ethics to make learners sensitive towards societal issues.

- To excel in the research and development activities related to Electronics and Communication Engineering.

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Department of Electronics and Communication Engineering

Program Educational Objectives (PEO's)

PEO-I: Equip Graduates with a robust foundation in mathematics, science and Engineering Principles, enabling them to excel in research and higher education in Electronics and Communication Engineering and related fields.

PEO-II: Impart analytic and thinking skills in students to develop initiatives and innovative ideas for Start-ups, Industry and societal requirements.

PEO-III: Instill interpersonal skills, teamwork ability, communication skills, leadership, and a sense of social, ethical, and legal duties in order to promote lifelong learning and Professional growth of the students.

Program Outcomes (PO's)

Engineering Graduates will be able to:

PO1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7.Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. Individual and Teamwork: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. Life-long learning: Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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Department of Electronics and Communication Engineering

Program Specific Outcomes (PSO's)

PSO1: Develop and implement modern Electronic Technologies using analytical methods to meet current as well as future industrial and societal needs.

PSO2: Analyze and develop VLSI, IoT and Embedded Systems for desired specifications to solve real world complex problems.

PSO3: Apply machine learning and deep learning techniques in communication and signal processing.

PSPICE Lab
II B.Tech – I Semester (Code: 18ECL33)

Lectures	0	Tutorial	0	Practical	3	Credits	1
Continuous Internal Assessment			50	Semester End Examination (3 Hours)			50

Prerequisites: None

Course Objectives: Students will

- Understand the netlist from the given circuit, simulate and observe the DC operating point and DC analysis.
- Analyze the frequency response of various amplifier circuits with ac analysis.
- Obtain the transient response of nonlinear wave shaping circuits.
- Verify the truth tables of different logic gates

Course Outcomes: After studying this course, the students will be able to

CO1	Understand the netlist from the given circuit, simulate and observe the DC operating point and DC analysis.
CO2	Analyze the frequency response of various amplifier circuits with ac analysis
CO3	Design of various rectifier circuits with and without filters
CO4	Verify the truth tables of different logic gates

Mapping of Course Outcomes with Program Outcomes & Program Specific Outcomes

	PO's												PSO's		
CO	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
CO1	3	2		2	2								1	1	3
CO2	2	3		2	2								2	2	2
CO3	3	2			2								2	2	3
CO4	3	1			2								2	2	3
AVG	3	2		2	2								1	1	3

LIST OF LAB EXPERIMENTS

1. PSPICE Simulation Of Nodal Analysis For DC Circuits
2. PSPICE Simulation for finding DC voltages and currents
3. PSPICE Simulation for finding resonant frequency of series RLC circuit
4. Verification of Low pass and High pass Filters using PSPICE.
5. Verification of Half–Wave and Full-Wave Rectifier
6. Frequency Response of CE Amplifier
7. Frequency Response of CC Amplifier

8. Verification of Clippers
9. Verification of Clampers
10. Design and Verification of Logic Gates
11. Design and Verification of Class-A Power Amplifier
12. Design and Verification of Voltage Regulator
13. Design and Verification of Differential amplifier
14. Design and Verification of Attenuators
15. Design and Verification of RC coupled amplifier.

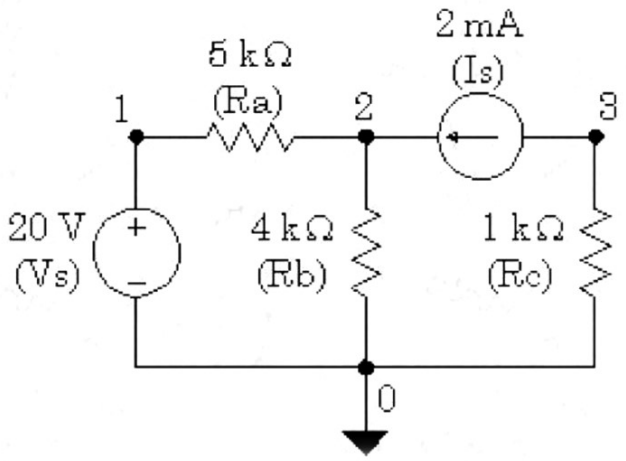
NOTE: A minimum of 10 (Ten) experiments have to be Performed and recorded by the candidate to attain eligibility for Semester End Examination.

1.PSPICE SIMULATION OF Nodal analysis for DC circuits

AIM: To Simulate the DC Circuit for determining the all node voltages using PSPICE.

SOFTWARE REQUIRED: OrCAD PSPICE 9.1

Circuit diagram:



Program:

```
Vs   1   0   DC   20.0V ; note the node placements
Ra   1   2   5.0k
Rb   2   0   4.0k
Rc   3   0   1.0k
Is   3   2   DC   2.0mA ; note the node placements
.END
```

Output :

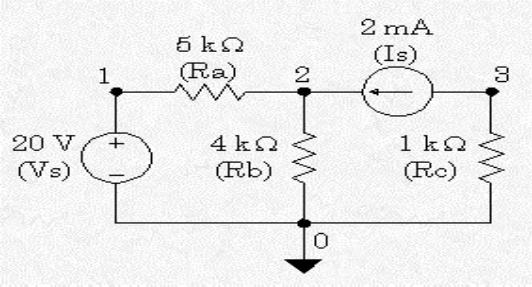
```
NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE
( 1) 20.0000 ( 2) 13.3330 ( 3) -2.0000 <==

Results
VOLTAGE SOURCE CURRENTS
NAME CURRENT
Vs -1.333E-03 <== Current entering node 1 of Vs

TOTAL POWER DISSIPATION 2.67E-02 WATTS
JOB CONCLUDED
TOTAL JOB TIME .26
```

2. PSPICE Simulation for finding DC voltages and currents.

AIM: To Simulate the DC Circuit for printing the required voltages and currents using PSPICE.

SOFTWARE REQUIRED: OrCAD PSPICE 9.1

Circuit diagram:



Program:

```
Vs   1   0   DC   20.0V
Ra   1   2   5.0k
Rb   2   0   4.0k
Rc   3   0   1.0k
Is   3   2   DC   2.0mA
.DC  Vs  20 20 1          ; this enables the .print commands
.PRINT  DC  V(1,2)  I(Ra)
.PRINT  DC  V(2)  I(Rb)
.PRINT  DC  V(3)  I(Rc)
.END
```

Output :

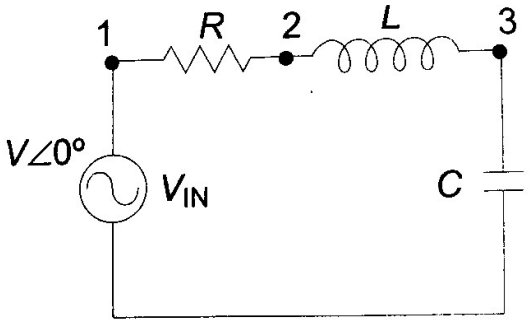
```
Vs              V(1,2)            I(Ra)

2.000E+01    6.667E+00     1.333E-03  <== data for Ra

Vs              V(2)                I(Rb)

2.000E+01      1.333E+01       3.333E-03  <== data for Rb

Vs              V(3)                I(Rc)

2.000E+01      -2.000E+00     -2.000E-03  <== data for Rc

JOB CONCLUDED

TOTAL JOB TIME .13
```

3. PSPICE Simulation for finding resonant frequency of series RLC circuit.

AIM: To find the resonant frequency of series RLC circuit using PSPICE software
Assume R=25ohms, L=10mH, C=100uF,V=100V

SOFTWARE REQUIRED: PSPICE – OrCAD PSPICE 9.1

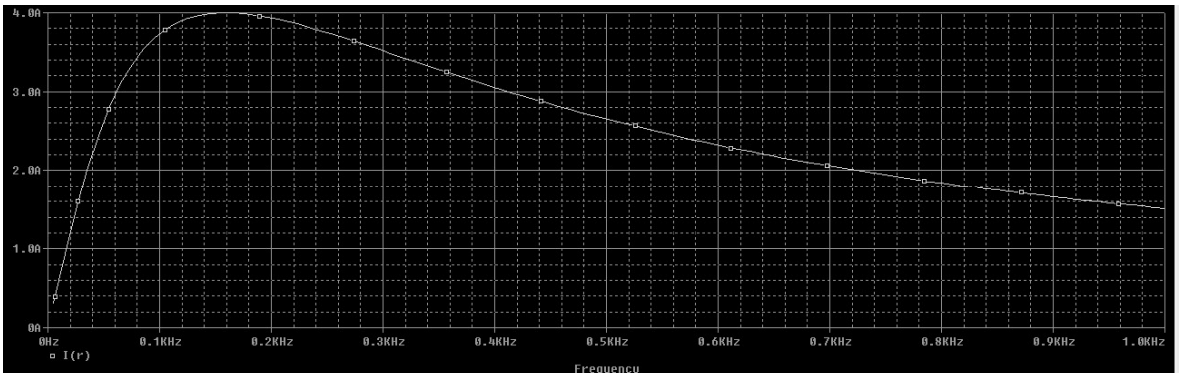
CIRCUIT DIAGRAM:



Program:

```
VIN  1  0  AC 100
R 1  2  25
L 2  3  10m
C 3 0 100u
.AC LIN  100 5 1000
.PROBE
.PRINT AC I(R)
.END
```

OUTPUT

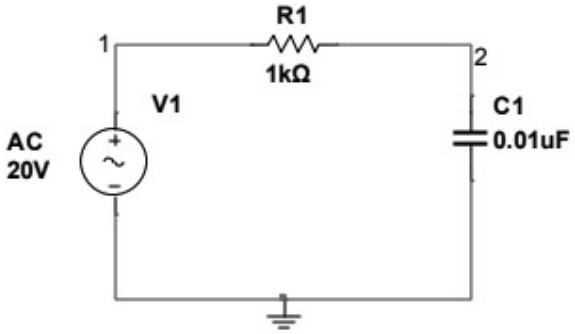


4. Verification of Low pass and High pass Filter

AIM: To verify the characteristics of Low pass and High pass filter

SOFTWARE REQUIRED: OrCAD PSPICE 9.1

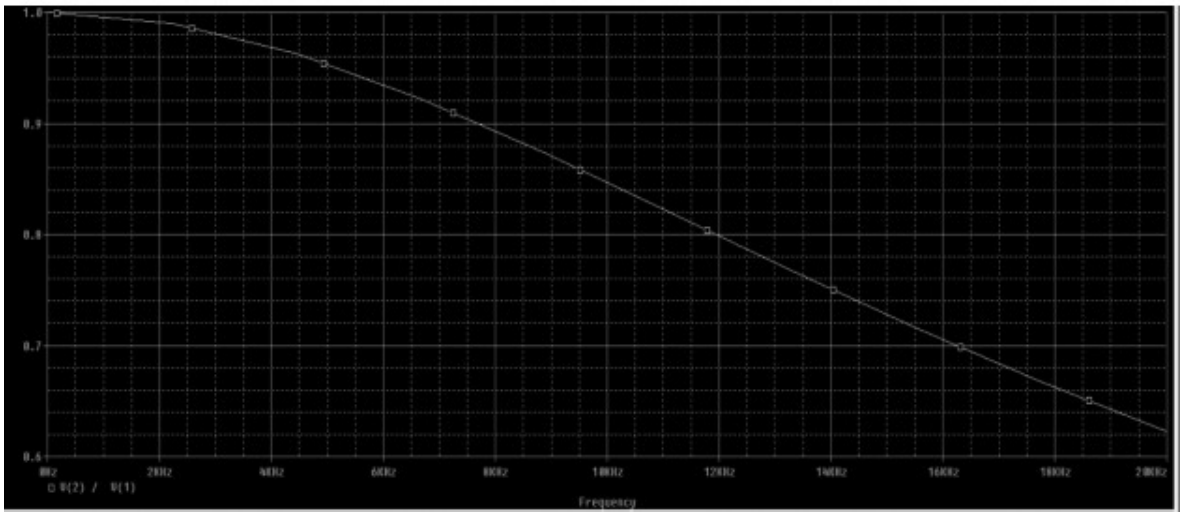
CIRCUIT DIAGRAM:
Low Pass Filter:



Program:

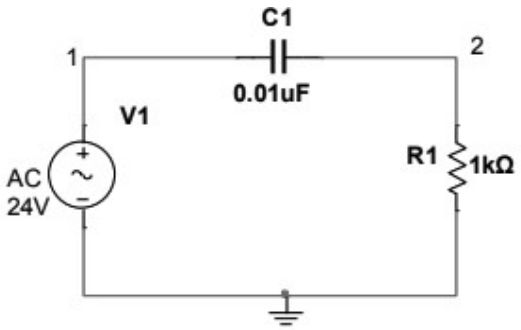
```
*LOW PASS FILTER
V1 1 0 AC 20v
 R1 1 2 1k
 C1 2 0 0.01uf
.AC LIN 10 10 20k
 .PROBE
.END
```

Output:



High Pass Filter

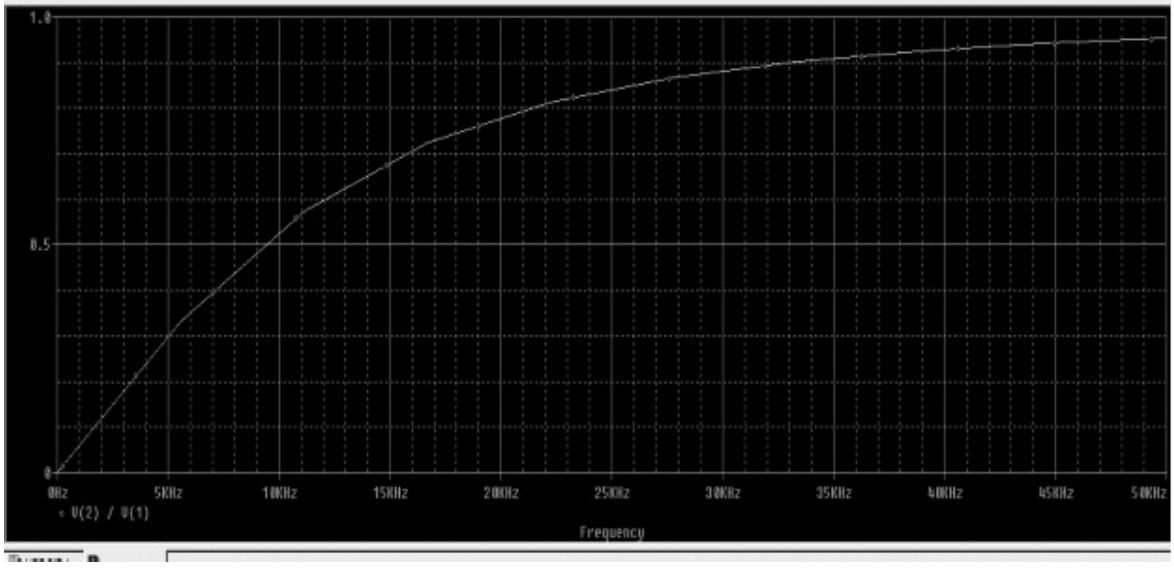
Circuit Diagram:



PROGRAM:

```
 *HIGH PASS FILTER
V1 1 0 AC 24V
 C1 1 2 0.01UF
R1 2 0 1K
.AC LIN 10 10 50K
.PROBE
.END
```

Output:



Result:

Hence the design of Low pass filter and High pass filter is simulated using OrCAD PSPICE 9.1

5. To design Rectifiers with and without filter using pspice

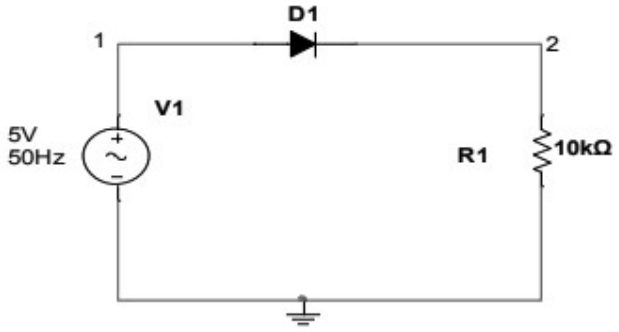
AIM: To design Rectifiers with and without filter using pspice

Software Required: OrCADPspice 9.1

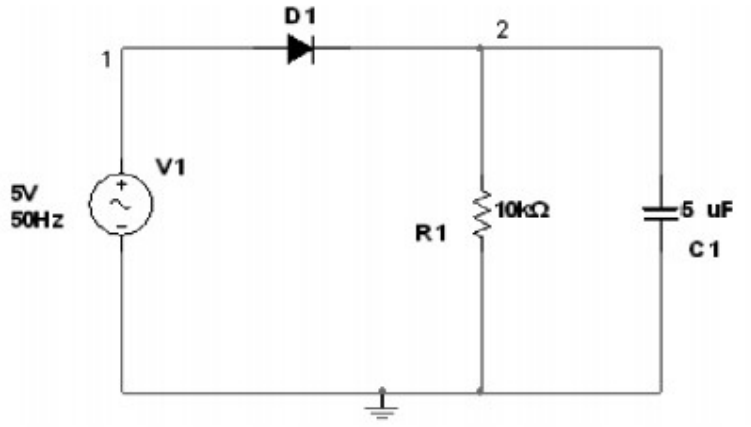
Half Wave Rectifier:

Circuit Diagram:

Without filter:



With filter:



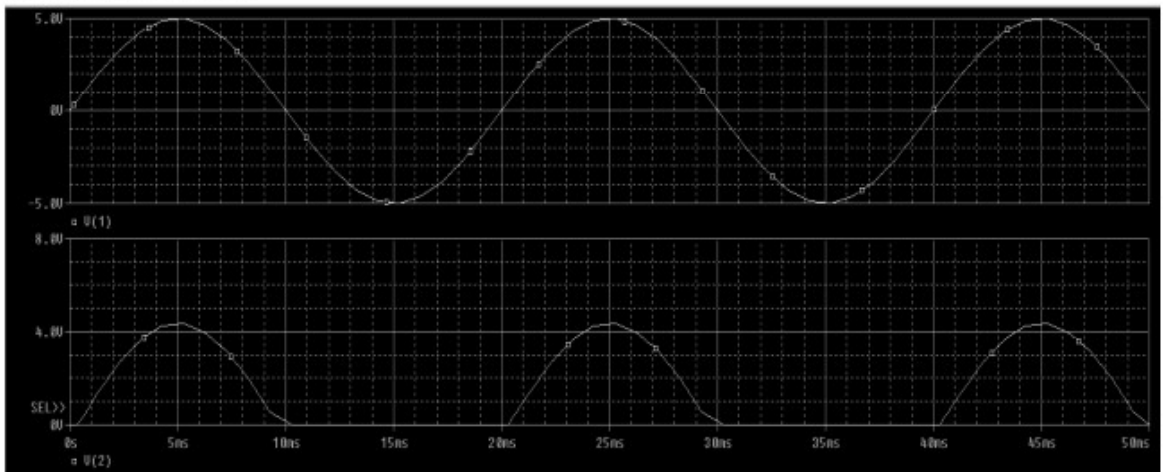
PSPICE Program:

```
*HALF WAVE RECTIFIER WITHOUT FILTER
Vin 1 0 sin(0 5 50)
D1 1 2 mod1
R1 2 0 10k
.MODEL mod1 D
.TRAN 0 50ms
.PROBE
.END
```

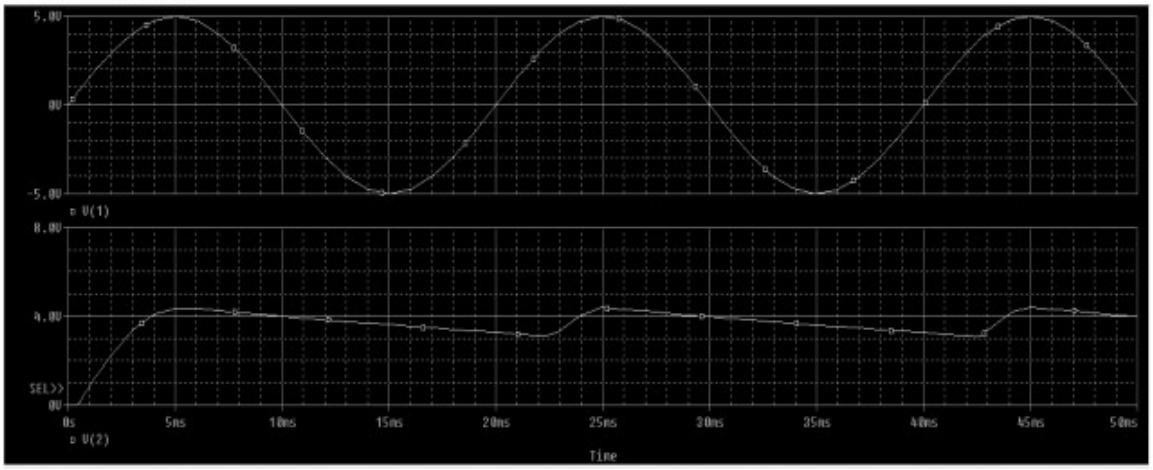
```
*HALF WAVE RECTIFIER WITH FILTER
Vin 1 0 sin(0 5 50)
D1 1 2 mod1
R1 2 0 10k
C1 2 0 5uf
.MODEL mod1 D
.TRAN 0 50ms
.PROBE
.END
```

Output:

WITHOUT FILTER:



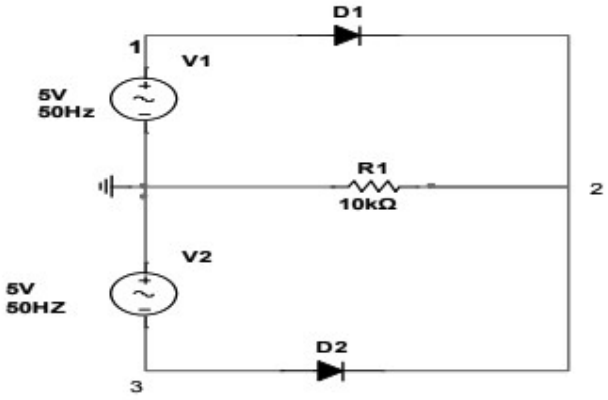
WITH FILTER:



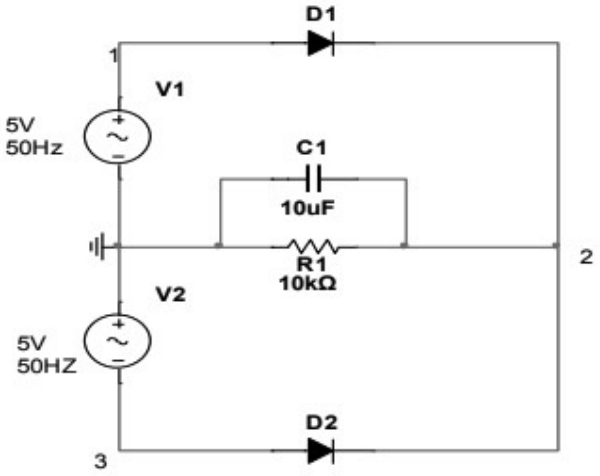
Full Wave Rectifier

Circuit Diagram:

Without filter:



With filter:



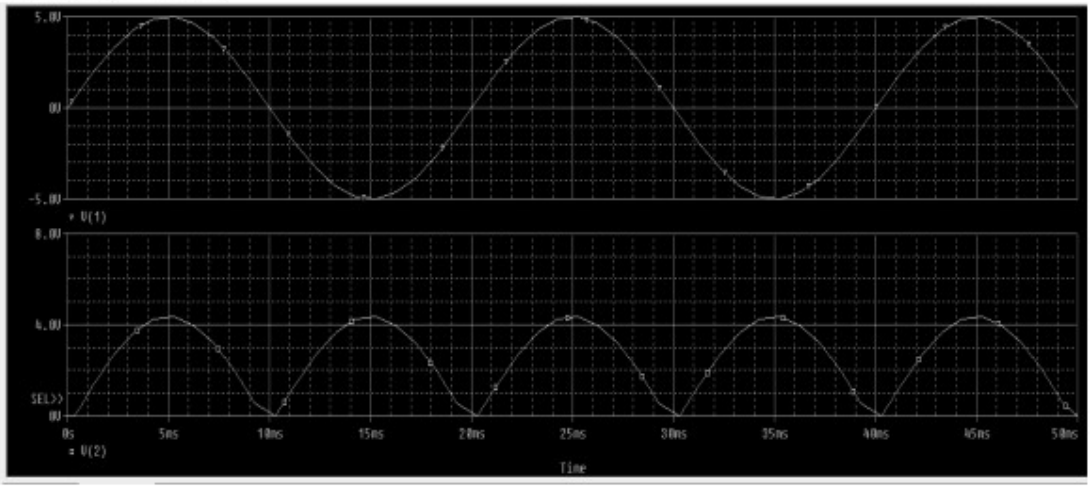
PSPICE Program:

```
*FULL WAVE RECTIFIER WITHOUT FILTER
V1 1 0 sin(0 5 50)
D1 1 2 mod1
V2 0 3 sin(0 5 50)
D2 3 2 mod1
R1 0 2 10k
.MODEL mod1 D
.TRAN 0 50ms
.PROBE
.END
```

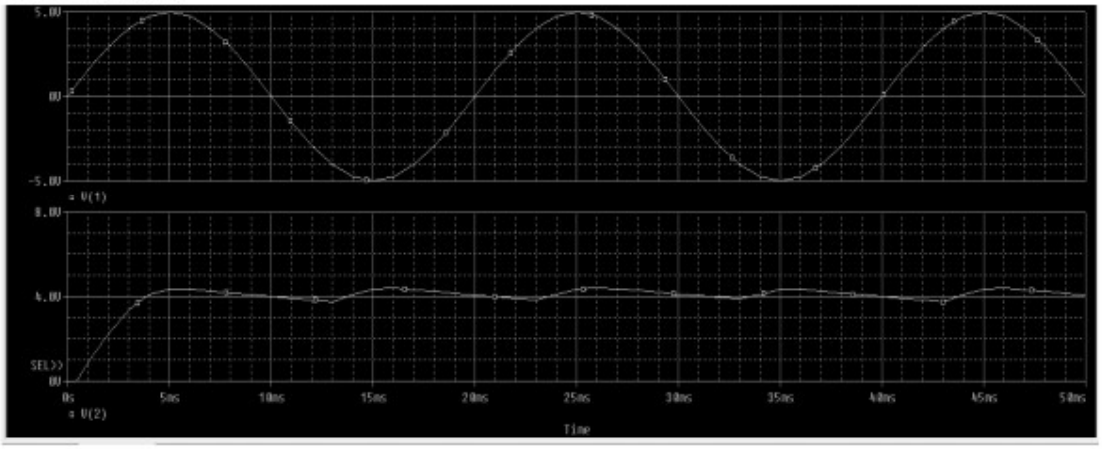
```
*FULL WAVE RECTIFIER WITH FILTER
V1 1 0 sin(0 5 50)
V2 0 3 sin(0 5 50)
D1 1 2 mod1
D2 3 2 mod1
R1 0 2 10k
C1 0 2 5uf
.MODEL mod1 D
.TRAN 0 50ms
.PROBE
.END
```

Output:

WITHOUT FILTER:



WITH FILTER:



Result: Hence the design of Rectifiers is simulated using OrCADPspice 9.1

6.CE Amplifier

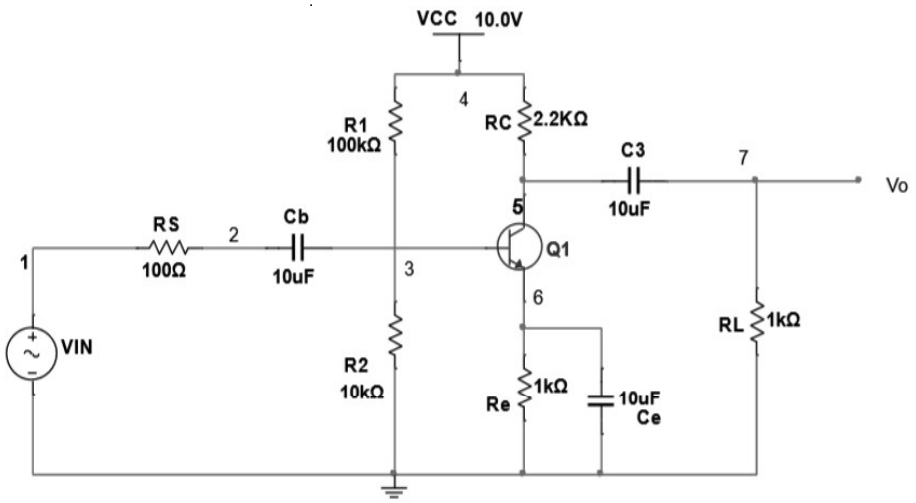
AIM: To verify the characteristics of CE Amplifier

Software Required: OrcadPspice 9.1

Theory:

The COMMON-EMITTER CONFIGURATION (CE) is the most frequently used configuration in practical amplifier circuits, since it provides good voltage, current, and power gain. The input circuit, making the emitter the element "common" to both input and output. The CE is set apart from the other configurations, because it is the only configuration that provides a phase reversal between input and output signals.

Circuit Diagram:



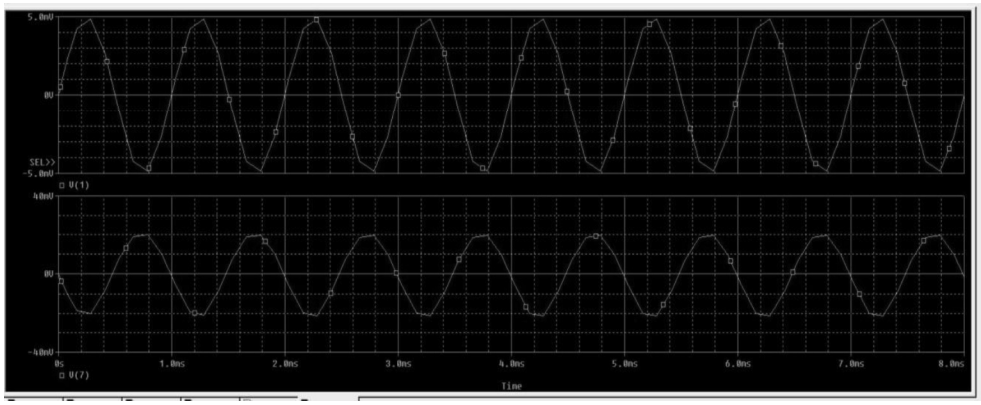
PSPICE Program:

*COMMON EMITTER AMPLIFIER
Vin 1 0 AC 5mV SIN (0 5m 1K) Rs
1 2 100
R1 3 4100K
R2 3 010K
RC 4 5 2.2K
RE601K
RL701K

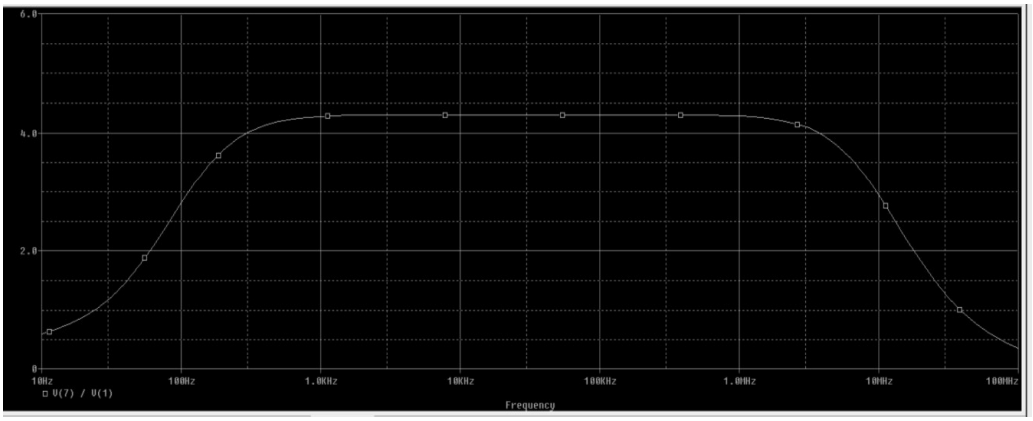
Cb2 3 10U
Ce6 0 10U
Cc5 7 10U
cc 4 0 10v
Q1 5 3 6 MOD1
. MODEL MOD1 NPN(Cjc=80PF,Cje=3PF)
.AC DEC 10 10 100MEG
. TRAN 0 8m
. PROBE
. END

Output:

COMMON EMITTER AMPLIFIER TRANSIENT ANALYSIS



COMMON EMITTER AMPLIFIER AC ANALYSIS



Result:

Hence the design of CE Amplifier is simulated using OrCAD PSPICE 9.1 and their characteristics were observed.

7.CC Amplifier

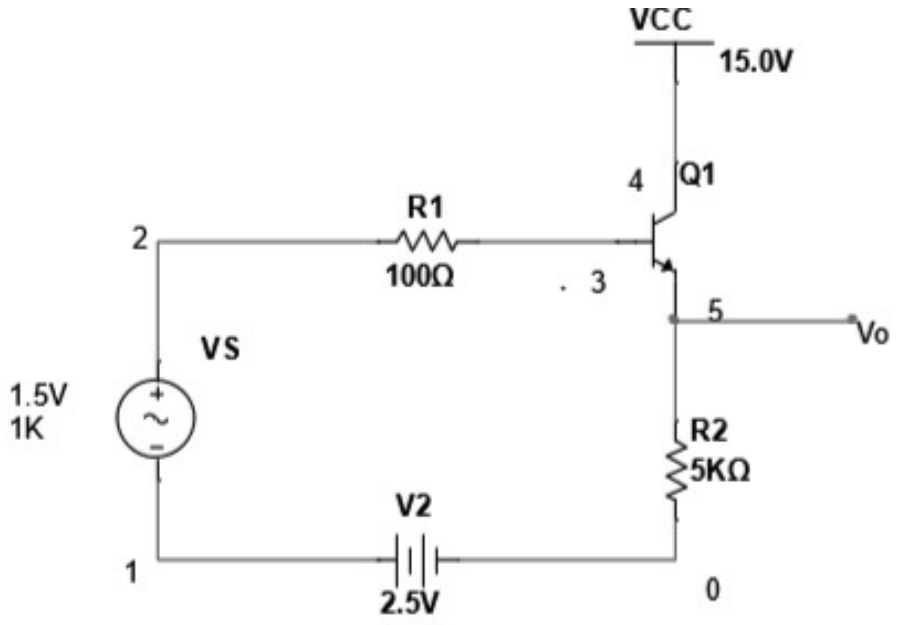
AIM: To verify the characteristics of CCAmplifier

Software Required: OrCAD Pspice 9.1

Theory:

Common collector amplifier has collector common to both input and output.
It is called the *common-collector* configuration because (ignoring the power supply battery) both the signal source and the load share the collector lead as a common connection point.
Common collector: Input is applied to base and collector. Output is from emitter-collector circuit. It should be apparent that the load resistor in the common-collector amplifier circuit receives both the base and collector currents, being placed in series with the emitter. Since the emitter lead of a transistor is the one handling the most current (the sum of base and collector currents, since base and collector currents always mesh together to form the emitter current), it would be reasonable to presume that this amplifier will have a very large current gain. This presumption is indeed correct: the current gain for a common-collector amplifier is quite large, larger than any other transistor amplifier configuration. However, this is not necessarily what sets it apart from another amplifier design.

Circuit Diagram:

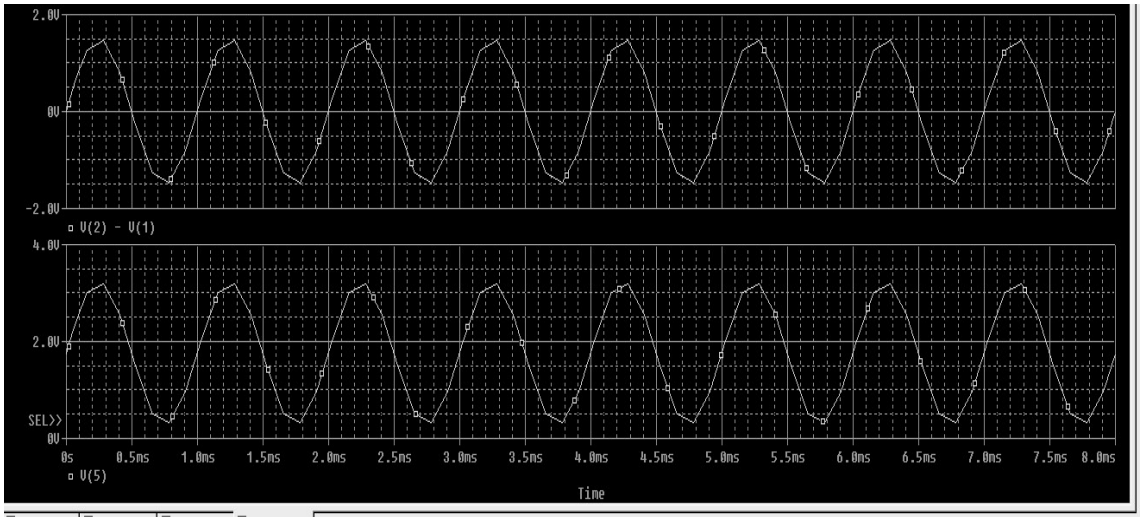


Pspice Program:

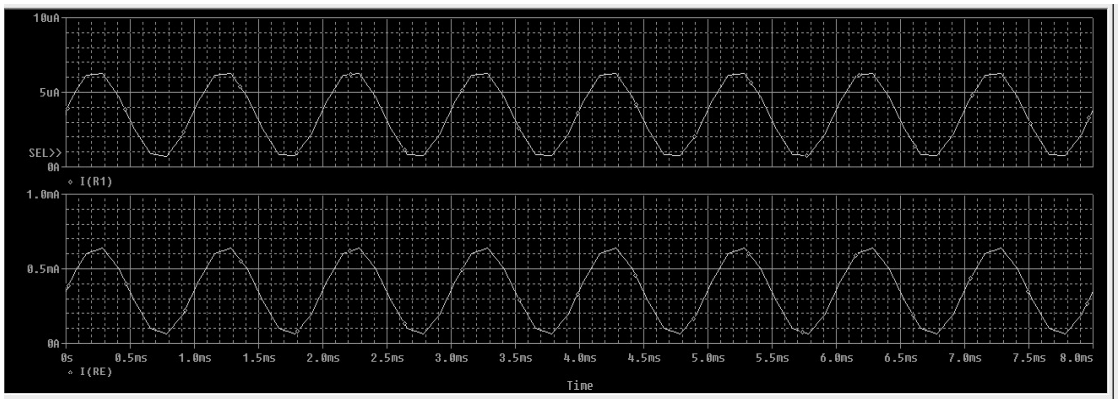
```
*COMMON COLLECTOR AMPLIFIER
Vin 2 1 AC 5MV SIN (0 1.5V 1K)
V1 1 0 2.5V
R1 2 3 100
RE 5 0 5K
Q1 4 3 5 MOD1
VCC 4 0 15V
. MODEL MOD1 NPN (CJC=80PF, CJE=3PF)
. TRAN 0 8mS
.AC DEC 10 10 100MEG
. PROBE
. END
```

Output:

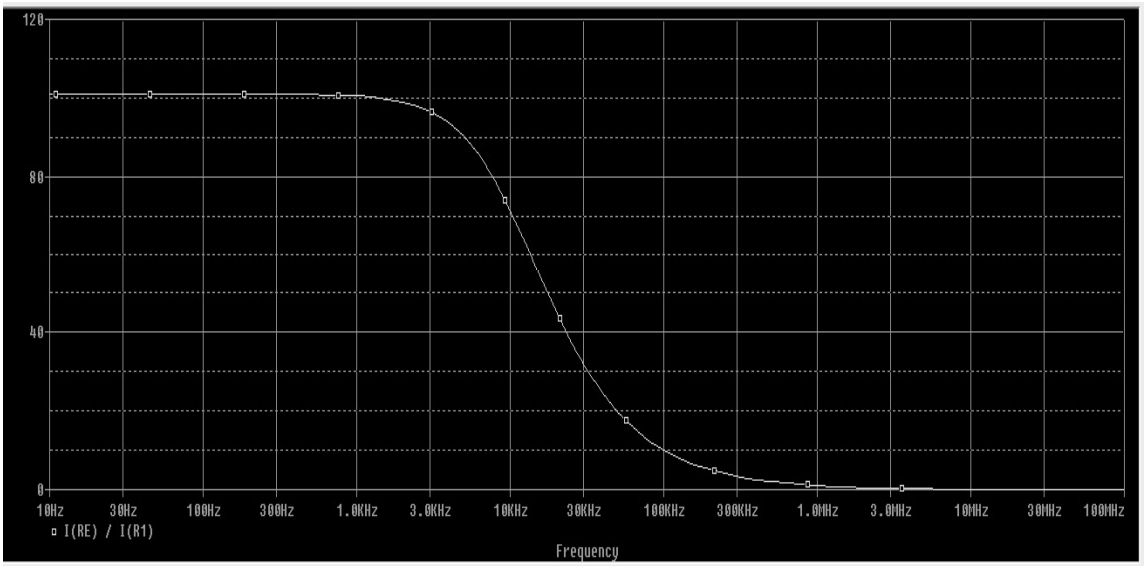
COMMON COLLECTOR AMPLIFIER TRANSIENT ANALYSIS(VOLTAGE)



COMMON COLLECTOR AMPLIFIER TRANSIENT ANALYSIS(CURRENT)



COMMON COLLECTOR AMPLIFIER AC ANALYSIS



Result:

Hence the design of CC Amplifier is simulated using OrCADPspice 9.1 and their characteristics were observed.

8.CLIPPERS

AIM: To verify the characteristics of CLIPPERS

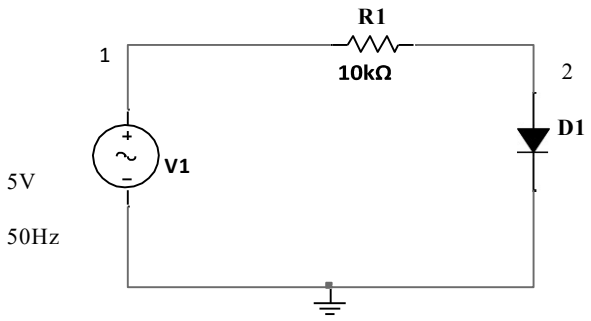
Software Required: OrcadPspice 9.1

Theory:

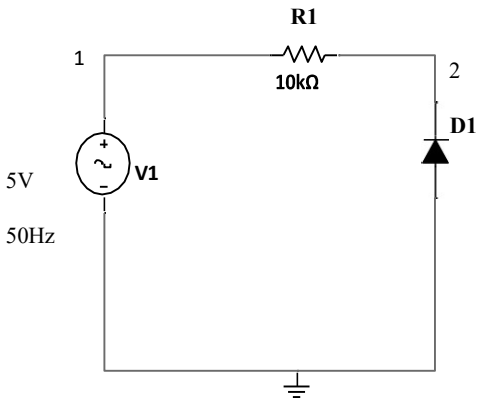
A circuit which removes the peak of a waveform is known as a *clipper*. A negative clipper is shown in Figure above.
During the positive half cycle of the 5 V peak input, the diode is reversed biased. The diode does not conduct. It is as if the diode were not there. The positive half cycle is unchanged at the output V (2) in Figure below. Since the output positive peaks actually overlays the input sinewave V (1), the input has been shifted upward in the plot for clarity.

Circuit Diagram:

Unbiased Positive Clipper:



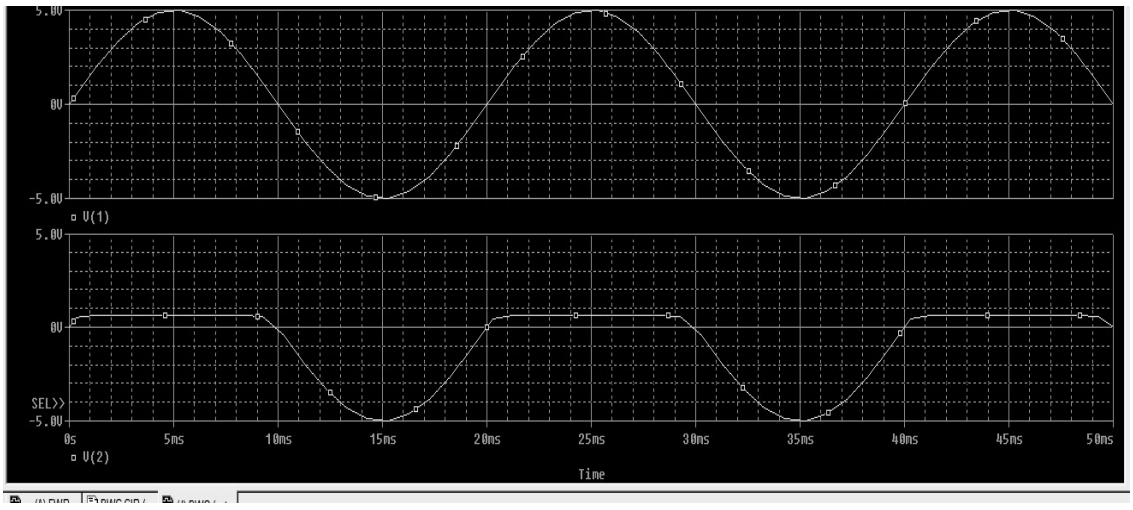
Unbiased Negative Clipper:



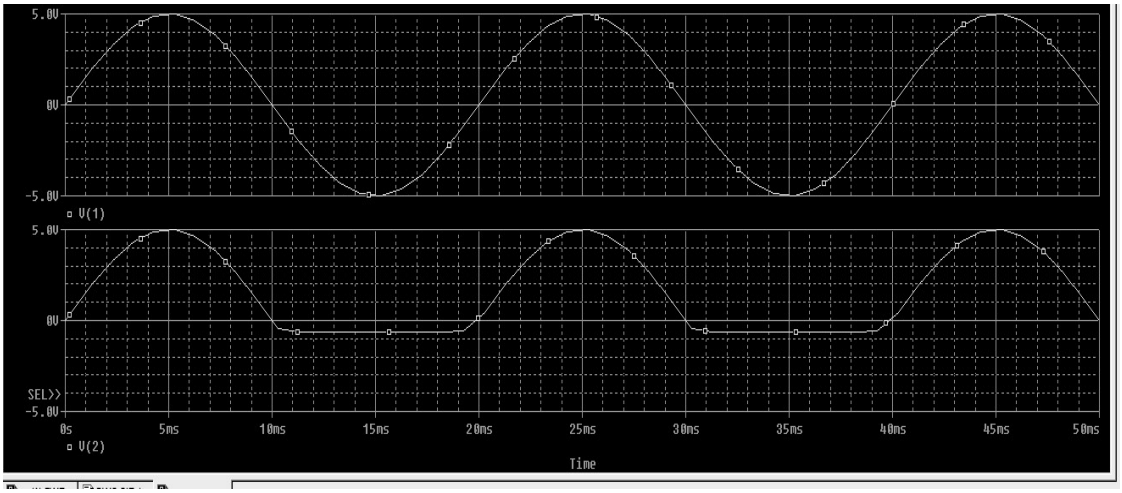
```
*POSITIVE PEAK CLIPPER
V1 1 0 sin(0 5 50)
R 1 2 10k
D 2 0 mod1
.MODEL mod1 D
.TRAN 0 50ms
.PROBE V[1] V[2]
.END

*NEGATIVE PEAK CLIPPER
V1 1 0 sin(0 5 50)
R1 1 2 10k
D1 0 2 mod1
.MODEL mod1 D
.TRAN 0 50ms
.PROBE V[1] V[2]
.END
```

Output:

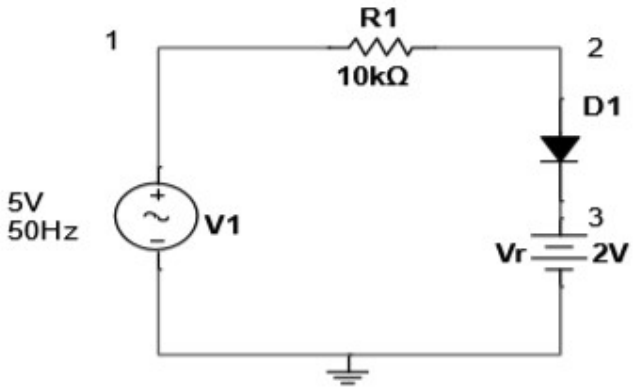
Unbiased Positive Clipper



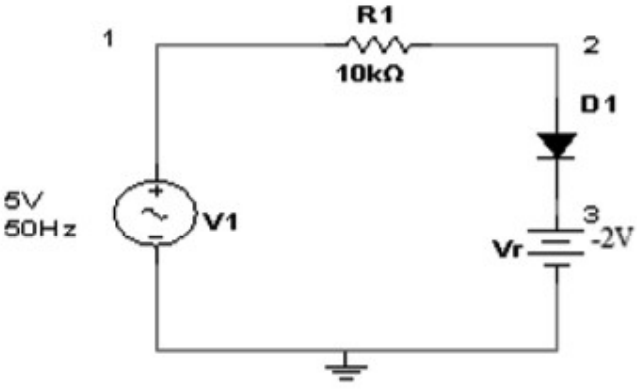
Unbiased Negative Clipper



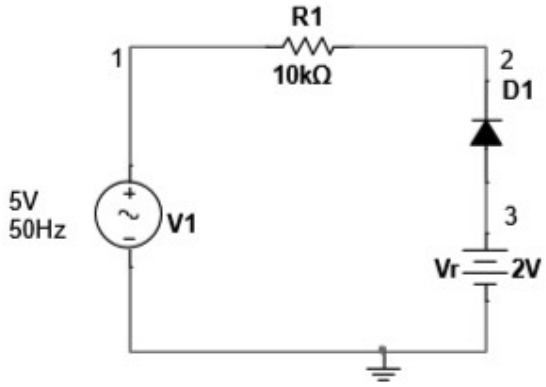
Biased Positive Peak Clipper with positive reference:



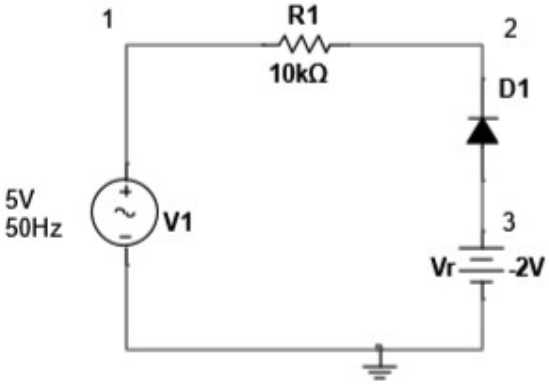
Biased Positive Peak Clipper with negative reference



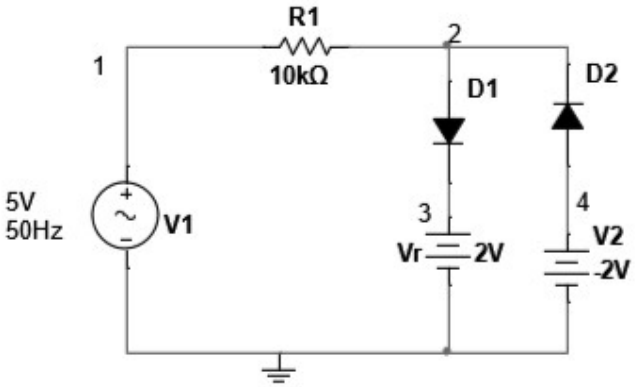
Biased negative Peak Clipper with positive reference



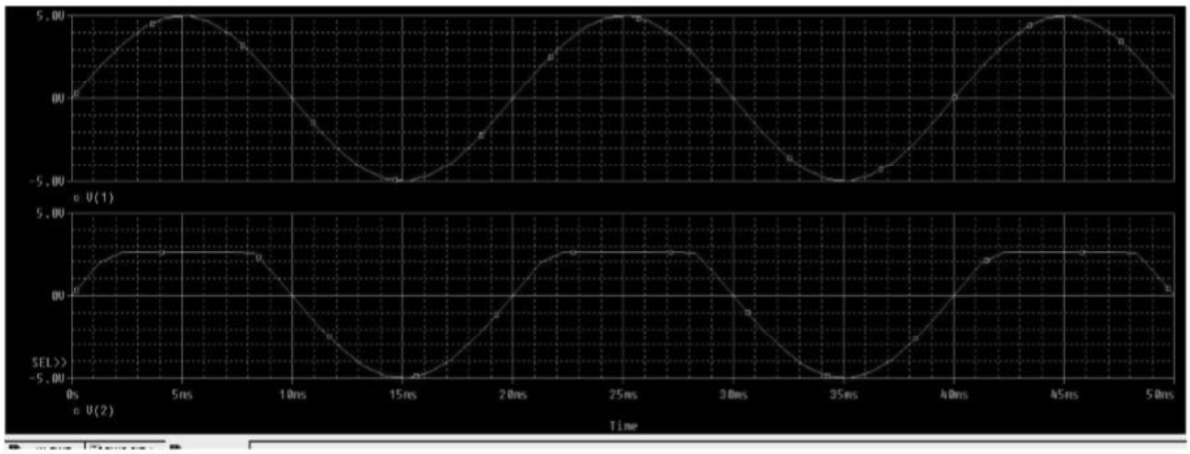
Biased negative Peak Clipper with negative reference



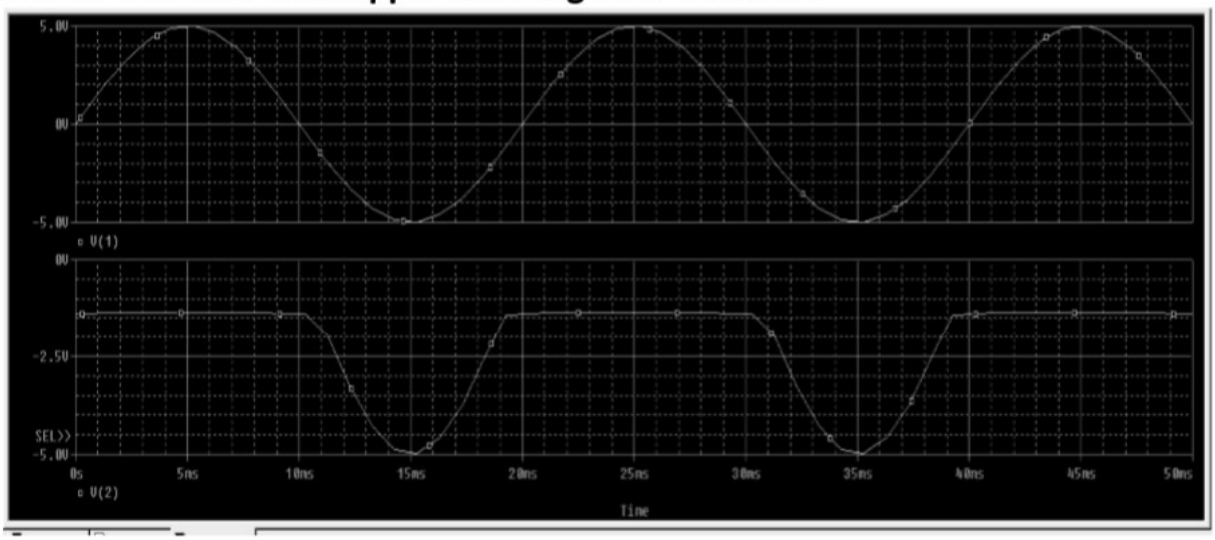
Two Way Clipper



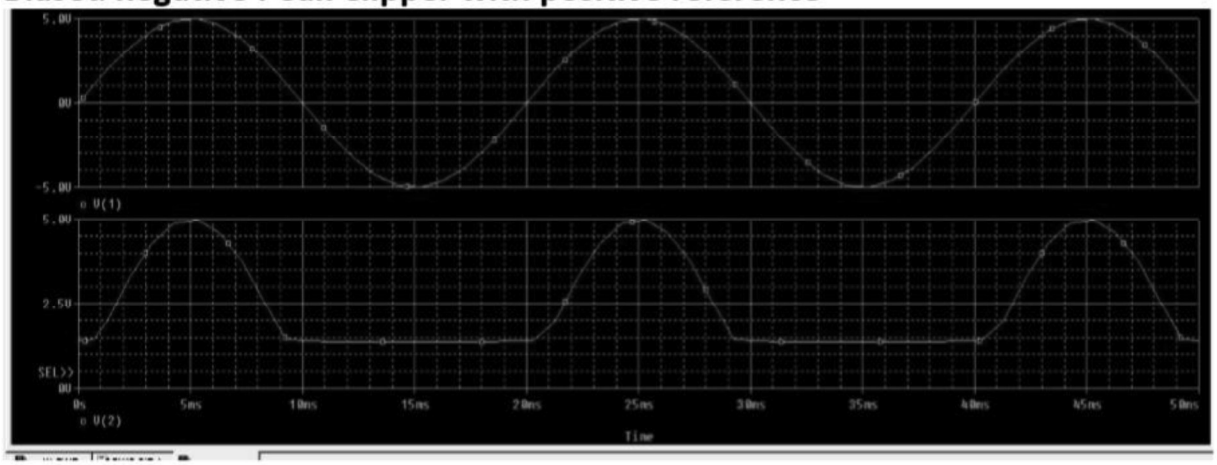
Biased Positive Peak Clipper with positive reference



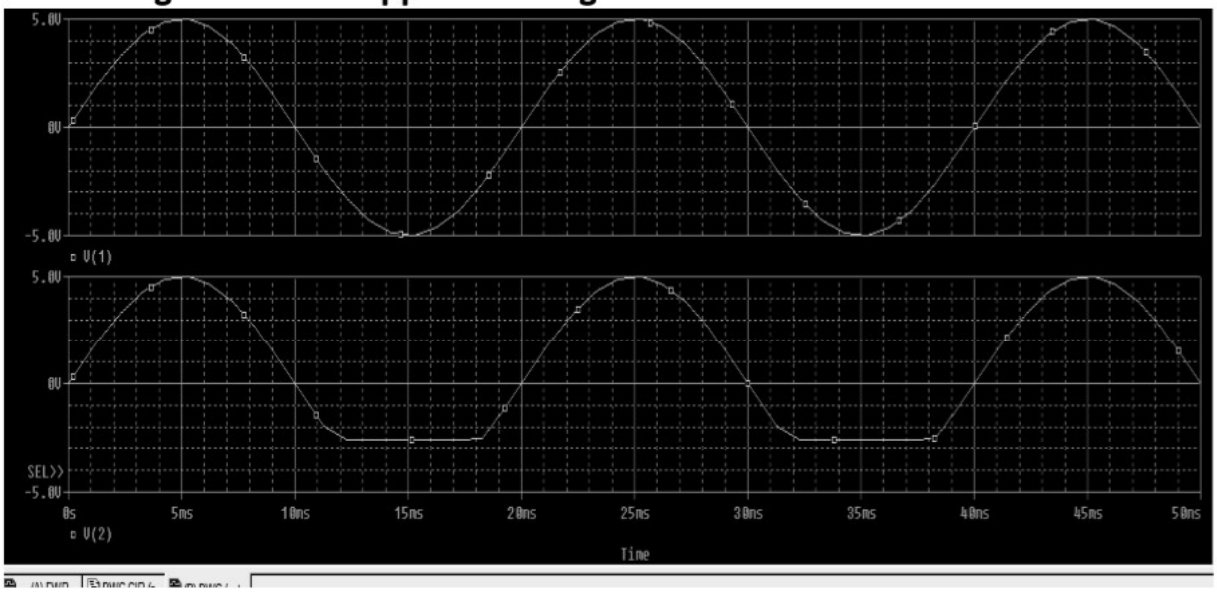
Biased Positive Peak Clipper with negative reference



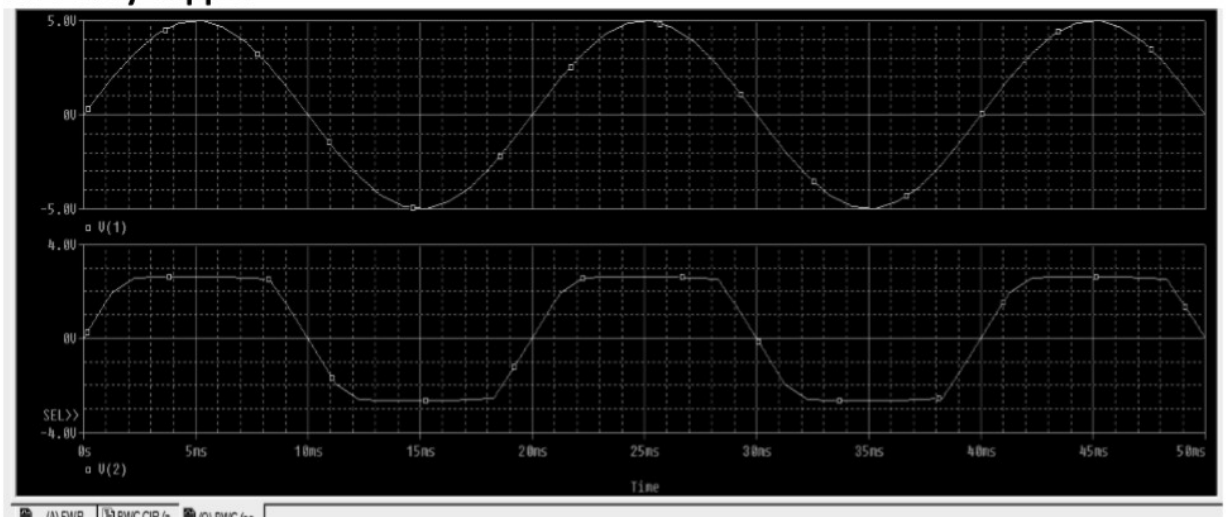
Biased negative Peak Clipper with positive reference



Biased negative Peak Clipper with negative reference



Two Way Clipper



Result ::Hence the design of Clippers is simulated using OrCADPspice 9.1

9.CLAMPERS

AIM: To verify the characteristics of CLAMPPERS

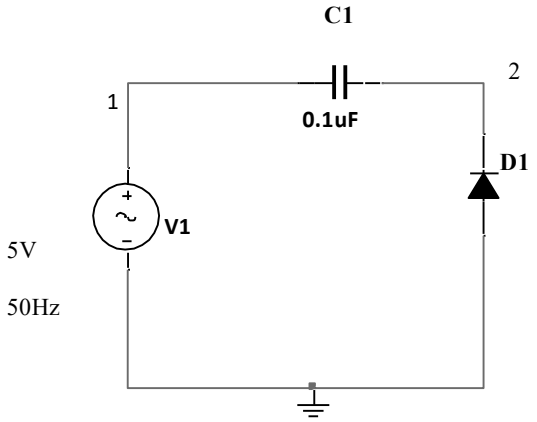
Software Required: OrCADPspice 9.1

Theory:

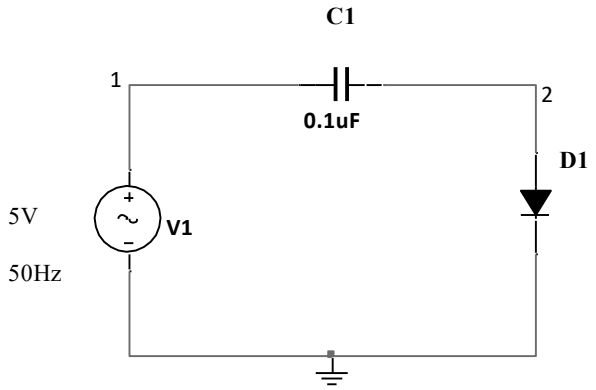
The circuits in Figure above are known as *clampers* or *DC restorers*. These circuits clamp a peak of a waveform to a specific DC level compared with a capacitively coupled signal which swings about its average DC level (usually 0V). If the diode is removed from the clamper, it defaults to a simple coupling capacitor– no clamping.

Circuit Diagram:

Unbiased Positive Clamper



Unbiased Negative Clamper

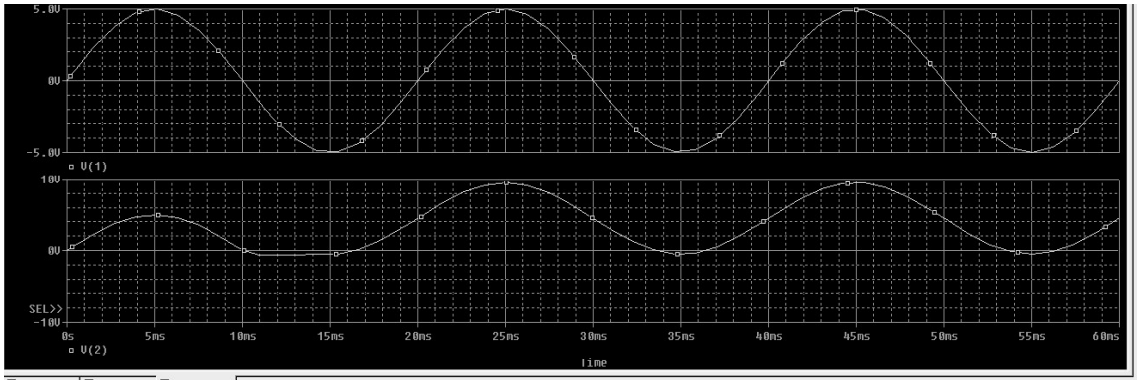



```
*CLAMPINGPOSITIVEPEAK
V1 1 0 sin(0 5 50)
C1 1 2 0.1uf
D1 0 2 mod1
.MODEL mod1 D
.TRAN 0 60ms
.PROBE V[1] V[2]
.END
```

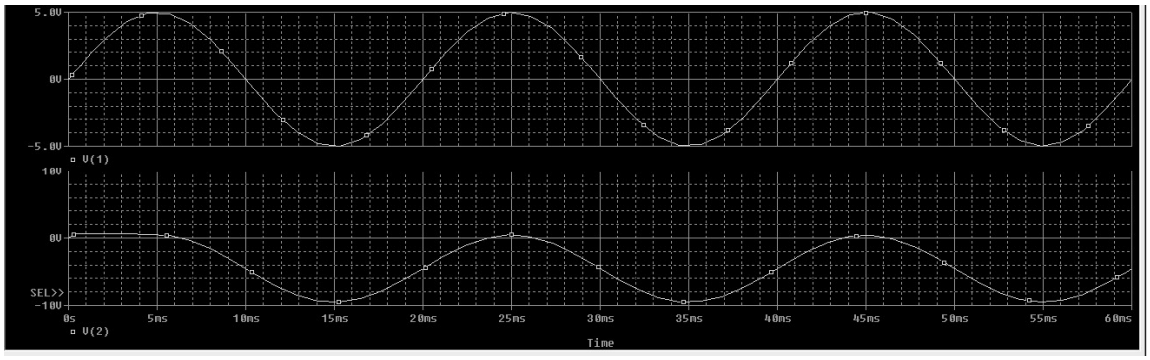
```
*CLAMPING NEGATIVE PEAK
V1 1 0 sin(0 5 50)
C1 1 2 0.1uf
D1 2 0 mod1
.MODEL mod1 D
.TRAN 0 60ms
.PROBE V[1] V[2]
.END
```

Output:

Unbiased Positive Clamper



Unbiased Negative Clamper



Result:

Hence the design of biased and unbiased clampers is simulated using OrCADPspice 9.1

10.LOGIC GATES

AIM: To verify the characteristics of *Basic Digital Gates-AND,OR,NOT*

Software Required: OrCADPspice 9.1

Theory:

A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions *low* (0) or *high* (1), represented by different voltage levels. The logic state of a terminal can, and generally does, change often, as the circuit processes data. In most logic gates, the low state is approximately zero volts (0 V), while the high state is approximately five volts positive (+5 V).There are seven basic logic gates: AND, OR, XOR, NOT, NAND, NOR, and XNOR.

The *AND gate* is so named because, if 0 is called "false" and 1 is called "true," the gate acts in the same way as the logical "and" operator. The following illustration and table show the circuit symbol and logic combinations for an AND gate. (In the symbol, the input terminals are at left and the output terminal is at right.) The output is "true" when both inputs are "true." Otherwise, the output is "false."

AND gate

Input 1	Input 2	Output
0	0	0
0	1	0
1	0	0
1	1	1

The *OR gate* gets its name from the fact that it behaves after the fashion of the logical inclusive "or." The output is "true" if either or both of the inputs are "true." If both inputs are "false," then the output is "false."

OR gate

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

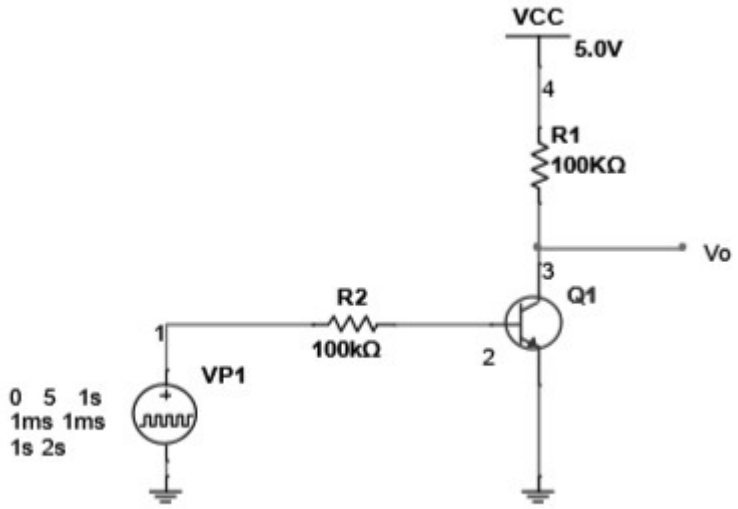
A logical *inverter* , sometimes called a *NOT gate* to differentiate it from other types of electronic inverter devices, has only one input. It reverses the logic state.

Inverter or NOT gate

Input	Output
1	0

Circuit Diagram:

NOT GATE

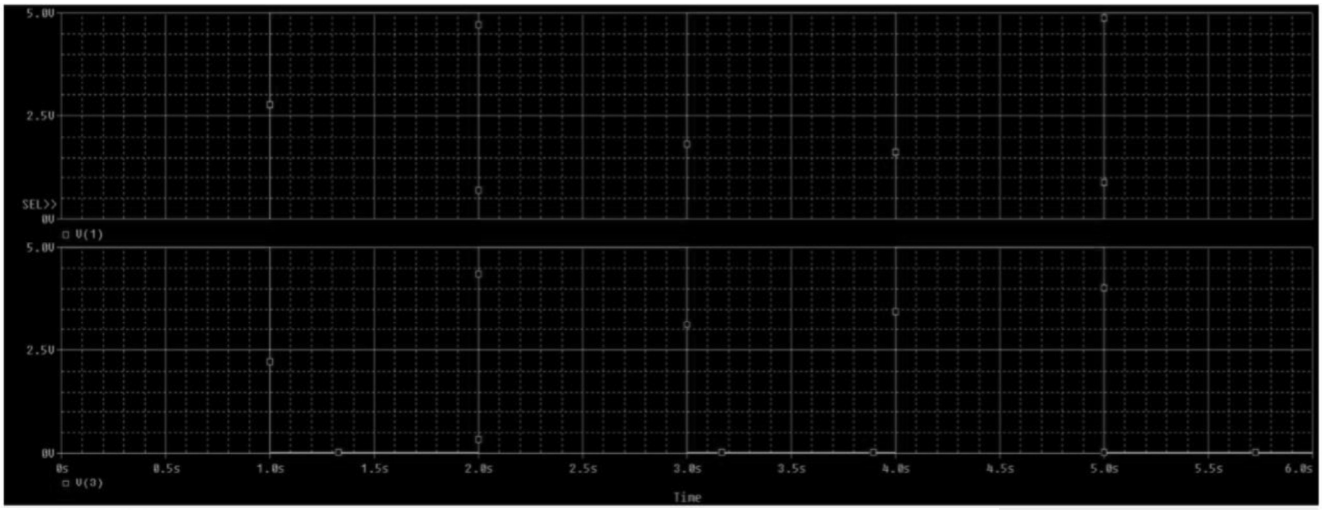


PSPICE Program:

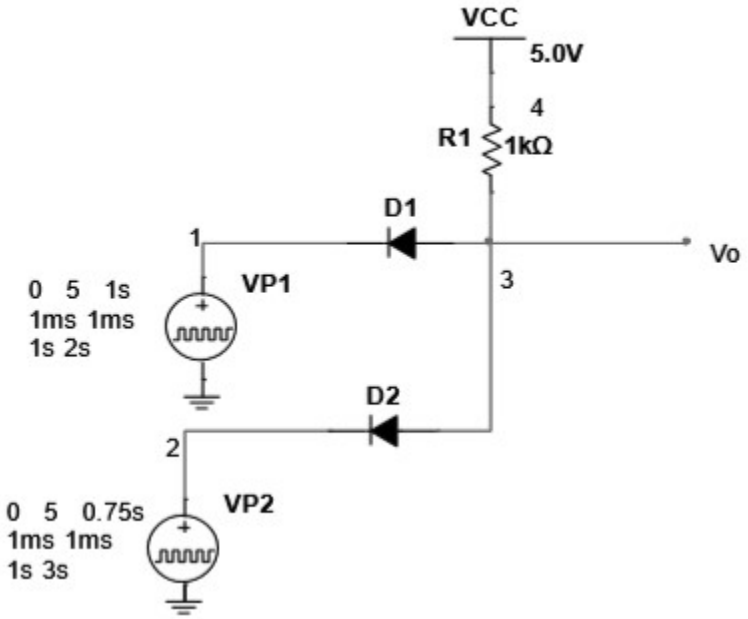
```
*NOT GATE
Vp1  0  Pulse(0,5,1s,1ms,1ms,1s,2s)
Rb  1  2  100k
Rc  4  3  100k
Vcc  4  0  5v
Q1  3  2  0
MOD1 .MODEL MOD1 NPN
.TRAN  0  6S
.PROBE
.END
```

Output:

NOT GATE

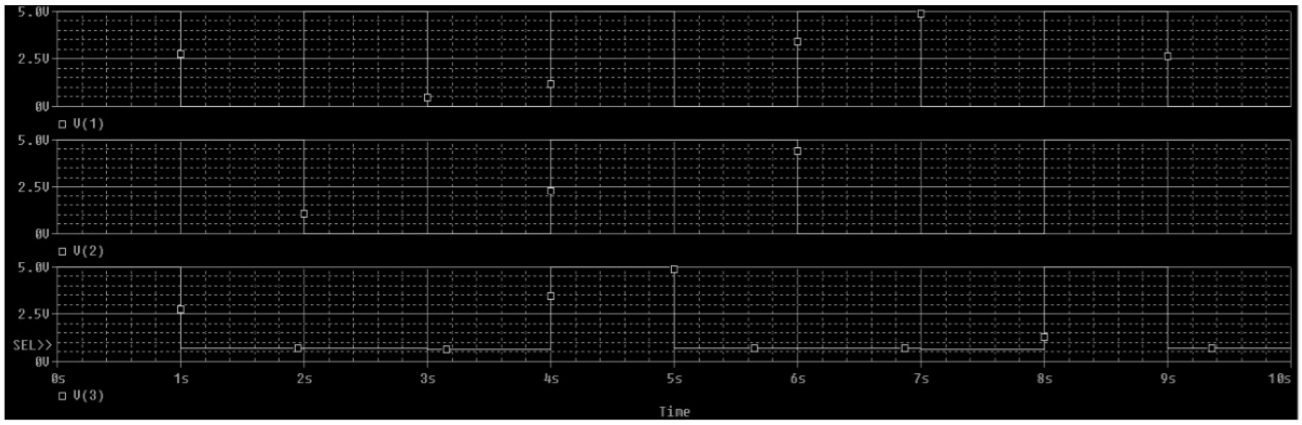


AND GATE

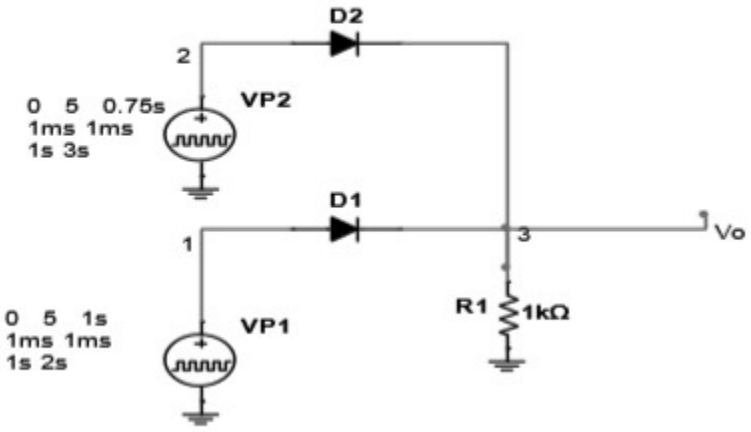


```
*AND GATE
Vp1  1  0  PULSE(5,0,1S,1MS,1MS,1S,2S)
Vp2  2  0  PULSE(5,0,2S,1MS,1MS,2S,4S)
R  3  4  1K
D1  3  1  MOD1
D2  3  2  MOD1
Vcc 4 0 DC 5v
.MODEL  MOD1  D
.TRAN  0  10S
.PROBE
.END
```

AND GATE

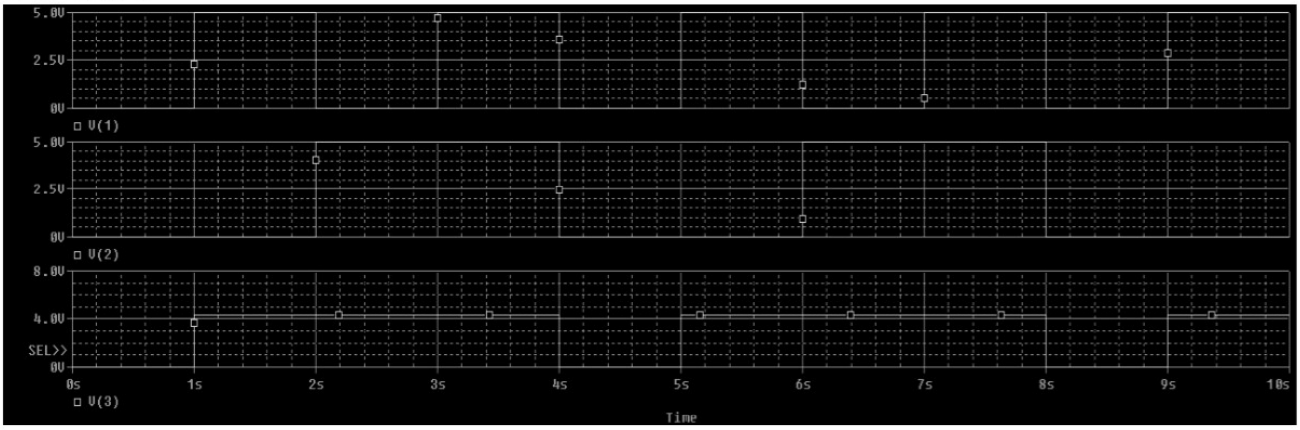


OR GATE



```
*OR GATE
Vp1  1  0  PULSE(0,5,1S,1MS,1MS,1S,2S)
Vp2  2  0  PULSE(0,5,2S,1MS,1MS,2S,4S)
R  3  0  1K
D1  1  3  MOD1
D2  2  3  MOD1
.MODEL  MOD1  D
.TRAN  0  10S
.PROBE
.END
```

OR GATE



Result:

Hence the design of logic gates is simulated using OrCADPspice 9.1

11.Wein Bridge Oscillator

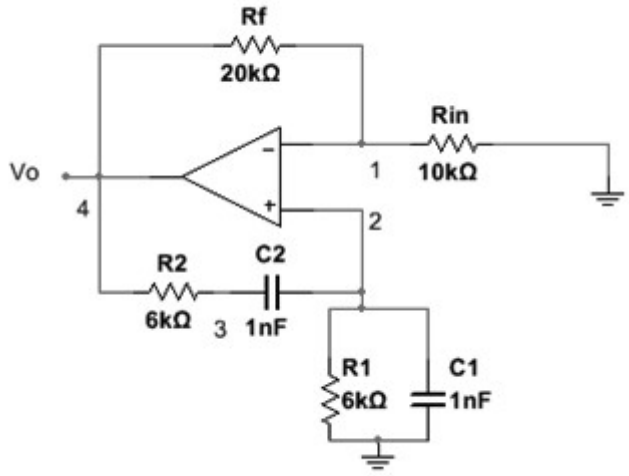
AIM: To verify the characteristics of wein Bridge Oscillator.

Software Required: OrCAD Pspice 9.1

Theory: The Wien bridge oscillator is one of the simplest oscillators. The figure below shows the basic Wien bridge circuit. OPAMP is used as the amplifying device and the Wien Bridge is used as the feedback element. The OPAMP is used in noninverting mode that provides a phase shift of 0^0. One can expect that the phase shift introduced by the feedback network also to be equal to 0^0 at the frequency of oscillations. The frequency of oscillations is,

$$f = \frac{1}{2\pi RC}$$

Circuit Diagram:

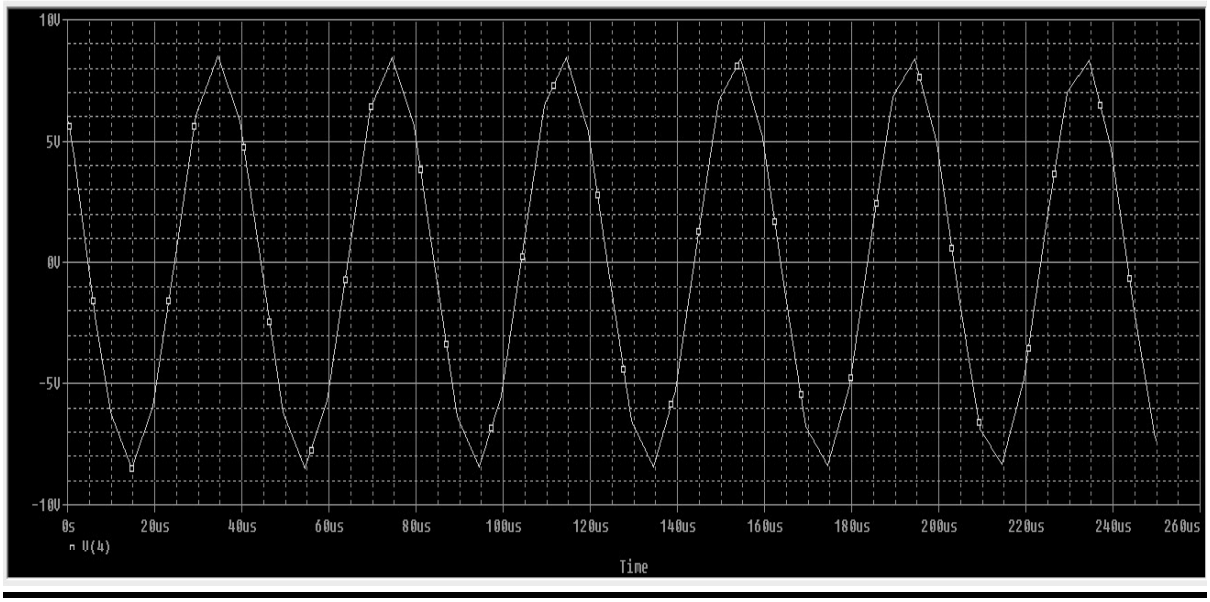


Pspice Program:

```
*wein bridge oscillator
.subckt opamp p_in n_in com out
Ri p_in n_in 1meg
Ro int out 50
Ex  int com p_in n_in 1e5
```

.ends
Ri1 1 0 10k
Rf 1 4 20k
R3 2 0 6k
c1 2 0 1nf (ic=2v)
c2 2 3 1nf
R4 3 4 6k
x1 2 1 0 4 opamp
.tran 0 0.25m
.probe
.end

Output:



Result:

Hence the design of wein bridge oscillator is simulated using OrCAD Pspice 9.1 and the waveform is observed.

11.CLASS -A POWER Amplifier

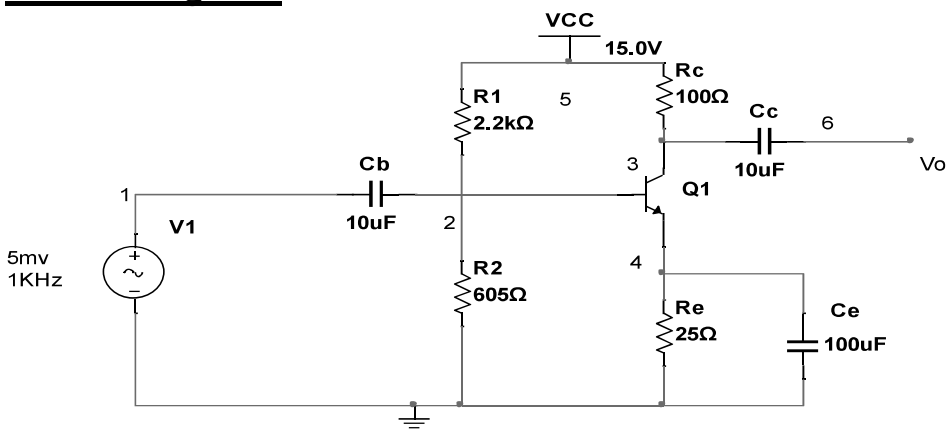
AIM: To verify the characteristics of CLASS A Power Amplifier

Software Required: OrcadPspice 9.1

Theory:

An electronic amplifieris used for increasing the power of a signal. It does this by taking energy from a power supply and controlling the output to match the input signal shape but with larger amplitude. In this sense, an amplifier may be considered as modulating the output of the power supply.

Circuit Diagram:



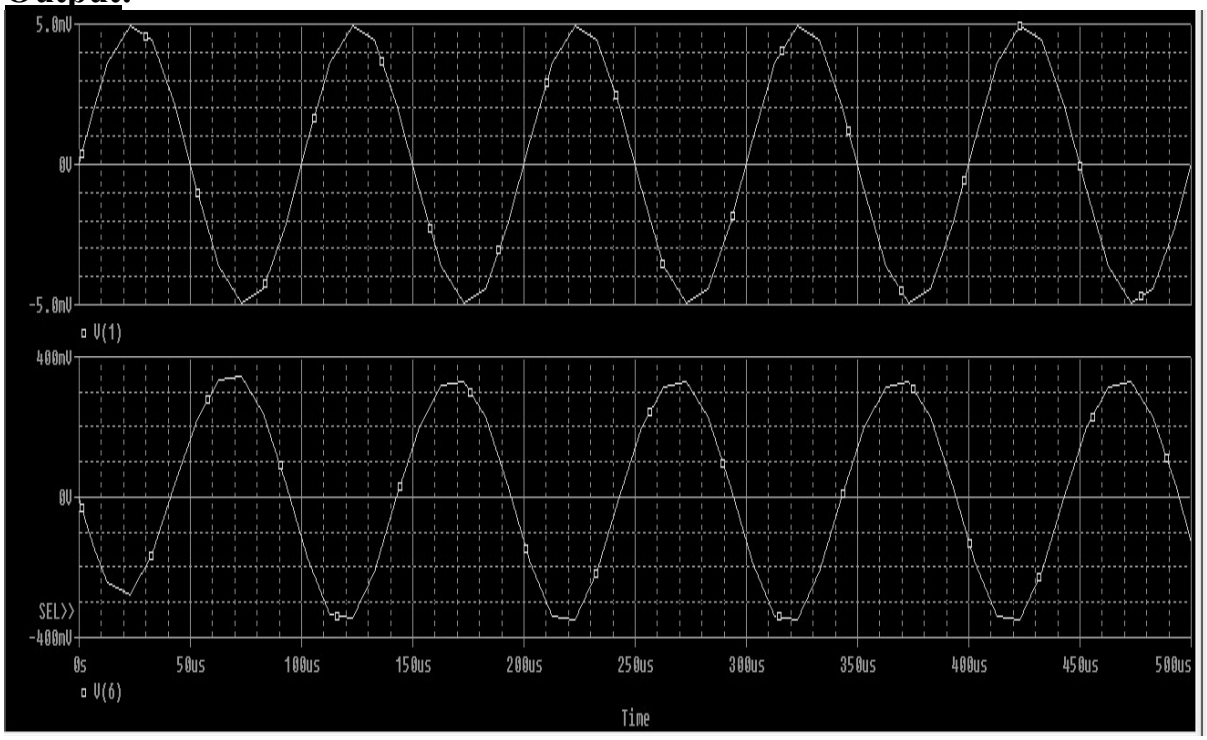
PSPICE Program:

*CLASS -A AMPLIFIER

VS 1 0 SIN(0 5MV 10KHZ)
VCC 5 0 15V
CB 1 2 10UF
CC 3 6 10UF
CE 4 0 100UF
R1 5 2 2.7K

```
R2 2 0 605
RC 5 3 100
RE 4 0 25
RL 6 0 47
Q1 3 2 4 SL100
.MODEL SL100 NPN
.TRAN 0.1MS 0.5MS
.PROBE
.END
```

Output:



Result:

Hence the design of Class-A power Amplifier is simulated using OrCAD Pspice 9.1 and their characterstics was observed.

12.VOLTAGE REGULATOR

AIM: Op Amp Regulator with Series-Pass Transistor

Software Required: OrCAD Pspice 9.1

Theory:

Here, we explain the general concept of using an operational amplifier for voltage regulation. By utilizing an op-amp and few other external components, we can easily build a linear voltage regulator. Apart for being a regulator, the same circuit is also a voltage stabilizer, able to stabilize voltage at a grade better than 0.01%. The circuit is powered from a non-stabilized DC-power source, and uses a transistor (T1) inside a feedback loop. The transistor is used to supply the load with much more current than the op-amp itself could possibly supply. The D1 diode is a Zener - type diode and it is used for voltage reference.

Basic op-amp voltage regulator
D1 is biased through Rz. When correctly reserve biased, the Zener diode keeps the voltage across its leads close to the Zener breakdown voltage. The op-amp is used as a linear voltage amplifier. Due to the high open loop voltage gain of the op-amp, and as far as the op-amp remains in its linear region, the voltage difference between its inverting (V_-) and non-inverting input (V_+) is almost equal to zero. In other words, the voltage at its non-inverting input, in respect to the ground, equals the voltage at its inverting input:

$V_-=V_+$ (1)

Equation (1) holds true for any op-amp working at its linear region (as an amplifier).

R1 and R2 form a voltage divider, and the voltage (V_-) at their connection point is also given by the well known voltage-divider formula:

$V_-=V_L \cdot R1/(R1+R2)$ (2)

However, V+ is also equal to the Zener breakdown voltage (Vz), because the non-inverting input of the op-amp is directly connected to the cathode of the Zener diode.

$V_+=V_Z$ (3)

After solving (1),(2) and (3), we get:

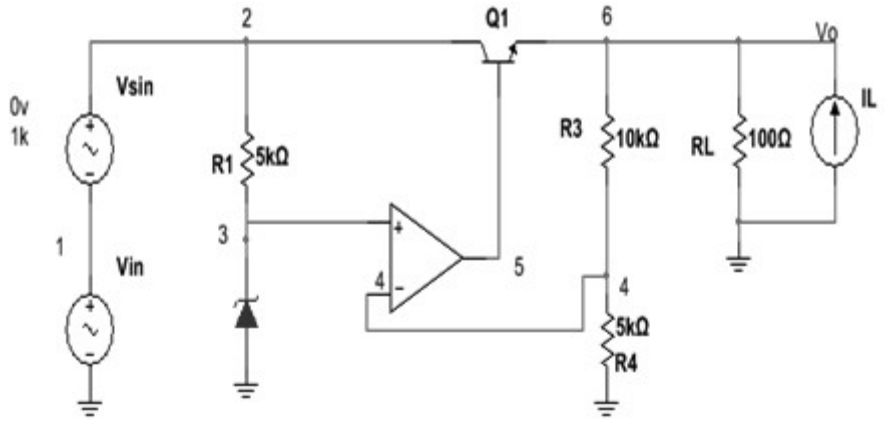
$V_L=V_Z \cdot (1+R2/R1)$ (4)

From equation (4), we conclude that V_L voltage (which is the voltage applied to the load) is directly proportional to the Zener voltage. As far as the Zener voltage remains stable, V_L also remains stable. Additionally, the voltage applied to the load, can be easily adjusted by adjusting R1, R2 or both of them. For continues voltage adjustment, R1 and R2 should replaced by a potentiometer, having its wiper at the non-inverting input of the op-amp, and its other leads at the ground and the V_L line, respectively.

V_L, is not possible to exceed V_{DC}. It can be almost as much high as V_{DC} when T1 saturates, but no more than this. V_L (the voltage at the load) could not also be lower than Vz. That's why $V_Z<V_L<V_{DC}$.

As in any linear regulator, heat losses on T1 increase when the output voltage decreases. In fact, the power loss due to heating is the current times the voltage dropped across T1. Besides heating losses, a linear regulator is often preferred over a switching one because it does not require any inductors which can be relatively expensive or bulky.

Circuit Diagram:



PSPICE Program:

```
*voltage regulator load regulation
.subckt opamp p_in n_in com out
Rin p_in n_in 1MEG
R0 int out 50
E1 int com p_in n_in 1e6
.ends
```

```
vin 1 0 DC 15
vsin 2 1 sin(0 0 1k)
R1 2 3 5k
D1 0 3 mod1
.model mod1 D(IS=1e-14 cjo=0.1pf Rs=0.1 BV=5v IBV=2ma)
x1 3 4 0 5 opamp
q1 2 5 6 mod2
.model mod2 npn
R3 6 4 10k
R4 4 0 5k
Rl 6 0 100
Il 6 0 PWL(0.5m 0.1A 2ms 0.2A)
.OP
.end
```

OUTPUT

voltage regulator

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

* NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

(1) 15.0000 (2) 15.0000 (3) 5.0002 (4) 4.9998

(5) 16.0050 (6) 14.9990 (x1.int) 395.6100

Result:

Hence the design of series voltage regulator using opamp is simulated using OrCAD Pspice 9.1 and their characterstics was observed.

13.Differential Amplifier

AIM: To verify the characteristics of Differential Amplifier

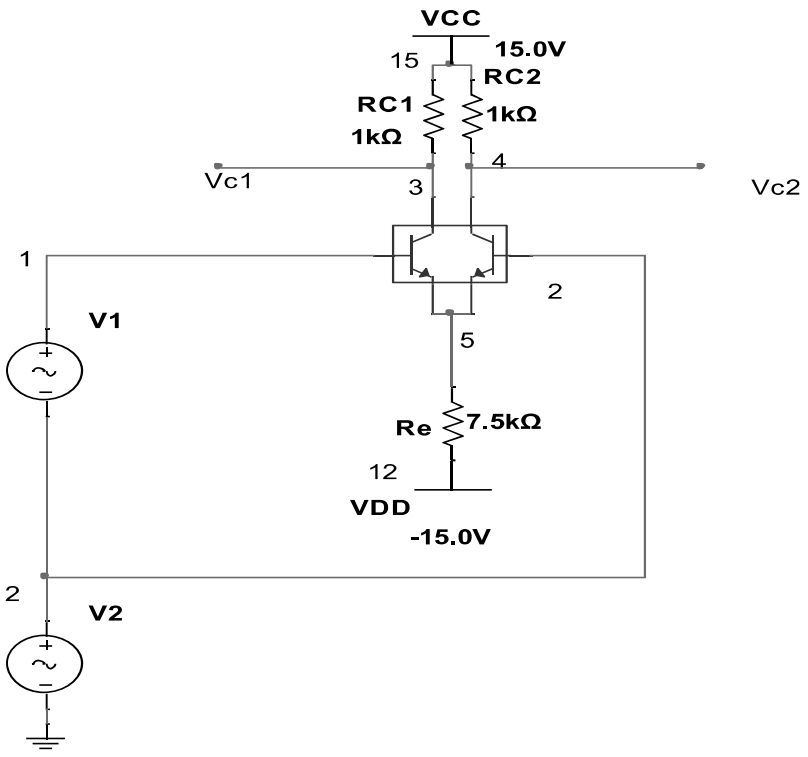
Software Required: OrcadPspice 9.1

Theory:

Look under the hood of most op amps, comparators or audio amplifiers, and you'll discover this powerful front-end circuit - the differential amplifier. A simple circuit able to amplify small signals applied between its two inputs, yet reject noise signals common to both inputs. This circuit has a unique topology: two inputs and two outputs. Although you can tap the signal from one output only, taking the difference between both outputs delivers twice the gain! And it improves Common-Mode Rejection (CMR), an essential function when the common-mode signal is a noise source or DC bias from a previous stage
GAIN AND REJECTION
How does this amplifier amplify differential signals and reject common ones? The bias condition assumes equal voltages at VB1 and VB2, forcing the bias current IE (set by RE) to split equally between the transistors resulting in IC1 = IC2. With RC1 = RC2, equal voltages develop at VC1 and VC2.

DIFFERENTIAL GAIN
Now suppose a differential signal is applied to the inputs. This will incrementally increase and decrease the base voltages to
VB1 + _V and *VB2 - _V*
Because Q1 conducts a little more and Q2 a little less, IE now splits unevenly creating
IC1 >IC2
This, in turn, forces the voltage at VC1 to decrease and VC2 to increase. The result: a voltage change at each output due to a differential input.

Circuit Diagram:



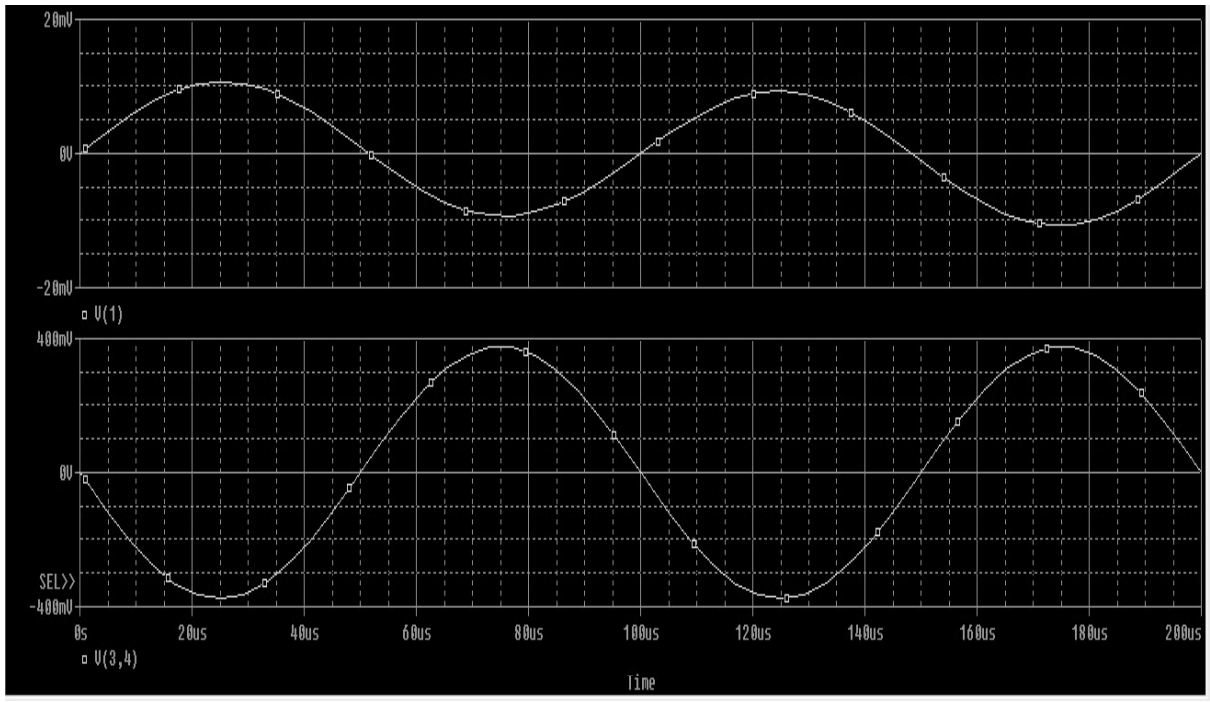
PSPICE Program:

```
*DIFFERENTIAL AMPLIFIER
VS 1 2 AC 1 SIN(0 10MVPEAK 10KHZ)
VCM 2 0 SIN(0 1MVPEAK 5KHZ)
VCC 11 0 DC +15V
VDD 12 0 DC -15V
Q1 3 1 5 mod1
Q2 4 2 5 mod1
RC1 11 3 1000
RC2 11 4 1000
RE 5 12 7.2K
.model mod1 NPN(Is=3.108f Cjc=14.57p Cje=26.08p)
.FOUR 10KHZ V(3,4)
.TRAN 5US 200US
.AC DEC 5 1K 100MEG
.PRINT TRAN V(3)
.PRINT AC V(3)
```

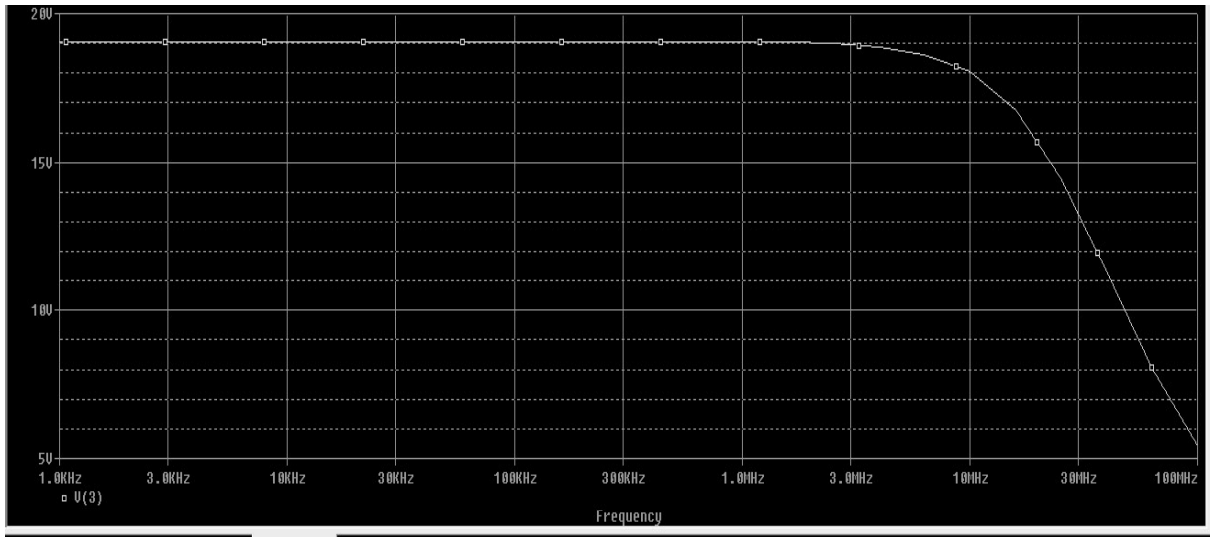
.PROBE
.END

Output:

Differential amplifier transient analysis:



Differential amplifier ac analysis:



Then we observe the output file and the total harmonic distortion is calculated

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(3,4)

DC COMPONENT = -4.401798E-05

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+04	3.750E-01	1.000E+00	1.800E+02	0.000E+00
2	2.000E+04	4.845E-05	1.292E-04	1.386E+02	-2.214E+02
3	3.000E+04	1.110E-03	2.960E-03	-1.791E+02	-7.191E+02
4	4.000E+04	1.311E-05	3.495E-05	-8.984E+01	-8.098E+02
5	5.000E+04	1.009E-05	2.690E-05	-1.028E+02	-1.003E+03
6	6.000E+04	8.513E-06	2.270E-05	-8.225E+01	-1.162E+03
7	7.000E+04	8.336E-06	2.223E-05	-8.848E+01	-1.348E+03
8	8.000E+04	9.202E-06	2.454E-05	-9.414E+01	-1.534E+03
9	9.000E+04	1.037E-05	2.764E-05	-9.760E+01	-1.717E+03

TOTAL HARMONIC DISTORTION = 2.963924E-01 PERCENT

Result:

Hence the design of differential amplifier is simulated using OrCAD Pspice 9.1 and their characteristics are observed.

14.ATTENUATOR

AIM: To verify the characteristics of ATTENUATOR

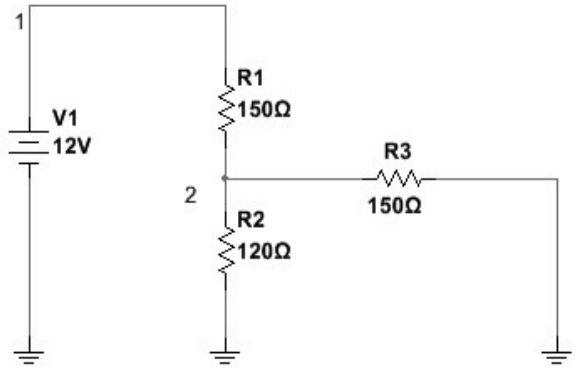
Software Required: OrcadPspice 9.1

Theory:

An **attenuator** is an electronic device that reduces the amplitude or power of a signal without appreciably distorting its waveform.

An attenuator is effectively the opposite of an amplifier, though the two work by different methods. While an amplifier provides gain, an attenuator provides loss, or gain less than 1. Attenuators are usually passive devices made from simple voltage divider networks. Switching between different resistances forms adjustable stepped attenuators and continuously adjustable ones using potentiometers. For higher frequencies precisely matched low VSWR resistance networks are used. Fixed attenuators in circuits are used to lower voltage, dissipate power, and to improve impedance matching. In measuring signals, attenuator pads or adaptors are used to lower the amplitude of the signal a known amount to enable measurements, or to protect the measuring device from signal levels that might damage it. Attenuators are also used to 'match' impedances by lowering apparent SWR

.**Circuit Diagram:**



PSPICE Program:

```
*ATTENUATORS

V1 1 0 12V

R1 1 2 150

R2 2 0 120

R3 2 0 150

.PROBE

.END
```

Output:

```
*ATTENUATORS

 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000
DEG C

**********************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE
VOLTAGE


(   1)   12.0000 (   2)    3.6923
```

Result:

Hence the design of attenuators is simulated using OrCAD Pspice 9.1 and their characteristics are observed.

15.RC COUPLED AMPLIFIER

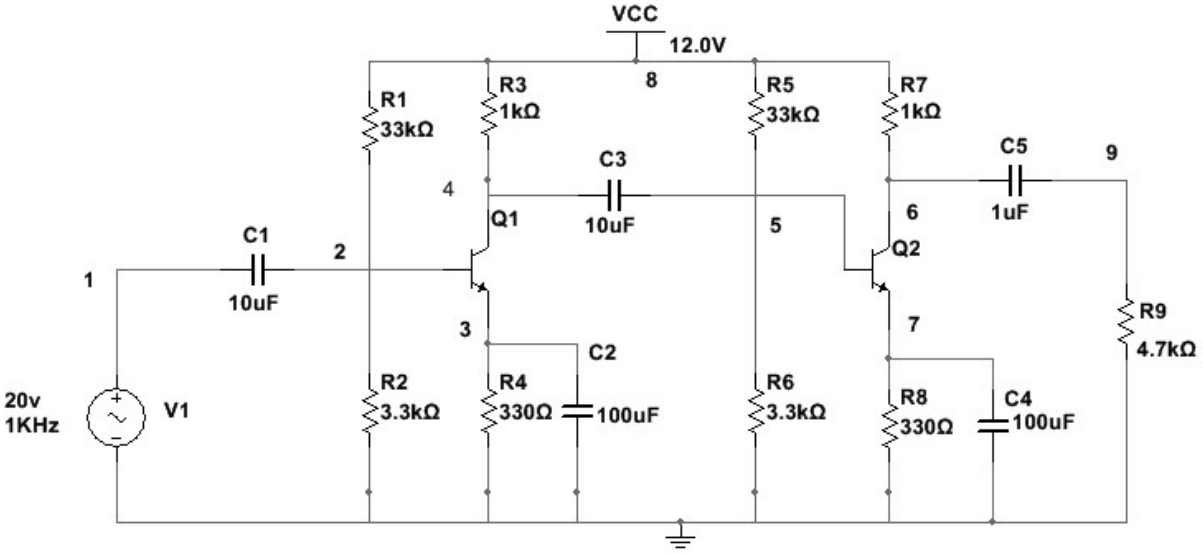
AIM: To verify the characteristics of RC Coupled Amplifier

Software Required: OrcadPspice 9.1

Theory:

When a.c. signal is applied to the base of the first transistor, it is amplified and developed across the out of the 1st stage. This amplified voltage is applied to the base of next stage through the coupling capacitor Cc where it is further amplified and reappears across the out put of the second stage. Thus the successive stages amplify the signal and the overall gain is raised to the desired level. Much higher gains can be obtained by connecting a number of amplifier stages in succession (one after the other). Resistance-capacitance (RC) coupling is most widely used to connect the output of first stage to the input (base) of the second stage and so on. It is the most popular type of coupling because it is cheap and provides a constant amplification over a wide range of frequencies. The above shows the circuit arrangement of a two stage RC coupled CE mode transistor amplifier where resistor R is used as a load and the capacitor C is used as a coupling element between the two stages of the amplifier.

Circuit Diagram:



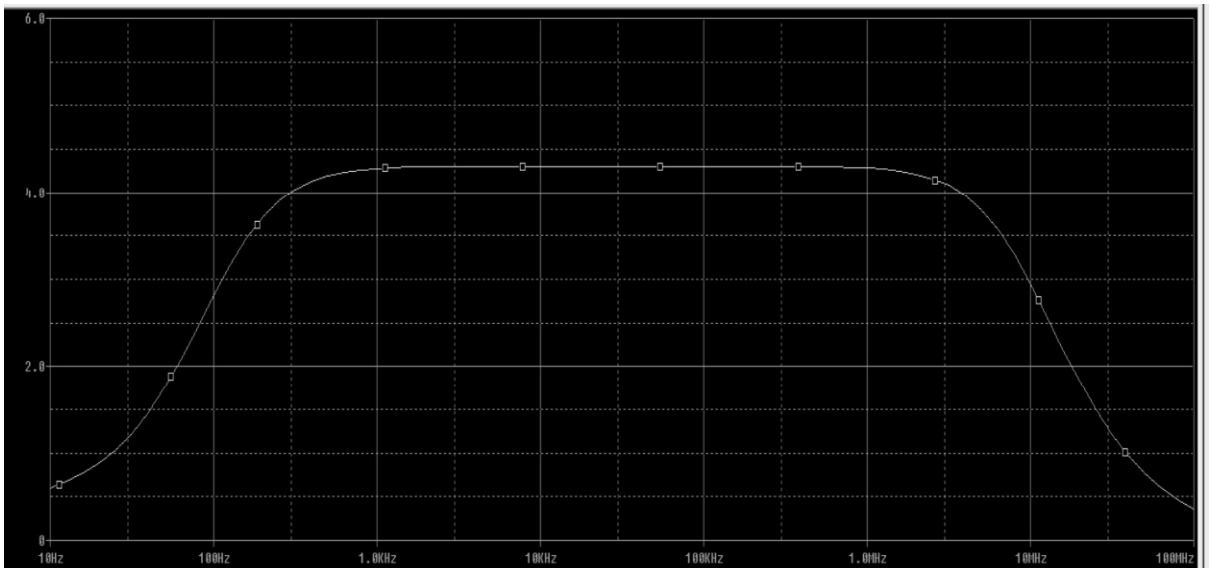
PSPICE Program:

```
*RC COUPLED AMPLIFIER

V1 1 0 AC 5MV SIN(0 50M 5K)

R1 1 8 33k

R2 2 0 3.3k

R3 4 8  1k

R4 3 0 330

R5 5 8 33k

R6 5 0 3.3K

R7 6 8 1k

R8 7 0 330

R9 9 0 4.7k

C1 1 2 10UF

C2 3 0 100UF

C3 4 5 10UF

C4 7 0 100UF

C5 6 9 10UF

Q1 4 2 3 MOD1

Q2 6 5 7 MOD1

VCC 8 0 12V

.MODEL MOD1 NPN

.TRAN 0 5m

.AC DEC 10 10 1000MEG
```

.PROBE

.END

Output:



Result:

Hence the design of RC coupled Amplifier is simulated using OrCAD PSPICE 9.1 and their characteristics were observed.