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(57) Abstract :
The arithmetic logic unit is one of the most important components of the Central Processing Unit (CPU) that can be part of a programmable reversible computing device. Reversible logic is one of the emerging technologies having promising applications in quantum computing; it also finds its wide range of applications in the fields of optical computing, quantum computing, complementary metal oxide semiconductors, and nanotechnology. The ALU is a digital electronic circuit that conducts operations on binary numbers in arithmetic and logical operations. However, conventional ALUs constructed by using the irreversible logic gates are used for their substantial power consumption, presenting a pressing need for more energy-efficient alternatives in digital system design. In response to this challenge is the development of a 32-bit ALU utilizing reversible logic gates, with the dual objective of reducing power consumption and enhancing computational performance. So, there is a need for low-power-consuming ALU designs. The proposed 32-bit ALU seeks to revolutionize digital system design by offering a solution that not only optimized complexity of design, power, delay and garbage outputs. Therefore, the aim is to contribute to the advancement of digital system design, addressing the critical need for energy-efficient solutions in today's technology-driven world. The simulation and synthesis are carried out with the Xilinx Vivado Software, and it was implemented on the Nexys 4 DDR, a platform featuring the latest Artix FPGA.

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