**20CS205/20CB205/20DS205/20IT205**

**Hall Ticket Number:**

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| **I/IV B.Tech (Regular) DEGREE EXAMINATION** | | | |
| **October, 2021** | **Common to CSE/CS/CB and IT** | | |
| **Second Semester** | **Digital Logic Design** | | |
| **Time:** Three Hours | | **Maximum: 7**0 Marks | |
| *Answer Question* ***No. 1*** *Compulsorily.* | | | (14X1 = 14 Marks) |
| *Answer* ***ONE*** *question from each* ***Unit.*** | | | (4X14=56Marks) |

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| 1. Answer the following. (14X1=14 Marks) | | | | | |
|  | a) | Convert (110100) binary to gray. | CO1 | |  |
|  | b) | Write the NAND gate truth table. | CO1 | |  |
|  | c) | Convert (0.513)10 to Binary. | CO1 | |  |
|  | d) | State Demorgan’s laws. | CO1 | |  |
|  | e) | Define Encoder | CO2 | |  |
|  | f) | Define Full adder | CO2 | |  |
|  | g) | Draw the logic diagram of Half adder. | CO2 | |  |
|  | h) | Define Latch. | CO3 | |  |
|  | i) | What is sequential circuit. | CO3 | |  |
|  | j) | Define Truth table | CO3 | |  |
|  | k) | Define T Flip Flop | CO3 | |  |
|  | l) | Define Counter? | CO4 | |  |
|  | m) | What is shift register. | CO4 | |  |
|  | n) | Define PLD. | CO4 | |  |
| **Unit - I** | | | | | |
| 2. | a) | Convert ( 2598 ) 10 to Hexadecimal & ( 1010011101100111 )2 to octal and Decimal. | CO1 | **7M** | |
|  | b) | Generate the Hamming code word for the message 1011010101. | CO1 | **7M** | |
|  |  | **(OR)** |  |  | |
| 3. | a) | Draw the truth tables for AND,OR,NOT,EXOR,NAND & EXNOR Gates. | CO1 | **7M** | |
|  | b) | Minimize the following function using K-map  F(A,B,C,D) = ∑ m (0,2,4,6,7,8,10,12,13,15) | CO1 | **7M** | |
| **Unit - II** | | | | | |
| 4. |  | Minimize the following Boolean function using tabulation method and determine the prime implecants and select the prime implecants for the given Boolean function  f(w,x,y,z) = Σm(1,2,3,7,8,9,10,12,15). | CO2 | **14M** | |
|  |  | **(OR)** |  |  | |
| 5. | a) | Design 3 to 8 Decoder | CO2 | **7M** | |
|  | b) | Design the Boolean function F= ∑m(0,1,3,5,7) with the 4\*1 Multiplexer | CO2 | **7M** | |
| **Unit - III** | | | | | |
| 6. | a) | Explain Design procedure for Sequential circuits | CO3 | **7M** | |
|  | b) | Analyze the working of clocked JK flip flop and explain about the race around condition | CO3 | **7M** | |
|  |  | **(OR)** |  |  | |
| 7. | a) | Explain D flip-flop in detail and write the characteristic and excitation table. | CO3 | **7M** | |
|  | b) | Explain the design procedure for State Reduction & state Assignment | CO3 | **7M** | |
| **Unit - IV** | | | | | |
| 8. | a) | Draw and explain Bi - directional Shift Register. | CO4 | **7M** | |
|  | b) | Design a 3 bit Synchronous up counter. | CO4 | **7M** | |
|  |  | **(OR)** |  |  | |
| 9. | a) | Write the differences between PROM,PAL and PLA | CO4 | **7M** | |
|  | b) | Explain different types of ROM’s. | CO4 | **7M** | |

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| **DIGITAL LOGIC DESIGN**  I B.Tech – II Semester(Code:20CS205/CS02) | | | |
| Lectures: | **4** Periods / Week | Continuous Internal Assessment: | **30** Marks |
| Final Exam: | **3** hours | Semester End Exam: | **70** Marks |
| **UNIT-I** | | | **14 Periods** |
| **DIGITAL SYSTEMS AND BINARY NUMBERS:** Digital System, Binary Numbers, Number base Conversions, Octal and Hexadecimal Numbers, Complements of Numbers, Signed Binary Numbers, Binary Codes, Binary Storage and Registers, Binary Logic, Error Detection and Correction: 7 bit Hamming Code.  **BOOLEAN ALGEBRA & LOGIC GATES**: Introduction, Basic definitions, Axiomatic definition of Boolean algebra, Basic theorems and properties of Boolean algebra, Boolean functions, Canonical and Standard Forms, Other Logic Operations, Digital logic gates.  **GATE –LEVEL MINIMIZATION**: Introduction, The map method, Four-variable K-Map, Product-of-Sums Simplification, Don’t –Care Conditions, NAND and NOR implementation, Other Two level Implementations. | | | |
| **UNIT-II** | | | **14 Periods** |
| **MINIMIZATION:** The Tabulation method, Determination of prime implicants, Selection of prime-implicants.  **COMBINATIONAL LOGIC:** Introduction, Combinational Circuits, Analysis Procedure, Design Procedure, Binary Adders - Subtractor, Decimal Adder, Magnitude Comparator, Decoders, Encoders, Multiplexers. | | | |
| **UNIT-III** | | | **14 Periods** |
| **SYNCHRONOUS SEQUENTIAL LOGIC:** Introduction, Sequential Circuits, Storage Elements - Latches, Storage Elements -Flip Flops, Analysis of Clocked Sequential Circuits: State Equations, State Table, State Diagram, Flip Flop Input Equations, Analysis with D, JK and T Flip Flops; State reduction and Assignment, Design Procedure. | | | |
| **UNIT-IV** | | | **14 Periods** |
| **REGISTERS and COUNTERS**: Registers, Shift registers, Ripple Counters, Synchronous Counters.  **MEMORY and PROGRAMMABLE LOGIC:** Introduction, Random Access Memory: Read and Write Operations, Types of Memories; Read Only Memory, Programmable Logic Devices: PROM, PLA, PAL. | | | |
| **Text Book(s) :** | 1. M. Morris Mano, Michael D. Ciletti, “Digital Design”, 5th Edition, Prentice Hall, 2013. 2. A.Anand Kumar, “fundamentals of digital circuits”, 4th Edition, PHI. | | |
| **References :** | 1. John F. Wakerly, “Digital Design: Principles and Practices”, 4th Edition, Pearson, 2006. 2. Brian Holdsworth , Clive Woods, “Digital Logic Design”, 4th Edition, Elsevier Publisher, 2002. 3. Donald E Givone, “digital principles and design”, TMT. | | |