**20EC206**

**Hall Ticket Number:**

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| **I/IV B.Tech (Regular) DEGREE EXAMINATION** | | | |
| **October, 2021** | **Electronics and Communication Engineering** | | |
| **Second Semester** | **Fundamentals of Digital Electronics** | | |
| **Time:** Three Hours | | **Maximum: 7**0 Marks | |
| *Answer Question* ***No. 1*** *Compulsorily.* | | | (1X14 = 14 Marks) |
| *Answer* ***ONE*** *question from each* ***Unit.*** | | | (4X14=56 Marks) |

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| 1. | a) | Convert the binary number (01011.1011)2 into decimal. | CO1 |  |
|  | b) | Convert the following number (52)7 with the given radix to decimal | CO1 |  |
|  | c) | Convert the binary number 11011101 to gray code. | CO1 |  |
|  | d) | Find the dual of the function: A'B(C+D)+B'C'D+AB'C. | CO2 |  |
|  | e) | Define the essential prime implicants in a K-map method | CO2 |  |
|  | f) | What are universal gates and why they are called so? | CO2 |  |
|  | g) | How many minimum number of NAND gates are required to realize EX –NOR gate. | CO2 |  |
|  | h) | Why a multiplexer is called a data selector? | CO4 |  |
|  | i) | Define encoder and mention its applications. | CO4 |  |
|  | j) | Define combinational circuit. | CO4 |  |
|  | k) | Draw the truth table of Half Adder. | CO3 |  |
|  | l) | Write the Boolean expression for Ex-OR gate. | CO3 |  |
|  | m) | Draw the logic diagram of Half Subtractor. | CO3 |  |
|  | n) | Implement AND gate with NAND gates. | CO3 |  |
| **Unit-I** | | | | |
| 2. | a) | Perform the following addition using BCD code i)386+756 ii)576 + 444 | CO1 | 7M |
|  | b) | How are negative numbers represented? Represent signed numbers from +7 to -8 using 1’s complement and 2’s complement representation. | CO1 | 7M |
|  |  | **(OR)** |  |  |
| 3. | a) | Generate Hamming code for a 4-bit1001 message to detect and correct single bit errors. | CO1 | 7M |
|  | b) | Encode the decimal numbers using 6, 3, 1,-1 weighted code. Is it a self- complementing code? | CO1 | 7M |
|  |  | **Unit-II** |  |  |
| 4. | a) | F (A, B, C, D) = πM + [5, 8, 14] + dM [7, 11, 12, 13, 15]. Obtain minimal sop function. | CO2 | 7M |
|  | b) | Simplify the following using K- map and implement the same using gates.  Y (A, B, C) =∑(0,2,4,5,6,7) | CO2 | 7M |
|  |  | **(OR)** |  |  |
| 5. | a) | For the given Boolean function F=x y’ z + x’ y’ z +w’ x y + w x’ y + w x y   1. Simplify the function to minimal literals using Boolean algebra. 2. Construct the logic diagram AND-OR-Invert (AOI) logic. | CO3 | 7M |
|  | b) | Represent and draw the following Boolean function using minimum number of basic gates (i) (AB + AB’) (AB)’ (ii) [(ABD(C + D + E)) + (A +DBC)’] (ABC + (CAD)’) | CO3 | 7M |
|  |  | **Unit-III** |  |  |
| 6. | a) | Derive Boolean expression for a 2 input Ex-NOR gate to realize with 2 input NOR gates without using complemented variables and draw the circuit.. | CO3 | 7M |
|  | b) | Design Full adder and implement using basic gates. | CO3 | 7M |
|  |  | **(OR)** |  |  |
| 7. | a) | How can a NOR gate be used as an inverter, AND gate and OR gate? Explain with logical diagrams. | CO3 | 7M |
|  | b) | Design BCD to gray code converter and realize using logic gates. | CO3 | 7M |
|  |  | **Unit-IV** |  |  |
| 8. | a) | Implement the following Boolean functions with a decoder   1. F1=Σ(3, 6, 7, 10, 13, 15) 2. F2=Σ(1, 9, 12, 15) 3. F3=Σ(2, 6, 8, 10, 14, 15) | CO4 | 7M |
|  | b) | Design a 1:8 de-multiplexer using two1:4 de-multiplexer. | CO4 | 7M |
|  |  | **(OR)** |  |  |
| 9. | a) | Implement the following Boolean function with 8X1 multiplexer and external gates: F(A, B, C, D)=Σ(1, 3, 4, 11, 12, 13, 14, 15) | CO4 | 7M |
|  | b) | Design and implement 2 bit magnitude comparator with basic gates. | CO4 | 7M |

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