**18EC305**

**Hall Ticket Number:**

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| **II/IV B.Tech(Regular / Supplementary) DEGREE EXAMINATION** | | | |
| **February, 2021** | **Electronics and Communication Engineering** | | |
| **Third Semester** | **Digital Electronics** | | |
| **Time:** Three Hours | | **Maximum:**50 Marks | |
| *Answer ALL Questions from PART-A.* | | | (10X1 = 10 Marks) |
| *Answer* ***ANY FOUR*** *questions from PART-B.* | | | (4X10=40 Marks) |
| Part - A | | | |

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| 1. | Answer all questions | | | (10X1=10 Marks) | | |
|  | a) | | Convert the octal number 615 to its equivalent hexadecimal number | |  |  |
|  | b) | | Represent -9 in signed-magnitude and 1’s complement 8-bit form | |  |  |
|  | c) | | Simply the expression A+AB’+A’B | |  |  |
|  | d) | | Write NAND gate IC number and its pin configuration | |  |  |
|  | e) | | Implement NOR function using only NAND gates | |  |  |
|  | f) | | Write ‘D’ Flip-Flop characteristic equation | |  |  |
|  | g) | | Difference between a decoder and multiplexer | |  |  |
|  | h) | | Write any two difference between PAL and PLA | |  |  |
|  | i) | | List the basic characteristics of logic families | |  |  |
|  | j) | | Size of a ROM to implement a full adder | |  |  |
|  | | **Part - B** | | | | |
| 2. | a) | | The Hamming code 1 0 1 1 0 1 1 0 1 is received. Correct errors. There are 4 parity bits and odd parity is used. | | | 5M |
|  | b) | | Perform the 15’s complement subtraction for the following.  (i)(B02)16–(98F)16 (ii) (69B)16-(C14)16 | |  | 5M |
|  | |  | | | | |
| 3. | a) | | Explain the Classification of Binary Codes. | |  | 5M |
|  | b) | | Simplify the Boolean expression AB+(AC)’+A(B’)C(AB+C) | |  | 5M |
|  | |  | | | | |
| 4. | a) | | Simply the following function using K-map f (a, b, c, d) = ∑ (1,3,7,11,15) +∑d(0, 2, 4) | | | 5M |
|  | b) | | Design full adder using two half adders and OR gate | |  | 5M |
|  | |  | | | | |
| 5 | a) | | Simplify the following Boolean function by using a Quine-McCluskey method.  F (A, B, C, D) = ∑m (0, 1, 3, 4, 5, 7, 10,13, 14, 15) | |  | 7M |
|  | b) | | Implement Ex-NOR gate using NOR gate only. | |  | 3M |
|  | |  | | | | |
| 6. | a) | | What is the advantage of Master slave JK Flip-Flop? Explain its operation with neat sketch. | | | 5M |
|  | b) | | Explain the SR flip-flop and D flip-flop with neat logic diagram. | |  | 5M |
|  | | | | | | |
| 7. | a) | | Explain the operation of carry look ahead adder | |  | 5M |
|  | b) | | Implement the following Boolean function using 8:1 MUX  F(A, B, C) = ∑m(0, 1, 3, 4 ,8, 9, 15) | |  | 5M |
|  | | | | | | |
| 8. |  | | Design a synchronous BCD counter using T Flip-flop | |  | 10M |
|  | |  | | | | |
| 9. | a) | | Explain DTL logic family with neat sketch. | |  | 5M |
|  | b) | | Compare the logic families PLA, PAL and ROM | |  | 5M |

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