**18EC405**

**Hall Ticket Number:**

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| **II/IV B.Tech(Regular/Supplementary) DEGREE EXAMINATION** | | | |
| **August, 2021** | **Electronics and Communication Engineering** | | |
| **Fourth Semester** | **Digital Design using HDL** | | |
| **Time:** Three Hours | | **Maximum:**50 Marks | |
| *Answer Question No. 1 Compulsorily.* | | | (10X1 = 10 Marks) | |
| *Answer* ***ANY ONE*** *question from each Unit.* | | | (4X10=40 Marks) | |
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| 1. | a) | Give an example for Module Instantiation | CO1 | |  |
|  | b) | What are the different types used in Verilog. | CO1 | |  |
|  | c) | List the components of simulation. | CO2 | |  |
|  | d) | Define relational operator. | CO2 | |  |
|  | e) | Explain difference between bitwise and reduction operator. | CO2 | |  |
|  | f) | Explain lumped delay. | CO3 | |  |
|  | g) | Generate a free running clock with 50% duty cycle and time period of 20 time units. | CO3 | |  |
|  | h) | Define named event control with an example. | CO3 | |  |
|  | i) | Define rise and fault time. | CO4 | |  |
|  | j) | What are the parts in UDP? | CO4 | |  |
| **Unit - I** | | | | | |
| 2. | a) | Draw and explain the Design Flow for designing VLSI IC circuits | CO1 | **5M** | |
|  | b) | Explain different data type of Verilog HDL with examples. | CO1 | **5M** | |
|  |  | **(OR)** |  |  | |
| 3. | a) | Explain digital design methodologies with example. | CO1 | **5M** | |
|  | b) | Explain about system task and compiler directives. | CO1 | **5M** | |
| **Unit – II** | | | | | |
| 4. |  | Design a 4-bit ripple carry adder using 1-bit full adder. Write verilog code for the same in gate level with test bench | CO2 | **10M** | |
|  |  | **(OR)** |  |  | |
| 5. | a) | List different types of operators used in Verilog HDL with example. | CO2 | **6M** | |
|  | b) | Write a Verilog code for 4X1 multiplexer using data flow style. | CO2 | **4M** | |
| **Unit – III** | | | | | |
| 6. |  | Write Verilog behavior code for 8:3 encoder **(with and without)** priority with test bench. | CO3 | **10M** | |
|  |  | **(OR)** |  |  | |
| 7. | a) | Write the differences between task and functions. Explain task with example. | CO3 | **5M** | |
|  | b) | Explain different loop statements in Verilog HDL. | CO3 | **5M** | |
| **Unit – IV** | | | | | |
| 8. |  | Explain different types of delay models used in verilog HDL with an example. | CO4 | **10M** | |
|  |  | **(OR)** |  |  | |
| 9. | a) | With an example explain UDP and also list the UDP rules. | CO4 | **5M** | |
|  | b) | How sequential UDP is different from combinational UDP. | CO4 | **5M** | |

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