**18EC503**

**Hall Ticket Number:**

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| **III/IV B.Tech(Regular) DEGREE EXAMINATION** | | | |
| **February, 2021** | **Electronics & Communication Engineering** | | |
| **Fifth Semester** | **Microprocessors & Microcontrollers** | | |
| **Time:** Three Hours | | **Maximum:**50 Marks | |
| *Answer ALL Questions from PART-A.* | | | (1X10 = 10 Marks) |
| *Answer* ***ANY FOUR*** *questions from PART-B.* | | | (4X10=40 Marks) |
| **Part - A** | | | |

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| 1. | Answer all questions | | | (10X1=10 Marks) | | |
|  | a) | | What is the difference between NEG and NOT instruction 8086? | | CO4 |  |
|  | b) | | Name the pipeline stages present in 8086. | | CO1 |  |
|  | c) | | In the process of interfacing an ADC, SOC and EOC represent \_\_\_\_? | | CO3 |  |
|  | d) | | In the process of interfacing stepper motor why should a delay be given after every excitation of a winding? | | CO3 |  |
|  | e) | | How is Near Jump different from Far Jump in 8086? | | CO2 |  |
|  | f) | | Name the two tools, one that’s used to check for programming errors; one that’s used to combine different modules to bring them together. | | CO1 |  |
|  | g) | | With a suitable example demonstrate push instruction in 8086. Write the value of stack pointer before and after push instruction. | | CO1 |  |
|  | h) | | Using 8051bit wise instructionsset 4rth bit(Assume bit ordering 0 to 7) in bit addressable memory location 22H. | | CO2 |  |
|  | i) | | How is a strobed I/O different from single handshake I/O in methods of parallel data transfer? | | CO4 |  |
|  | j) | | Differentiate between SJMP, AJMP instructions of 8051. | | CO4 |  |
|  | | **Part - B** | | | | |
| 2. | a) | | Demonstrate address generation/calculation logic in 8086 Microprocessor using segment with index or pointer registers and explain about segment registers. | | CO1 | 5M |
| b) | | Explain the following addressing modes using suitable example  1) Register Indirect 2) Based Indexed 3) Register Relative 4) Implicit 5) Direct | | CO1 | 5M |
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| 3. | a) | | Demonstrate the following instructions using suitable example.  1) LOOP 2) SCASB 3) LEA 4) DAA 5) IN | | CO1 | 5M |
|  | b) | | Explain the following addressing modes  1) ASSUME 2) ORG 3) EVEN 4) EQU 5) DB | | CO1 | 5M |
|  | |  | | | | |
| 4. | a) | | Assume the values in the address 5000H onwards are 11H, 22H, 33H, 44H; also 5004 and 5005H contains 66H, 88H respectively. Analyze the following program and write the register, memory location address and their contents after each instruction step by step.  MOV SI, 5000H  MOV AX, [SI]  INC SI  INC SI  MOV DX,[SI]  ADD SI, 02H  MOV BX, [SI]  ADD SI, 02H  DIV BX  MOV [SI], AX  INC SI  INC SI  MOV [SI], DX | | CO4 | 4M |
| b) | | Explain the process of steps that take place when an interrupt occurs in 8086. Explain the interrupt vector types of 8086. | | CO1 | 6M |
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| 5. | a) | | Write an 8086 ALP to find number of 1’s and 0’s in an 8-Bit number. | | CO2 | 5M |
|  | b) | | Differentiate between macros and procedures, write basic format of both. | | CO4 | 5M |
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| 6. | a) | | Describe the 8255 CWR format, configure PA as output, PB as input, PCU as input and PCL as input | | CO3 | 3M |
| b) | | Explain the operation of DMA and draw 8237 block diagram. | | CO3 | 7M |
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| 7. | a) | | Explain the block diagramof 8254 timer. | | CO3 | 5M |
|  | b) | | Write an 8051 ALP to generate a saw tooth waveform of increasing ramp. | | CO2 | 5M |
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| 8. | a) | | Write an 8051 ALP to receive data serially and send to port 2based on interrupt. Hint: Can make use of register formats given below. Clearly write baud rate calculation. | | CO2 | 5M |
| b) | | Explain the structure of Timer in 8051.  Calculate the amount of time for which over flow occurs if TH = 45H for timer in mode 2 with 8051’s clock frequency around 22MHz. | | CO1 | 5M |
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| 9. | a) | | Write an 8051 ALP to perform addition of two 16-bit numbers using multibank addition; where one 16-bit number 1 is in bank 1, second 16-bit number 2 is in bank 2 and 16-bit result need to stored in bank 3. | | CO2 | 4M |
|  | b) | | Explain the memory organization of 8051. Demonstrate accessing of memory – internal/external RAM, ROM using respective instructions. | | CO1 | 6M |

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