**Hall Ticket Number: 14EC702**

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| **IV/IV B.Tech (Regular/Supplementary) DEGREE EXAMINATION** | | | |
| **January, 2021** | **Electronics and Communication Engineering** | | |
| **Seventh Semester** | **VLSI Design** | | |
| **Time:** Three Hours | | **Maximum :** 60 Marks | |
| *Answer ALL Questions from PART-A.* | | | (1X12 = 12 Marks) |
| *Answer* ***ANY FOUR*** *questions from PART-B.* | | | (4X12=48 Marks) |
| **Part - A** | | | |

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| 1 | Answer all questions | | (1X12=12 Marks) | | | |
|  | a) | Explain briefly about Depletion mode transistor action. | | |  | |
|  | b) | What is Body effect? | | |  | |
|  | c) | What are the disadvantages of NMOS depletion mode pull up inverter. | | |  | |
|  | d) | What are stick diagrams? | | |  | |
|  | e) | Design Dynamic CMOS 2 input nor gate. | | |  | |
|  | f) | What is Programmable Logic Array? | | |  | |
|  | g) | What is FPGA? | | |  | |
|  | h) | What is Full custom design? | | |  | |
|  | i) | Write difference between PLA,PAL,PLD | | |  | |
|  | j) | Write about limitations on scaling. | | |  | |
|  | k) | Design 2 input EX-OR gate using transmission gates. | | |  | |
|  | l) | What does `timescale 1ns/ 1ps signifies in a Verilog code? | | |  | |
| **Part - B** | | | | | | |
| 2 | a) | Explain Latch up in CMOS circuits and how to avoid this problem? | | | 6M | |
|  | b) | Derive the Drain to Source current equation in NMOSFET. | | | 6M | |
|  | | | | | | |
| 3 | a) | Explain the CMOS-N-Well fabrication process with suitable diagrams. | | | 6M | |
|  | b) | Determine Pull-up to Pull-down ratio for an NMOS inverter driven by another NMOS inverter. | | | 6M | |
|  | | | | | | |
| 4 | a) | What is meant by Sheet resistance RS ? Explain the concept of RS applied to MOS transistors. | | | 6M | |
|  | b) | Design a layout for CMOS logic for Y=(A+B)(C+D) | | | 6M | |
|  | | | | | | |
| 5 | a) | How the following parameters effected when constant electric field scaling model applied.  a)Gate area(Ag) b) Gate capacitance (Cg) c) Channel resistance (Ron) d) Maximum operating frequency (f0) e) Switching energy per gate (Eg) f) Power speed product (Pa) | | | 6M | |
|  | b) | Draw the stick diagram and a mask layout for an 8:1 NMOS inverter circuit. Both the input and output points should be on the poly-silicon layer. | | | 6M | |
|  | | | | | | |
| 6 | a) | Design two-phase clock generator using D flip-flops. | | | 6M | |
|  | b) | Explain the operation of master slave based edge triggered register | | | 6M | |
|  | | | | | | |
| 7 | a) | Realize a Logical function Y = AB + CD using transmission gates. | | | 6M | |
|  | b) | Explain how to optimize power for sequential circuits? | | | 6M | |
|  | | | | | | |
| 8 | a) | Design a four bit ripple carry adder using one bit full adder using Verilog HDL. | | | 6M | |
|  | b) | |  | | --- | | Design a BCD to excess-3 converter using PLA? | |  | | | | 6M | |
|  | | | | | | |
| 9 | a) | Explain about Gate Array Design. | | 6M | |
|  | b) | Discuss typical design flow for designing VLSI IC circuits. | | 6M | |

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**SCHEME**

**Hall Ticket Number: 14EC702**

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| **IV/IV B.Tech (Regular/Supplementary) DEGREE EXAMINATION** | | | |
| **January, 2021** | **Electronics and Communication Engineering** | | |
| **Seventh Semester** | **VLSI Design** | | |
| **Time:** Three Hours | | **Maximum :** 60 Marks | |
| *Answer Question No.1 compulsorily.* | | | (1X12 = 12 Marks) |
| *Answer ONE question from each unit.* | | | (4X12=48 Marks) |

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| 1 | | Answer all questions | | | | | (1X12=12 Marks) | |
|  | | a) | | | Explain briefly about Depletion mode transistor action.   * Explaining Depletion mode transistor action.---1M | | | 1M |
|  | | b) | | | What is Body effect?  -Defining Body effect. -----1M | | | 1M |
|  | | c) | | | What are the disadvantages of NMOS depletion mode pull up inverter.   * Listing out any two disadvantages of NMOS depletion mode pull up inverter –1M | | | 1M |
|  | | d) | | | What are stick diagrams?  ­­-- Defining stick diagram---1M | | | 1M |
|  | | e) | | | Design Dynamic CMOS 2 input nor gate.  --Designing Dynamic CMOS 2 input nor gate.—1M | | | 1M |
|  | | f) | | | What is Programmable Logic Array?  --Writing about programmable Logic array. –1M | | | 1M |
|  | | g) | | | What is FPGA?  --Writing about FPGA---1M | | | 1M |
|  | | h) | | | What is Full custom design?  --Writing about full custom design--1M | | | 1M |
|  | | i) | | | Write difference between PLA,PAL,PLD  --List at least 2 differences between PLA,PAL,PLD --1M | | | 1M |
|  | | j) | | | Write about limitations on scaling.  -List any two limitation on scaling-----1M | | | 1M |
|  | | k) | | | Design 2 input EX-OR gate using transmission gates.  --Designing 2 input EX-OR gate using transmission gates---1M | | | 1M |
|  | | l) | | | What does `timescale 1ns/ 1ps signifies in a Verilog code?  --- Writing about timescale 1ns/ 1ps signifies in a Verilog code---1M | | | 1M |
| **UNIT I** | | | | | | | | |
| 2 | | a) | | | Explain Latch up in CMOS circuits and how to avoid this problem?  --Explaining Latch up in CMOS circuits and how to avoid this problem---6M | | | 6M |
|  | | b) | | | Derive the Drain to Source current equation in NMOSFET.  --Deriving the Drain to Source current equation in NMOSFET with diagram—6M | | | 6M |
| **(OR)** | | | | | | | | |
| 3 | | a) | | | Explain the CMOS-N-Well fabrication process with suitable diagrams.  --Explaining the CMOS-N-Well fabrication process with suitable diagrams. | | | 6M |
|  | | b) | | | Determine Pull-up to Pull-down ratio for an NMOS inverter driven by another NMOS inverter.  ---Determining pull-up to pull-down ratio for an NMOS inverter driven by another NMOS inverter.---.6M | | | 6M |
| **UNIT II** | | | | | | | | |
| 4 | | | a) | | | What is meant by Sheet resistance RS ? Explain the concept of RS applied to MOS transistors.  ---Defining sheet resistance Rs. ---2M  ---Concept of MOS transistor----4M | | 6M |
|  | | | b) | | | Design a layout for CMOS logic for Y=(A+B)(C+D)  --Stick diagram representation.—3M  ---Layout representation---3M | | 6M |
| **(OR)** | | | | | | | | |
| 5 | | a) | | | | How the following parameters effected when constant electric field scaling model applied.  a)Gate area(Ag) b) Gate capacitance (Cg) c) Channel resistance (Ron) d) Maximum operating frequency (f0) e) Switching energy per gate (Eg) f) Power speed product (Pa)  --- Gate area---1M  -- Gate capacitance—1M  ----Channel resistance—1M  ---Maximum operating frequency—1M  ---Switching energy per gate---1M  ---Power speed product.---1M | | 6M |
|  | | b) | | | | Draw the stick diagram and a mask layout for an 8:1 NMOS inverter circuit. Both the input and output points should be on the poly-silicon layer.  ---Stick diagram ---6M | | 6M |
| **UNIT III** | | | | | | | | |
| 6 | a) | | | Design two-phase clock generator using D flip-flops.  ---Designing a two phase clock generator using D flip flop—6M | | | | 6M |
|  | b) | | | Explain the operation of master slave based edge triggered register  ---The operation of master slave based edge triggered register---6M | | | | 6M |
| **(OR)** | | | | | | | | |
| 7 | a) | | | | Realize a Logical function Y = AB + CD using transmission gates.  -- Realizing a Logical function Y = AB + CD using transmission gates.---6M | | | 6M |
|  | b) | | | | Explain how to optimize power for sequential circuits?  -- Optimization power for sequential circuits—6M | | | 6M |
| **UNIT IV** | | | | | | | | |
| 8 | a) | | | | Design a four bit ripple carry adder using one bit full adder using Verilog HDL.  -- Design a four bit ripple carry adder using one bit full adder using Verilog HDL—6M | | | 6M |
|  | b) | | | | |  | | --- | | Design a BCD to excess-3 converter using PLA?  --- Designing a BCD to excess-3 converter using PLA --6M | |  | | | | 6M |
| **(OR)** | | | | | | | | |
| 9 | a) | | | | Explain about Gate Array Design.  --Explaining about Gate Array Design—6M | | | 6M |
|  | b) | | | | Discuss typical design flow for designing VLSI IC circuits.  --Explaining design flow for designing VLSI circuits—6M | | | 6M |