**18EE402**

**Hall Ticket Number:**

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| **II/IV B.Tech (Regular/Supplementary) DEGREE EXAMINATION** | | | |
| **July, 2021** | **Electrical & Electronics Engineering** | | |
| **Fourth Semester** | **Digital Electronics** | | |
| **Time:** Three Hours | | **Maximum:** 50 Marks | |
| *Answer Question number ONE Compulsory* | | | (10X1 = 10 Marks) |
| *Answer* ***ANY ONE***  *questions from each unit* | | | (4X10=40 Marks) |
| **1. Answer all Questions compulsory** | | | **10X1=10Marks** |

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|  | a) | A group of 4 bits is known as \_\_\_\_\_\_\_\_\_\_. | |  |
|  | b) | (44)8 in Hexadecimal system is \_\_\_\_\_\_\_\_\_\_. | |  |
|  | c) | What is Excess 3 code. | |  |
|  | d) | State Distributive law. | |  |
|  | e) | Convert A+AB+ABC into canonical SOP form. | |  |
|  | f) | What is application of comparator? | |  |
|  | g) | What is a Decoder?. | |  |
|  | h) | What do you mean by Latch? | |  |
|  | i) | What is Asynchronous counter? | |  |
|  | j) | What are the applications of D/A converters? | |  |
| **UNIT - I** | | | | |
| 2. | a) | Subtract the following in Excess 3 Code.   1. 79 - 27 ii. 476.7 – 258.9 | | 5M |
|  | b) | What are the different types of logic gates and explain it. | | 5M |
|  |  | **(OR)** | |  |
| 3. | a) | Expand A( + B) ( + B + ) to maxterms and minterms. | | 5M |
|  | b) | Explain TTL -Logic family with neat sketches. | | 5M |
|  |  | **UNIT - II** | |  |
| 4. |  | Simplify the Boolean function using K map in SOP form.  F= ∑m(0,1,2,4,7,8,12,14,15,16,17,18,20,24,28,30,31) | | 10 M |
|  |  | **(OR)** | |  |
| 5. | a) | Design a 2 bit Comparator. | | 5M |
|  | b) | Design a decimal to BCD encoder. | | 5M |
|  |  | **UNIT - III** |  | |
| 6. | a) | Explain JK flip flop with logic diagram and truth table. | | 5M |
|  | b) | Convert T flip flop to D flip flop. | | 5M |
|  |  | **(OR)** | |  |
| 7. | a) | Explain Parallel-In, Parallel-Out shift register. | | 5M |
|  | b) | Design 3 bit synchronous down counter. | | 5M |
|  |  | **UNIT - IV** | |  |
| 8. | a) | Explain Dual slope A/D converter. | | 5M |
|  | b) | Explain Sample and Hold circuit. | | 5M |
|  |  | **(OR)** | |  |
| 9. |  | Explain the classification and characteristics of memories. | | 10M |

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**18EE402(SET-2)**

**Hall Ticket Number:**

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| **II B. Tech (Regular) DEGREE EXAMINATION** | | | |
| **APRIL, 2020** | **EEE** | | |
| **Fourth Semester** | **Digital Electronics** | | |
| **Time:** Three Hours | | **Maximum:** 50 Marks | |
| *Answer Question No.1 compulsorily.* | | | (1X10 = 10 Marks) |
| *Answer ONE question from each unit.* | | | (4X10=40 Marks) |

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| --- | --- | --- | --- | --- | --- |
| 1. | Answer all questions | | | (1X10=10 Marks) | |
|  |  | a. | A group of 4 bits is known as \_\_\_\_\_\_\_\_\_\_. | |  |
|  |  | b. | (44)8 in Hexadecimal system is \_\_\_\_\_\_\_\_\_\_. | |  |
|  |  | c. | What is Excess 3 code. | |  |
|  |  | d. | State Distributive law. | |  |
|  |  | e. | Convert A+AB+ABC into canonical SOP form. | |  |
|  |  | f. | What is application of comparator? | |  |
|  |  | g. | What is a Decoder?. | |  |
|  |  | h. | What do you mean by Latch? | |  |
|  |  | i. | What is Asynchronous counter? | |  |
|  |  | j. | What are the applications of D/A converters? | |  |

**UNIT I**

|  |  |  |
| --- | --- | --- |
| 2.a | Subtract the following in Excess 3 Code.   1. 79 - 27 ii. 476.7 – 258.9 | 5M |
| 2.b | What are the different types of logic gates and explain it. | 5M |

**(OR)**

|  |  |  |
| --- | --- | --- |
| 3.a | Expand A( + B) ( + B + ) to maxterms and minterms. | 5M |
| 3.b | Explain TTL -Logic family with neat sketches. | 5M |

**UNIT II**

|  |  |  |
| --- | --- | --- |
| 4. | Simplify the Boolean function using K map in SOP form.  F= ∑m(0,1,2,4,7,8,12,14,15,16,17,18,20,24,28,30,31) | 10M |
|  |  |  |

**(OR)**

|  |  |  |
| --- | --- | --- |
| 5.a | Design a 2 bit Comparator. | 5M |
| 5.b | Design a decimal to BCD encoder. | 5M |

**UNIT III**

|  |  |  |
| --- | --- | --- |
| 6.a | Explain the master slave JK flip flop. | 5M |
| 6.b | Convert T flip flop to D flip flop. | 5M |

**(OR)**

|  |  |  |
| --- | --- | --- |
| 7.a | Explain Parallel-In, Parallel-Out shift register. | 5M |
| 7.b | Design 3 bit synchronous down counter. | 5M |

**UNIT IV**

|  |  |  |  |
| --- | --- | --- | --- |
| 8.a | Explain Dual slope A/D converter. | 5M | 5M |
| 8.b | Explain Sample and Hold circuit. | 5M | 5M |

**(OR)**

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| 9. | Realize the following function using a PAL with four inputs and 3 wide AND-OR Structure. Also write PAL programming table.  F1(A,B,C,D) = ∑m(6,8,9,12,13,14,15)  F2(A,B,C,D) = ∑m(1,4,5,6,7,10,11,12,13)  F3(A,B,C,D) = ∑m(4,5,6,7,10,11)  F4(A,B,C,D) = ∑m(4,5,6,7,9,10,11,12,13,14,15) | 10M | 5M |