**20EC206**

**Hall Ticket Number:**

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| **I/IV B.Tech (Regular / Supplementary) DEGREE EXAMINATION** | | | | | | | | | |
| **September, 2022** | | | | **Electronics and Communication Engineering** | | | | | |
| **Second Semester** | | | | **Fundamentals of Digital Electronics** | | | | | |
| **Time:** Three Hours | | | | | **Maximum: 7**0 Marks | | | | |
| ***Answer question 1 compulsory.*** | | | | | | **(14X1 = 14 Marks)** | | | |
| ***Answer one question from each unit.*** | | | | | | **(4X14=56 Marks)** | | | |
| 1. | a) | (22B)x =(555)10 then Find the value of ‘x’ | | | | CO1 |  |
|  | b) | Decimal 78 in radix 7(base7) is | | | | CO1 |  |
|  | c) | Convert the binary number 11011101 to gray code. | | | | CO1 |  |
|  | d) | What do you mean by adjacency rule? | | | | CO2 |  |
|  | e) | State De Morgan’s theorems | | | | CO2 |  |
|  | f) | Define the essential prime implicants. | | | | CO2 |  |
|  | g) | Find the complement of the function: A'B(C+D)+B'C'D+AB'C. | | | | CO2 |  |
|  | h) | Compare SOP and POS. | | | | CO3 |  |
|  | i) | Draw half adder circuit. | | | | CO3 |  |
|  | j) | Construct 2X1 MUX using AND gates. | | | | CO4 |  |
|  | k) | How many half adders are needed to construct one full adder? | | | | CO3 |  |
|  | l) | How can a NAND gate be used as an inverter gate? Explain with diagram | | | | CO3 |  |
|  | m) | Define encoder and mention its applications. | | | | CO4 |  |
|  | n) | Implement F(a,b,c)=∑m(2,4,6,7) using decoder. | | | | CO4 |  |
| **UNIT-I** | | | | | | | |
| 2. | a) | Convert the given decimal number 234 to binary, quaternary, octal, hexadecimal and BCD equivalent. | | | | CO1 | 7M |
|  | b) | Perform the following subtraction in binary using 1's and 2's complement method: (677)10 – (899)10 | | | | CO1 | 7M |
|  |  | **(OR)** | | | |  |  |
| 3. | a) | What is a reflected code? Write about reflected codes by giving examples. | | | | CO1 | 7M |
|  | b) | The message below has been coded in the 7 bit Hamming code and transmitted through noisy channel. Decode the message assuming that at most a single error has occurred in each code word 1001001, 0111001, 1110110, and 0011011. | | | | CO1 | 7M |
|  |  | **UNIT-II** | | | |  |  |
| 4. | a) | Reduce the following function using k-map technique F(A,B,C,D)=π M(0,2,3,8,9,12,13,15) | | | | CO2 | 7M |
|  | b) | Determine the canonical product-of-sums representation of the following functions   1. F(A,B,C)= C( (ii) F(A,B,C)= A | | | | CO2 | 7M |
|  |  | **(OR)** | | | |  |  |
| 5. | a) | Simplify the following using Boolean algebra to minimum number of literals   1. (ii) | | | | CO2 | 7M |
|  | b) | Reduce the following expression using tabulation method. F(A,B,C,D,E)=∑m(6,8,13,18,19,25,27,29,31) +d(2,3,11,15,17,24,28). | | | | CO2 | 7M |
|  |  | **UNIT-III** | | | |  |  |
| 6. | a) | Realize a 2 input EX-OR gate using minimum number of 2 input NAND gates | | | | CO3 | 7M |
|  | b) | Without reducing, implement the following expressions in AOI logic and then convert them into NAND logic and NOR logic   1. A + BC + (A + B’C)+ D ( ii) A + B’C + (B + C)’ + B’C’ | | | | CO3 | 7M |
|  |  | **(OR)** | | | |  |  |
| 7. |  | Design half subtractor , half adder and full adder and implement using basic gates. | | | | CO3 | 14M |
|  |  | **UNIT-IV** | | | |  |  |
| 8. | a) | Realize the function f(A,B,C,D) = ∑m (1,3,4,6,7,8,10,13,15) using i) 16:1 MUX ii) 8:1 MUX | | | | CO4 | 7M |
|  | b) | Define decoder. Construct 3x8 decoder using logic gates and truth table. | | | | CO4 | 7M |
|  |  | **(OR)** | | | |  |  |
| 9. | a) | Design and implement a two bit comparator using logic gates. | | | | CO4 | 7M |
|  | b) | Define an encoder. Design octal to binary encoder. | | | | CO4 | 7M |

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