**20EC305**

**Hall Ticket Number:**

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| **II/IV B.Tech (Regular) DEGREE EXAMINATION** | | | |
| **March, 2022** | **Electronics and Communication Engineering** | | |
| **Third Semester** | **Digital Logic Design** | | |
| **Time:** Three Hours | | **Maximum: 7**0 Marks | |
| Answer Question No.1 compulsorily. | | | (1X14 = 14 Marks) |
| Answer ONE question from each unit. | | | (4X14=56 Marks) |

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| 1. | a) | | Draw the RS latch circuit using NAND gates. | CO1 |  |
|  | b) | | Give the characteristic table for T-flip flop. | CO1 |  |
|  | c) | | What is race around condition? | CO1 |  |
|  | d) | | What is state diagram? | CO2 |  |
|  | e) | | How many flip flops are required to design ripple counter which counts 14 clock pulses? | CO2 |  |
|  | f) | | Draw the circuit of twisted ring counter. | CO2 |  |
|  | g) | | What are the different kinds of logic families? | CO3 |  |
|  | h) | | Write the disadvantage of ECL. | CO3 |  |
|  | i) | | Define figure of merit of a logic family. | CO3 |  |
|  | j) | | Write the three different output configurations of TTL gate. | CO3 |  |
|  | k) | | Distinguish ROM and RAM. | CO4 |  |
|  | l) | | Determine the size of ROM required to design 3-bit binary to gray code converter . | CO4 |  |
|  | m) | | Distinguish between static and dynamic RAM. | CO4 |  |
|  | n) | | Expand EPROM and EEPROM. | CO4 |  |
| **Unit - I** | | | | | |
| 2. | a) | Compare sequential and combinational circuits. | | CO1 | 7M |
|  | b) | Convert the SR-flip flop to JK and D flip flop. | | CO1 | 7M |
| **(OR)** | | | | | |
| 3. | a) | Explain the operation of JK flip flop with asynchronous inputs. | | CO1 | 7M |
|  | b) | Convert JK flip flop to SR and T flip flop. | | CO1 | 7M |
| **Unit - II** | | | | | |
| 4. | a) | Derive the state equations and draw the state diagram of sequential circuit with two JK flip-flops A and B and one input x. The circuit is described by the following equations:  JA = x, KA=B’, JB = x, KB=A | | CO2 | 8M |
|  | b) | Design mod-10 ripple counter. | | CO2 | 6M |
| **(OR)** | | | | | |
| 5. | a) | Explain the operation of universal shift register with a neat diagram. | | CO2 | 7M |
|  | b) | Illustrate the design procedure of synchronous sequential circuits. | | CO2 | 7M |
| **Unit - III** | | | | | |
| 6. | a) | Construct and explain the operation of CMOS 2-input NAND gate. | | CO3 | 7M |
|  | b) | Write short notes on TTL tri state logic. | | CO3 | 7M |
| **(OR)** | | | | | |
| 7. | a) | Compare different logic families. | | CO3 | 6M |
|  | b) | Explain the operation of CMOS. i) Inverter ii) NOR gate. | | CO3 | 8M |
| **Unit - IV** | | | | | |
| 8. | a) | Implement the following two Boolean functions with a PLA:  F1(A,B, C) = ∑ (0,1,2,4)  F2(A , B, C) = ∑ (0, 5, 6, 7) | | CO4 | 7M |
|  | b) | Compare PROM, PLA, PAL. | | CO4 | 7M |
| **(OR)** | | | | | |
| 9. | a) | Draw and explain the operation of static RAM. | | CO4 | 6M |
|  | b) | Implement the following Boolean functions using PROM  A(x, y, z) = ∑ (1,2, 4, 6 )  B(x, y, z) = ∑ (0,1,3,6,7)  C(x, y, z) = ∑ (1,2,4,6,7)  D(x, y, z) = ∑ ( 1,2,3, 5, 7) | | CO4 | 8M |

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