**18EC605**

**Hall Ticket Number:**

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| **III/IV B.Tech (Regular/Supplementary) DEGREE EXAMINATION** | | | |
| **June, 2022** | **Electronics & Communication Engineering** | | |
| **Sixth Semester** | **VLSI Design** | | |
| **Time:** Three Hours | | **Maximum: 5**0 Marks | |
| *Answer Question No. 1 Compulsorily.* | | | (10X1 = 10 Marks) |
| *Answer* ***ANY ONE*** *question from each Unit.* | | | (4X10=40 Marks) |

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| 1. | a) | What is Body effect? | CO1 | |  |
|  | b) | What is figure of Merit of MOS transistor? | CO1 | |  |
|  | c) | What are the two types of layout design rules? | CO2 | |  |
|  | d) | What is standard unit of Capacitance? | CO2 | |  |
|  | e) | Give expression for propagation delay of an inverter | CO2 | |  |
|  | f) | Give the basic process of IC Fabrication. | CO1 | |  |
|  | g) | Draw the circuit diagram of a two input AND gate using Pass transistor logic. | CO3 | |  |
|  | h) | Distinguish pass transistor logic and Transmission gate logic. | CO3 | |  |
|  | i) | What is Full custom design? | CO4 | |  |
|  | j) | Write differences between PLA and PAL. | CO4 | |  |
| **Unit - I** | | | | | |
| 2. | a) | Explain an nMOS fabrication process with suitable diagrams. | CO1 | **5M** | |
|  | b) | Derive the expression for Drain to Source current in both Saturated and Non- saturated regions of MOS transistor. | CO1 | **5M** | |
|  |  | **(OR)** |  |  | |
| 3. | a) | Describe N-well process in detail. | CO1 | **5M** | |
|  | b) | Explain Latch up in CMOS circuits and how to avoid this problem? | CO1 | **5M** | |
| **Unit - II** | | | | | |
| 4. | a) | Realize the three-input NOR gate using CMOS technology. | CO2 | **5M** | |
|  | b) | What are the limitations of scaling VLSI circuits and explain them briefly. | CO2 | **5M** | |
|  |  | **(OR)** |  |  | |
| 5. | a) | Discuss briefly the λ – based design rules for layers, wires and transistors. | CO2 | **5M** | |
|  | b) | Realize the two-input NAND gate using CMOS technology. | CO2 | **5M** | |
| **Unit - III** | | | | | |
| 6. | a) | Explain design of ALU Subsystem. | CO3 | **5M** | |
|  | b) | Design a transmission gate based inverter logic and explain? | CO3 | **5M** | |
|  |  | **(OR)** |  |  | |
| 7. | a) | Construct 4:1 Multiplexer using Pass Transistor Logic | CO3 | **5M** | |
|  | b) | How the propagation delay increases in Pass Transistor Logic. Explain with the help of neat diagram and mathematical expressions. | CO3 | **5M** | |
| **Unit - IV** | | | | | |
| 8. | a) | Design a Half-adder logic using programmable logic arrays. | CO4 | **5M** | |
|  | b) | Give VLSI Design Flow. | CO4 | **5M** | |
|  |  | **(OR)** |  |  | |
| 9. | a) | Design a Full Subtractor using PLA. | CO4 | **5M** | |
|  | b) | Explain about Gate Array Design. | CO4 | **5M** | |

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