**Hall Ticket Number: 20EC206**

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I/IV B.Tech (Regular/Supplementary) DEGREE EXAMINATION

August, 2023 Electronics & Communication Engineering

**Second Semester Fundamentals of Digital Electronics**

**Time:** Three Hours **Maximum: 7**0 Marks

*Answer Question* ***No. 1*** *Compulsorily.* (14X1 = 14 Marks)

*Answer* ***ANY ONE*** *questionfrom each* ***Unit.*** (4X14=56Marks)

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| 1. Answer the following. | | | |  |  |  |  |  | (14X1=14Marks) | | | |
|  | a) | | Convert (0.95)10 into ( )2. | | | | | | | L1 | CO1 | 1M |
|  | b) | | Convert (10111011)2 into Gray code. | | | | | | | L1 | CO1 | 1M |
|  | c) | | Find the 1’s complement of 110010101. | | | | | | | L1 | CO1 | 1M |
|  | d) | | Minimum number of bits required to represent (1023)10 is \_\_\_\_\_\_\_\_. | | | | | | | L1 | CO1 | 1M |
|  | e) | | Prove A+A’B = A+B | | | | | | | L2 | CO2 | 1M |
|  | f) | | Define a Minterm. | | | | | | | L1 | CO2 | 1M |
|  | g) | | Write the SOP form of F= πM (0,3,5,7) | | | | | | | L2 | CO2 | 1M |
|  | h) | | Write the output logic expressions for Half Adder. | | | | | | | L1 | CO3 | 1M |
|  | i) | | Define a Combinational Logic Circuit. | | | | | | | L1 | CO3 | 1M |
|  | j) | | Write the expression for NAND gate. | | | | | | | L1 | CO3 | 1M |
|  | k) | | Write the general size of a Decoder. | | | | | | | L1 | CO4 | 1M |
|  | l) | | How many selection lines does a 512 x1 Multiplexer has? | | | | | | | L1 | CO4 | 1M |
|  | m) | | In combinational logic circuits which one is also referred as data selector. | | | | | | | L1 | CO4 | 1M |
|  | n) | | Draw a 2 to 4 Decoder. | | | | | | | L1 | CO4 | 1M |
|  | | Unit – I | | | | | | | | | | |
| 2. | a) | | Perform 10’s complement of the given unsigned numbers  i. 2389 ii. 4069 iii. 1056.074 | | | | | | | L2 | CO1 | 7M |
|  | b) | | Perform 679.6 – 885.9 in BCD code using 9’s complement. | | | | | | | L2 | CO1 | 7M |
|  |  | | (OR) | | | | | | |  |  |  |
| 3. | a) | | Write about various binary codes with relative examples | | | | | | | L1 | CO1 | 8M |
|  | b) | | Write a short notes on Error detecting and correcting codes with examples. | | | | | | | L1 | CO1 | 6M |
|  | | Unit – II | | | | | | | | | | |
| 4. | a) | | State and prove i) Commutative law ii) Associative law iii) Distributive law | | | | | | | L2 | CO2 | 8M |
|  | b) | | Represent the given function in Standard SOP form. F = AB’+ABD+ABD’+ A’C’D’+ A’DC’ | | | | | | | L2 | CO2 | 6M |
|  |  | | **(OR)** | | | | | | |  |  |  |
| 5. | a) | | Minimize the given Boolean Function using K- Maps.  *F**A*,B,C,D  *m*0,7,8,9,10,12) *d*2,5,13 | | | | | | | L3 | CO2 | 7M |
|  | b) | | Simply the following Boolean function using Quine – McCluskey method.  *F* *A*, *B*,*C*, *D*  *m*2,6,8,9,10,11,14,15 | | | | | | | L3 | CO2 | 7M |
|  | | Unit – III | | | | | | | | | | |
| 6. | a) | | Design a Full Adder and also Implement it using Half Adders. | | | | | | | L3 | CO3 | 7M |
|  | b) | | Realize X-OR function using NAND and NOR logics. | | | | | | | L3 | CO3 | 7M |
|  |  | | **(OR)** | | | | | | |  |  |  |
| 7. | a) | | Construct a logic diagram to convert Binary to Gray code conversion. | | | | | | | L3 | CO3 | 8M |
|  | b) | | Explain about ripple carry adder | | | | | | | L2 | CO3 | 6M |
|  | | Unit – IV | | | | | | | | | | |
| 8. | a) | | What is a Decoder. Design a 4 to 16 decoder using 3 to 8 decoders. | | | | | | | L3 | CO4 | 7M |
|  | b) | | Implement the following Boolean expression using 8:1 Multiplexer.  *F* *A*, *B*,*C*, *D*  *m*0,1,3,4,8,9,15) | | | | | | | L3 | CO4 | 7M |
|  |  | | **(OR)** | | | | | | |  |  |  |
| 9. | a) | | Design a 4 bit Magnitude comparator. | | | | | | | L4 | CO4 | 7M |
|  | b) | | Define an Encoder and also design 4 bit priority encoder. | | | | | | | L3 | CO4 | 7M |

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