**20EC305**

**Hall Ticket Number:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| **II/IV B.Tech (Regular\Supplementary) DEGREE EXAMINATION** | | | |
| **January, 2024** | **Electronics and Communication Engineering** | | |
| **Third Semester** | **Digital Logic Design** | | |
| **Time:** Three Hours | | **Maximum:** 70 Marks | |
| ***Answer question 1 compulsory.*** | | | **(14X1 = 14Marks)** |
| ***Answer one question from each unit.*** | | | **(4X14=56 Marks)** |
|  | | |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  |  | CO | BL | M |
| 1 | a) | Show the NAND logic circuit for SR Latch | CO1 | L1 | 1M |
|  | b) | List the asynchronous inputs of a flip flop? | CO1 | L1 | 1M |
|  | c) | What is a flip flop? | CO1 | L1 | 1M |
|  | d) | Distinguish between Boolean equation and state equation. | CO2 | L2 | 1M |
|  | e) | List the contents of state table. | CO2 | L1 | 1M |
|  | f) | How many flip flops are required to design Mod 28 counter? | CO2 | L2 | 1M |
|  | g) | Compare the ring counter and Johnson counter in terms of clock pulse count. | CO2 | L1 | 1M |
|  | h) | Define Fan-In. | CO3 | L1 | 1M |
|  | i) | What is propagation delay? | CO3 | L1 | 1M |
|  | j) | List the outputs of tri-state buffer. | CO3 | L1 | 1M |
|  | k) | Which logic family has low power dissipation? | CO3 | L1 | 1M |
|  | l) | How many address lines are require to access 64K memory locations? | CO4 | L2 | 1M |
|  | m) | Distinguish between static and dynamic RAM. | CO4 | L1 | 1M |
|  | n) | Distinguish between PLA, PAL, PROM. | CO4 | L1 | 1M |
| **Unit-I** | | | | | |
| 2 | a) | Explain the operation of D-flip flop and derive its characteristic equation. | CO1 | L2 | 6M |
|  | b) | Convert the D-flip flop into SR and T flip flop. | CO1 | L3 | 8M |
|  |  | **(OR)** |  |  |  |
| 3 | a) | Derive the characteristic equation for complement output of a JK flip flop | CO1 | L3 | 7M |
|  | b) | Explain how race around condition is eliminated using master slave JK flip flop. | CO1 | L3 | 7M |
| **Unit-II** | | | | | |
| 4 | a) | Design a 3-bit up/down synchronous counter using T-FF’s | CO2 | L4 | 7M |
|  | b) | A sequential circuit with two D flip flops, A and B; two inputs x and y; one output z, is specified by the following state and output equations A(t+1)=x’y+xA; B(t+1)=x’B+xA; z=B; then draw the logic diagram of the circuit, state diagram and list the state table. | CO2 | L4 | 7M |
| **(OR)** | | | | | |
| 5 | a) | Explain the operation of universal shift register with neat sketch. | CO2 | L2 | 7M |
|  | b) | Design a sequential circuit with two JK-flip flops A and B and one input x. When x=0, the state of the circuit remains the same. When x=1, the circuit goes to the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats. | CO2 | L4 | 7M |
| **Unit-III** | | | | | |
| 6 | a) | Compare various logic families. | CO3 | L4 | 7M |
|  | b) | Construct a 2- input CMOS NAND gate and explain its operation. | CO3 | L3 | 7M |
| **(OR)** | | | | | |
| 7 | a) | Explain the operation of TTL NAND gate with Totem pole output | CO3 | L2 | 7M |
|  | b) | Construct 3-input NOR gate using CMOS logic. | CO3 | L3 | 7M |
| **Unit-IV** | | | | | |
| 8 | a) | Compare various PLDs. | CO4 | L2 | 6M |
|  | b) | Design a PAL to implement BCD to Excess-3 code converter | CO4 | L4 | 8M |
| **(OR)** | | | | | |
| 9 | a) | Implement the following Boolean functions using PROM  A(x, y, z)=∑(1,2,4,6); B(x, y, z)= ∑(0,1,6,7); C(x, y, z)= ∑(2,6); D(x, y, z)= ∑(1,2,3,5,7) | CO4 | L4 | 7M |
|  | b) | Design a PLA to implement the following Boolean functions  F1(A,B,C)= ∑(0,1,2,4) ; F2(A,B,C)= ∑(0,5,6,7) | CO4 | L4 | 7M |

