**20EE704/JO**

**Hall Ticket Number:**

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| **IV/IV B.Tech. (Regular) DEGREE EXAMINATION** | | | |
| **January, 2024** | **Electrical & Electronics Engineering** | | |
| **Seventh Semester** | **VLSI Design** | | |
| **Time:** Three Hours | | **Maximum:** 70 Marks | |
| ***Answer question 1 compulsory.*** | | | **(14X1 = 14Marks)** |
| ***Answer one question from each unit.*** | | | **(4X14=56 Marks)** |
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|  |  |  | CO | BL | M |
| 1 | a) | What is body effect? | CO1 | L1 | 1M |
|  | b) | List different steps in IC fabrication. | CO1 | L1 | 1M |
|  | c) | Give the expression for Transconductance. | CO1 | L1 | 1M |
|  | d) | State Moore’s law. | CO1 | L1 | 1M |
|  | e) | What is a stick diagram? | CO2 | L1 | 1M |
|  | f) | Define delay unit. | CO2 | L1 | 1M |
|  | g) | What are the three sources of wiring capacitance? | CO2 | L1 | 1M |
|  | h) | Draw circuit diagram for 3 input nMOS NOR gate. | CO3 | L1 | 1M |
|  | i) | Draw basic structure and symbol of transmission gate. | CO3 | L1 | 1M |
|  | j) | Draw pseudo nMOS NOR gate | CO3 | L1 | 1M |
|  | k) | What is disadvantage of Dynamic CMOS logic circuits? How it can be avoided? | CO3 | L1 | 1M |
|  | l) | What is an ASIC? | CO4 | L1 | 1M |
|  | m) | Define PLA. | CO4 | L1 | 1M |
|  | n) | What are the applications of FPGA? | CO4 | L1 | 1M |
| **Unit-I** | | | | | |
| 2 | a) | Explain an nMOS fabrication process with suitable diagrams. | CO1 | L2 | 7M |
|  | b) | Discuss the operation of bicmos inverter with neat sketch. | CO1 | L2 | 7M |
| **(OR)** | | | | | |
| 3 | a) | Describe the operation of enhancement mode MOS transistor with diagrams | CO1 | L2 | 7M |
|  | b) | Develop the equation for source to drain current in the three regions of operation of a MOS transistor. | CO1 | L3 | 7M |
| **Unit-II** | | | | | |
| 4 | a) | Write the layout design rules for wires and Draw the layout diagram for 2 input CMOS NAND gate. | CO2 | L3 | 10M |
|  | b) | Compute the expression for Sheet resistance. | CO2 | L2 | 4M |
| **(OR)** | | | | | |
| 5 | a) | Derive the expressions for Rise time and Fall time for CMOS inverter? | CO2 | L3 | 7M |
|  | b) | Draw the stick diagrams for NMOS, CMOS inverters. | CO2 | L3 | 7M |
| **Unit-III** | | | | | |
| 6 | a) | Explain switch logic with suitable examples. | CO3 | L2 | 7M |
|  | b) | Illustrate the operation of dynamic CMOS logic circuits and CMOS domino circuits. | CO3 | L3 | 7M |
| **(OR)** | | | | | |
| 7 | a) | Discuss the concept of dynamic register element and the working of NMOS based dynamic shift register with a neat sketch. | CO3 | L2 | 7M |
|  | b) | Describe the nature of parity generator and explain its structured design approach. | CO3 | L3 | 7M |
| **Unit-IV** | | | | | |
| 8 | a) | Explain about Gate Array Design. | CO4 | L2 | 7M |
|  | b) | Discuss the different steps that are taken in process of designing an ASIC | CO4 | L2 | 7M |
| **(OR)** | | | | | |
| 9 | a) | Design a Half-adder logic using PLA | CO4 | L2 | 7M |
|  | b) | Draw FPGA architecture and explain each block briefly. | CO4 | L2 | 7M |

