|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **20EI704/JO**  **Hall Ticket Number:**   |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | | **IV/IV B.Tech (Regular ) DEGREE EXAMINATION** | | | | | **January, 2023** | **Electronics & Instrumentation Engineering** | | | | **Seventh Semester** | **VLSI Design** | | | | **Time:** Three Hours | | **Maximum:7**0 Marks | | | *Answer Question No.1 compulsorily.* | | | (14X1 = 14 Marks) | | *Answer ONE question from each unit.* | | | (4X14=56 Marks) | |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  |  | CO | BL | M |
| 1 | a) | What are the advantages of CMOS process? | CO1 | L1 | 1M |
|  | b) | What is pull down device? | CO1 | L1 | 1M |
|  | c) | List the basic process for IC fabrication | CO1 | L2 | 1M |
|  | d) | What are the uses of Stick diagram? | CO2 | L1 | 1M |
|  | e) | Define sheet resistance. | CO2 | L1 | 1M |
|  | f) | Give the various colour coding used in stick diagram with examples. | CO2 | L2 | 1M |
|  | g) | Define Threshold voltage in CMOS? | CO3 | L1 | 1M |
|  | h) | What are the limitations of scaling? | CO3 | L1 | 1M |
|  | i) | What is the fundamental goal in subsystem design. | CO3 | L1 | 1M |
|  | j) | Write the principle of any one fast multiplier. | CO4 | L1 | 1M |
|  | k) | Draw the 2-input CMOS NAND gate | CO3 | L3 | 1M |
|  | l) | Define synthesis. | CO4 | L1 | 1M |
|  | m) | What you mean by full-custom design? | CO4 | L1 | 1M |
|  | n) | What are bit wise operators in verilog? | CO4 | L1 | 1M |
| **Unit-I** | | | | | |
| 2 | a) | Derive the relationship between drain to source current Ids versus drain to source voltage Vds in a non-saturated and a saturated region. | CO1 | L3 | 7M |
|  | b) | Describe the operation of enhancement mode NMOS transistor using its characteristics. | CO1 | L2 | 7M |
| **(OR)** | | | | | |
| 3 | a) | Realize CMOS inverter and describe its operation. | CO1 | L2 | 7M |
|  | b) | What are the steps involved in the NMOS fabrication? Explain with neat sketches | CO1 | L2 | 7M |
| **Unit-II** | | | | | |
| 4 | a) | What is a stick diagram? Draw the stick diagram and layout for a CMOS inverter. | CO2 | L3 | 7M |
|  | b) | Analyze the sheet resistance concept applied to MOS transistor and inverter. | CO2 | L4 | 7M |
| **(OR)** | | | | | |
| 5 | a) | Explain about the scaling models and scaling factors of MOS circuits. | CO2 | L2 | 7M |
|  | b) | Determine the rise time and fall time of a CMOS inverter. | CO2 | L3 | 7M |
| **Unit-III** | | | | | |
| 6 | a) | Draw the circuit of CMOS transmission gate and explain its operation. | CO3 | L1 | 7M |
|  | b) | Explain the step-by-step procedure to implement 4-bit ALU for AND, OR and XOR operations. | CO3 | L2 | 7M |
| **(OR)** | | | | | |
| 7 | a) | Write about bus arbitration logic for n-line bus in structured design. | CO3 | L2 | 7M |
|  | b) | Design a 4:1 multiplexer with switch logic implementation. | CO3 | L4 | 7M |
| **Unit-IV** | | | | | |
| 8 | a) | Draw and explain the basic architecture of FPGA. | CO4 | L3 | 7M |
|  | b) | Explain the concept of gate delay in VERILOG with example | CO4 | L2 | 7M |
| **(OR)** | | | | | |
| 9 | a) | Describe the steps in ASIC design flow? | CO4 | L2 | 7M |
|  | b) | Write the equations for a full adder in SOP form. Sketch a 3-input, 2-output PLA implementing this logic. | CO4 | L3 | 7M |

