Bapatla Engineering College

(Autonomous)

(Sponsored by Bapatla Education Society)

GBC Rd, Mahatmajipuram, BAPATLA, Andhra Pradesh - 522102

(Approved by AICTE, New Delhi & Affiliated to Acharya Nagarjuna University, Guntur)

www.becbapatla.ac.in

LABORATORY MANUAL

Department of Electrical and Electronics Engineering

Name of the Laboratory: Analog & Digital Electronics

Course Code: 20EEL402

Vision of the Department

The Department of Electrical & Electronics Engineering will provide programs of the highest quality to produce globally competent technocrats who can address challenges of the millennium to achieve sustainable socio-economic development.

Mission of the Department

M1. To provide quality teaching blended with practical skills.

M2. To prepare the students ethically strong and technologically competent in the field of Electrical and Electronics Engineering.

M3. To motivate the faculty and students in the direction of research and focus to fulfill social needs.

Program Educational Objectives (PEOs)

PEO1. To have a strong foundation in the principles of Basic Sciences, Mathematics and Engineering to solve real world problems encountered in modern electrical engineering and pursue higher studies/placement/research.

PEO2. To have an integration of knowledge of various courses to design an innovative and cost-effective product in the broader interests of the organization & society.

PEO3. To have an ability to lead and work in their profession with multidisciplinary approach, cooperative attitude, effective communication and interpersonal skills by participating in team oriented and open-ended activities.

PEO4. To have an ability to enhance career development, adapt to changing professional and societal needs by engaging in lifelong learning.

Program Outcomes:

Engineering graduates will be able to:

PO1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of Electronics and Instrumentation Engineering problems.

PO2. **Problem analysis:** Identify, formulate, research literature and analyze complex engineering problems reaching, substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.

PO3. **Design/development of solutions:** Design solutions for problems in the field of Electronics and Instrumentation Engineering and design system components or

processes that meet the specified needs with appropriate consideration for public health and safety and the cultural, societal and environmental considerations.

PO4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions.

PO5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6. **The Engineer and Society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7. **Environment and Sustainability:** Understand the impact of the Electronics and Instrumentation Engineering solutions in societal and environmental contexts, and demonstrate the need for sustainable development.

PO8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. **Individual and Team work:** Function effectively as an individual and as a member or leader in diverse teams and in multidisciplinary settings.

PO10. **Communication:** Communicate effectively on Electronics and Instrumentation Engineering activities with the engineering community and with the society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations and receive clear instructions.

PO11. **Project management and Finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work as a member and leader in a team to manage projects in a multidisciplinary environment.

PO12. **Life-long Learning:** Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSO's)

PSO1: The Electrical and Electronics Engineering graduates are capable of applying the Knowledge of mathematics and sciences in modern power industry.

PSO2: Analyse and design efficient systems to generate, transmit, distribute and utilize electrical energy to meet social needs using power electronic systems.

PSO3: Electrical Engineers are capable to apply principles of management and economics for providing better services to the society with the technical advancements in renewable and sustainable energy integration.

ANALOG & DIGITAL ELECTRONICS LAB

II B. Tech-V Semester (Code: 20EEL402)

Lectures	0	Tutorial	0	Problem Solving		0	Practical		3	Credits	1.5
Continuous Internal Assessment				30		Semester End Examination (3 Hours)					70

LIST OF EXPERIMENTS

1. Characteristics of PN Junction and Zener diode
2. Characteristics of Transistor in Common Emitter configuration
3. Verification of Transistor Self Bias Circuit
4. Characteristics of Junction Field Effect Transistor
5. Design of voltage shunt feedback amplifier.
6. Design of RC phase shift oscillator.
7. Waveform generation using OP-AMP
8. Realization of Logic Gates using Discrete Components & Universal Building Blocks.
9. Design of Combinational Logic Circuits like half-adder, Full adder, Half-subtractor and Full-subtractor
10. Design of Code converters.
11. Design of 4X1 Multiplexer and 1x4 Demultiplexer.
12. Realization of RS-JK & D flip-flop using logic gates.
13. Design of Synchronous Counter, Mod Counter, Up counter, Down counter and Up/Down counter using Flip Flops.
14. Design and testing of mono stable and astable Multi vibrators using 555 timers.
15. Design a 4-bit R-2R ladder type of digital to analog converter.

Note: Minimum 10 experiments should be conducted.

ANALOG & DIGITAL ELECTRONICS LAB

II B.Tech – IV Semester (Code: 20EEL402)

Lectures	3	Tutorial	0	Problem Solving	0	Practical	0	Credits	3
Continuous Internal Assessment			30	Semester End Examination (3 Hours)					70

Prerequisites: Basic Physics

Course Objectives: To make the students.

CO1: Describe formation of PN junction Diode and applications of diode like Rectifiers, clippers and clampers.

CO2: Explain and design the working concepts of BJT / FET amplifiers.

CO3: Examine the fundamental concepts of differential, multi-stage and operational amplifiers.

CO4: Study about basics of Differential, Multi-stage and operational amplifiers**.**

CO5: Gain knowledge about Linear and Nonlinear applications of Op-amp.

Course Learning Outcomes: After completion of this course, **s**tudents will be able to

CLO1: Demonstrate the fabrication a PN junction diode while delving into its diverse applications including rectification, clipping and clamping.

CLO2: Infer and outline the functioning principles and devise the operational mechanism of BJT/FET Amplifiers.

CLO3: Investigate and analyse a variety of feedback and oscillating circuits.

CLO4: Classify and discuss the core concepts of differential, multi-stage and operational amplifiers in detail.

CLO5: Illustrate the linear and nonlinear applications of operational amplifiers.

1. Characteristics of PN Junction and Zener diode

Aim: To plot the volt ampere characteristics of P-N junction diode and Zener diode.

Components:

S.No	Name	Quantity
1	Diode	1
2	Zener Diode	1
3	Resistors 1Kohm	1

Equipment:

S.No	Name	Range	Quantity
1	Breadboard	-	1
2	Regulated power supply	(0-30)V DC	1
3	Digital Ammeter	(0-200μA)/20mA	1
4	Digital Voltmeter	(0-2)V/20V DC	1
5	Connecting Wires	-	-

Theory:

Donor impurities (pentavalent) are introduced into one-side and acceptor impurities into the other side of a single crystal of an intrinsic semiconductor to form a p-n diode with a Junction called depletion region (this region is depleted off the charge carriers). This Region gives rise to a potential barrier V□ called *Cut- in Voltage.* This is the voltage across the diode at which it starts conducting. It can conduct beyond this Potential.

The P-N junction supports uni-directional current flow. If +ve terminal of the input supply is connected to anode (P-side) and –ve terminal of the input supply is connected to cathode (N- side) then diode is said to be forward biased. In this condition the height of the potential barrier at the junction is lowered by an amount equal to given forward biasing voltage.

Both the holes from p-side and electrons from n-side cross the junction simultaneously and constitute a forward current (*injected minority current* – due to holes crossing the junction and entering N-side of the diode, due to electrons crossing the junction and entering P-side of the diode). Assuming current flowing through the diode to be very large, the diode can be approximated as short-circuited switch.

If –ve terminal of the input supply is connected to anode (p-side) and +ve terminal of the input supply is connected to cathode (n-side) then the diode is said to be reverse biased. In this condition an amount equal to reverse biasing voltage increases the height of the potential barrier at the junction. Both the holes on p-side and electrons on n-side tend to move away

from the junction there by increasing the depleted region.

However the process cannot continue indefinitely, thus a small current called reverse saturation current continues to flow in the diode. This small current is due to thermally generated carriers. Assuming current flowing through the diode to be negligible, the diode can be approximated as an open circuited switch.

A Zener diode is a highly doped semiconductor device specifically designed to function in the reverse direction. It is engineered with a wide range of Zener voltages (Vz), and certain types are even adjustable to achieve variable voltage regulation.

The volt-ampere characteristics of a diode explained by following equation:

$$I = I_0(e^{\frac{V}{\eta V_T}} - 1) \quad \text{---------- (1)}$$

Where

I = current flowing in the diode

I_0=reverse saturation current

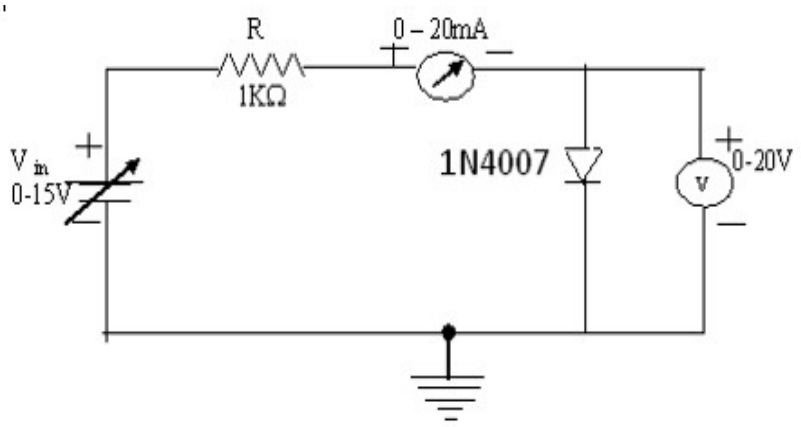
V=voltage applied to the diode

V_T=volt-equivalent of temperature = kT/q=T/11,600 = 26mV (@ room temp).

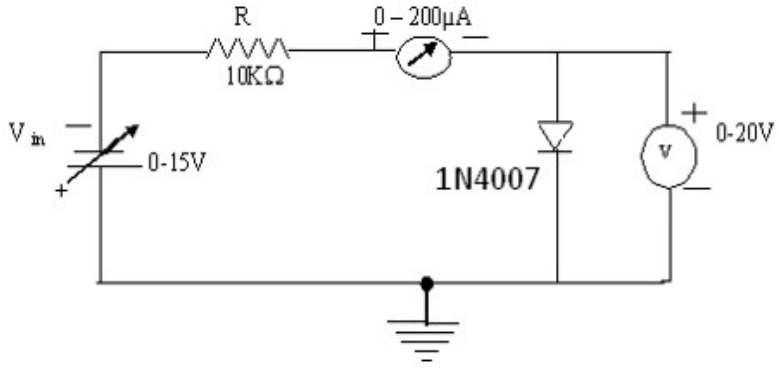
η=1(for Ge) and η=2 (for Si)

Circuit Diagrams:

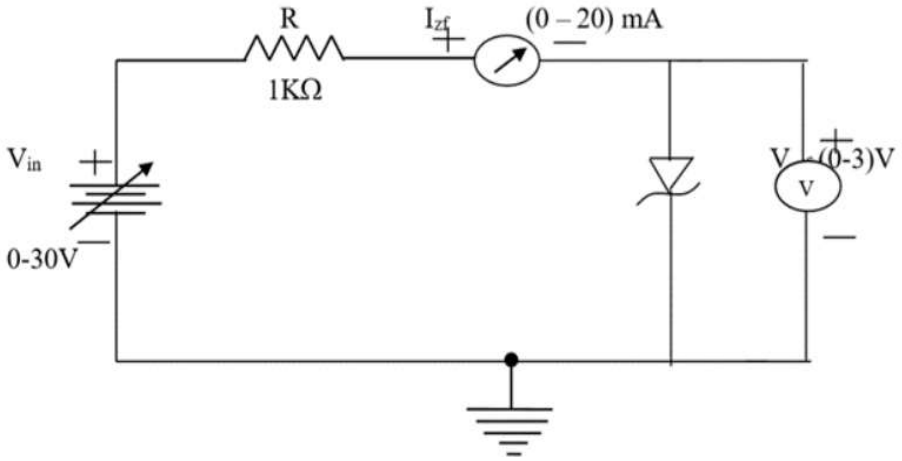
- Circuit diagram of P-N junction Diode in Forward bias:



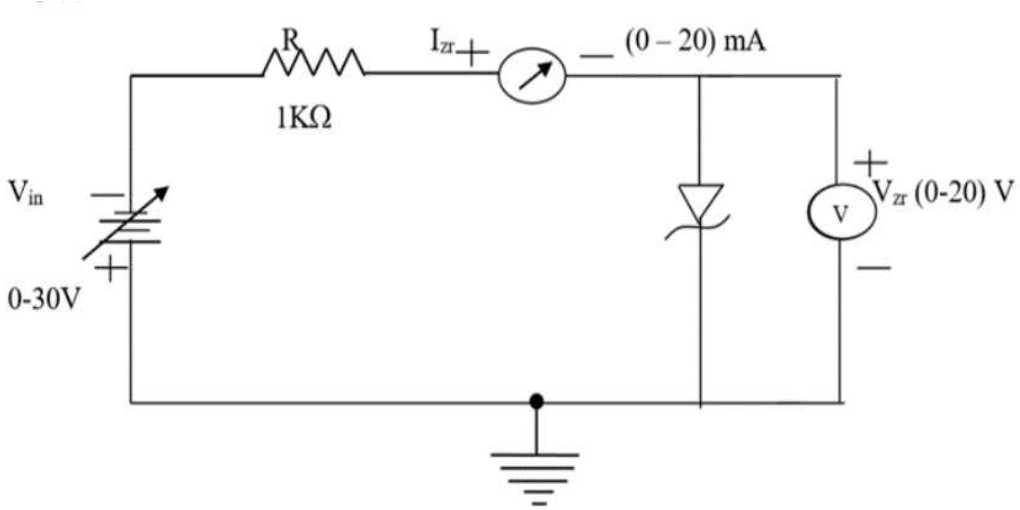
- Circuit diagram of P-N junction Diode in Reverse bias:



- Circuit diagram of Zener Diode in Forward bias:



- Circuit diagram of Zener Diode in Reverse bias:



Procedure:

Forward Bias Condition:

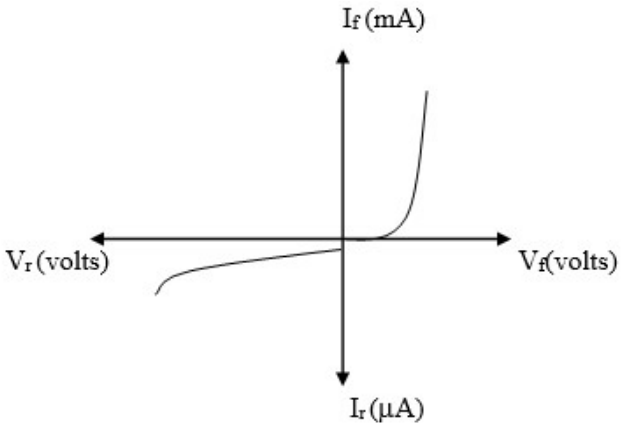
1. Connections are given as per the circuit diagram for P-N junction diode.
2. Vary Forward voltage gradually and note down the corresponding readings of forward current.
3. Tabulate different forward currents obtained for different forward voltages.
4. Draw the graph between forward voltage and forward current.
5. Repeat the above procedure for Zener diode.

Reverse Bias condition:

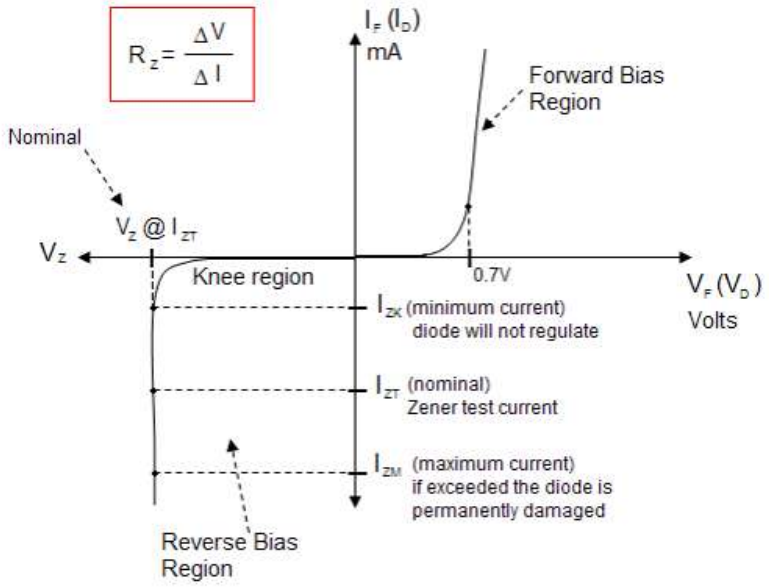
1. Connections are given as per the circuit diagram for P-N junction diode.
2. Vary Forward voltage gradually and note down the corresponding readings of forward current.
3. Tabulate different forward currents obtained for different forward voltages.
4. Draw the graph between forward voltage and forward current.
5. Repeat the above procedure for Zener diode.

Model Graph:

- V-I Characteristics of P-N junction diode:



V-I Characteristics of P-N junction diode:



Tabular form:

P-N junction diode in Forward bias Condition:

S.No	Diode Voltage in Volts	Diode current in mA

P-N junction diode in Forward bias Condition:

S.No	Diode Voltage in Volts	Diode current in µA

Zener diode in Forward bias Condition:

S.No	Zener Voltage in Volts	Diode current in mA

Zener diode Forward bias Condition:

S.No	Zener Voltage in Volts	Diode current in mA

Precautions:

1. While doing the experiment don't exceed the ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

Result:

2. Characteristics of Transistor in Common Emitter configuration

Aim: To study input and output characteristics of transistor in common Emitter configuration of Transistor.

Components:

S.No	Name	Quantity
1	Transistor	1
2	Resistor 100ohm	1
3	Resistor 100Kohm	1

Equipment:

S.No	Name	Range	Quantity
1	Breadboard	-	1
2	Regulated power supply	(0-30)V DC	1
3	Digital Ammeter	(0-200μA)/20mA	1
4	Digital Voltmeter	(0-2)V/20V DC	1
5	Connecting Wires		

Theory:

The configuration in which the emitter is connected between the collector and base is known as a common emitter configuration. The input circuit is connected between emitter and base, and the output circuit is taken from the collector and emitter. Thus, the emitter is common to both the input and the output circuit, and hence the name is the common emitter configuration.

Input Characteristics:

The curve plotted between base current I_B and the base-emitter voltage V_{EB} is called Input characteristics curve. For drawing the input characteristic the reading of base currents is taken through the ammeter on emitter voltage V_{BE} at constant collector - emitter current. The curve for different value of collector - base current. The curve for common base configuration is similar to a forward diode characteristic. The base current I_B increases with the increases in the emitter-base voltage V_{BE}.

Output Characteristics:

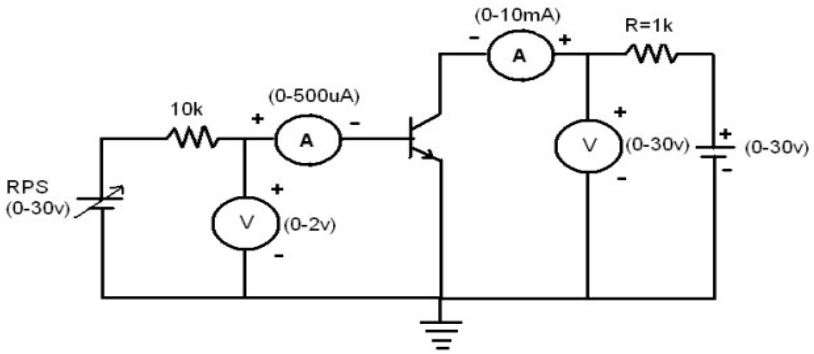
In CE configuration the curve draws between collector current I_C and collector-emitter voltage V_{CE} at a constant base current I_B is called output characteristic. In the active region, the collector current increases slightly as collector-emitter V_{CE} current increases. The slope of the curve is quite more than the output characteristic of CB configuration. The output resistance of

the common base connection is more than that of CE connection. The value of the collector current I_C increases with the increase in V_{CE} at constant voltage I_B, the value β of also increases. When the V_{CE} falls, the I_C also decreases rapidly.

The collector - base junction of the transistor always in forward bias and work saturate. In the saturation region, the collector current becomes independent and free from the input current I_B.

In the active region $I_C = \beta I_B$, a small current I_C is not zero, and it is equal to reverse leakage current I_{CEO}.

Circuit Diagram:



Procedure:

Input Characteristics:

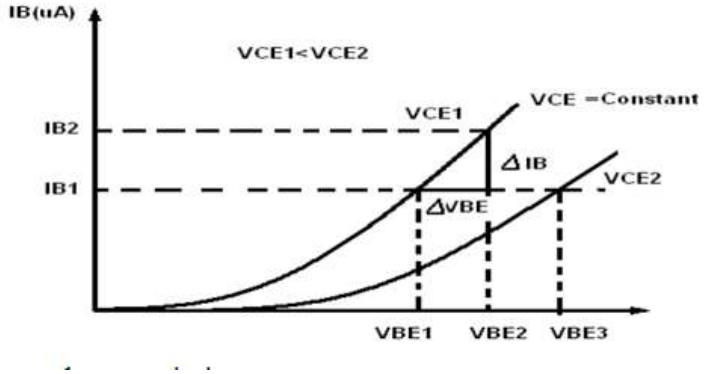
1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 2V and for different values of V_{BE}. Note down the values of IC.
3. Repeat the above step by keeping V_{CE} at 4V.
4. Tabulate all the readings.
5. Plot the graph between V_{BE} and I_B for constant V_{CE}

Output Characteristics:

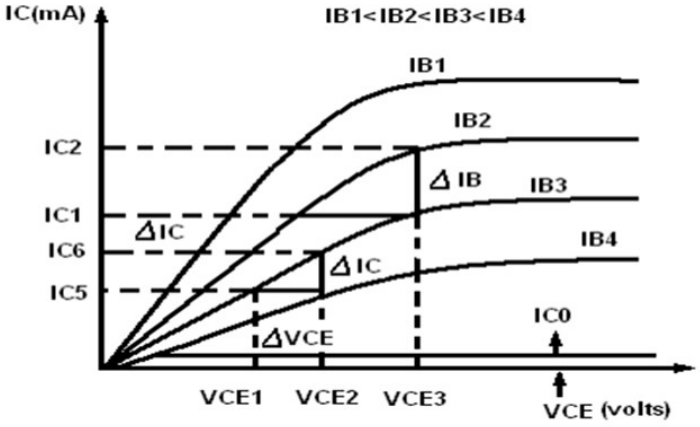
1. Connect the circuit as per the circuit diagram
2. For plotting the output characteristics the input current I_B is kept constant at 10μA and for different values of V_{CE} note down the values of IC.
3. Repeat the above step by keeping IB at 75 μA 100 μA
4. Tabulate the all the readings
5. Plot the graph between V_{CE} and I_C for constant I_B.

Model Graphs:

Input Characteristics:



Output characteristics:



Tabular form:

Input Characteristics:

VCE =2V		VCE=4V	
VBE in volts	**IB in µA**	**VBE in volts**	**IB in µA**

Output characteristics:

IB =50µA		IB =100µA	
VCE in volts	**IC in mA**	**VCE in volts**	**IC in mA**

Precautions:

1. While doing the experiment don't exceed the ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

Result:

3. Verification of Transistor Self Bias Circuit

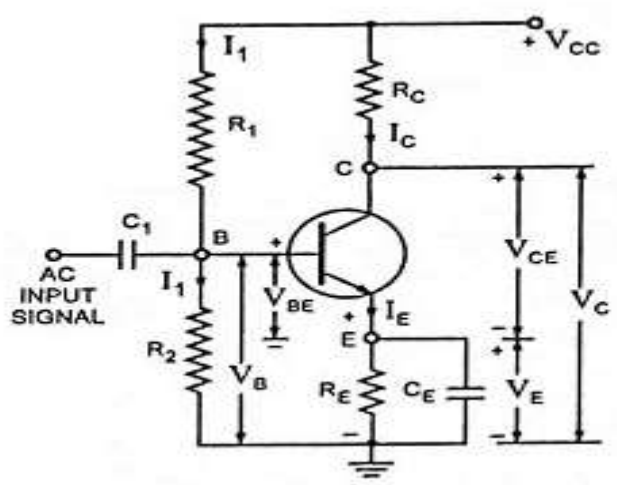
Aim: To design a self-bias circuit and observe stability by changing the value of transistor.

Components:

S.No	Name	Quantity
1	Transistor	4
2	Resistor	4
3	RPS (0-30)v	1
	Connecting Wires	

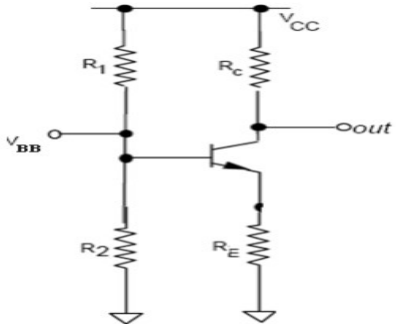
Theory:

This is the most used biasing arrangement. The arrangement of Self Bias or Potential Divider Bias Circuit. The name voltage divider is derived because the voltage divider is formed by the resistors R_1 and R_2 across V_{CC}. The emitter resistor R_E provides stabilization. The resistor R_E causes a voltage drop in a direction so as to reverse bias the emitter junction. Since the emitter-base junction is to be forward biased, the base voltage is obtained from supply V_{CC} through $R_1 - R_2$ network.



For forward biasing the emitter-base junction R_1 and R_2 are so adjusted that the base terminal becomes more positive than emitter. The net forward bias across the emitter-base junction, V_{BE} is equal to V_B minus dc voltage drop across R_E. The dc bias circuit is independent of transistor current gain factor β. In case of amplifiers, to avoid the loss of ac signal (because of feedback caused by R_E) a capacitor of large capacitance is connected across R_E. The capacitor offers a very small reactance to the ac signal and so it passes through the capacitor.

Circuit Diagram:



Calculations:

Given V_{CC}=10V, R_E=220 ohm I_C=4mA V_{CE}=6V V_{BE}=0.6V h_{fe}=229

$R_C=(V_{CC}-V_{CE})/I_C$

$I_B=I_C/\beta$

$R_B=\beta*R_E/10$

$V_{BB}=I_B*R_B+V_{BE}+(I_B+I_C)R_E$

$R_1=(V_{CC}/V_{BB})*R_B$

$R_2=R_B/(1-V_{BB}/V_{CC})$

Procedure:

1. Assemble the circuit on a bread board with designed values of resistors and transistor.
2. Apply Vcc and measure V_{CE}, V_{BE} and V_{EE} and record the readings in table.
3. Without changing the values of biasing resistors, change the transistor with other β values and repeat the above steps and record the readings in the table.

Tabular form:

S.No	β Value	V_{CE}	V_{BE}	V_{EE}	$I_C=(V_{CC}-V_{CE})/R_C$	$I_E=V_{EE}/R_E$
1						
2						
3						

Precautions:

1. The supply voltage should not exceed the rating of the transistor.
2. Connections must be tight.

Result:

4. Characteristics of Junction Field Effect Transistor

Aim: To study Drain and transfer characteristics of transistor of Junction Field Effect Transistor.

Components:

S.No	Name	Quantity
1	FET BFW10	1
2	Resistor 220 ohm	1

Equipment:

S.No	Name	Range	Quantity
1	Breadboard	-	1
2	Regulated power supply	(0-30)V DC	1
3	Digital Ammeter	(0-200μA)/20mA	1
4	Digital Voltmeter	(0-2)V/20V DC	1
5	Connecting Wires	As required	

Theory:

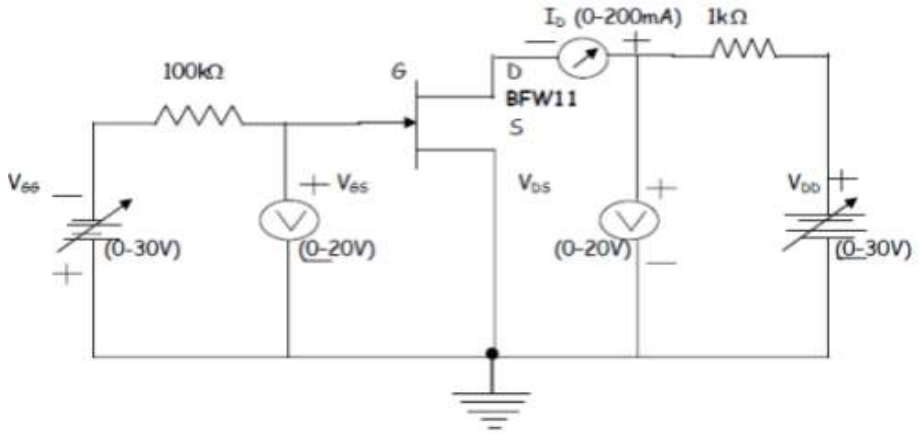
JFET or Junction Field Effect Transistor is one of the simplest types of field-effect transistor. Contrary to the Bipolar Junction Transistor, JFETs are voltage-controlled devices. In JFET, the current flow is due to the majority charge carriers. However, in BJTs, the current flow is due to both minority and majority charge carriers. Since only the majority charge carriers are responsible for the current flow, JFETs are unidirectional.

In the absence of external bias: In this case, as there is no voltage between gate and source terminal, thus, the drain current will flow from drain terminal to source terminal. The channel width is more as the width of depletion layer will not vary initially because there is no external reverse biasing. This allows a large magnitude of current to flow through the channel. In this case, the N-type channel will simply behave as resistance region. The flow of current from drain to source will create the voltage drop between gate and source. This will eventually result in reverse biasing of the gate-source terminal. The reverse biasing will be more towards drain region that source region.

With external bias: When the external bias is applied to the gate-source terminal, the gate-source terminal becomes reversed bias externally. Obviously, if we are supplying an external voltage, then we can achieve the pinch-off point quite early as compared to the circuit which is not biased.

Transfer Characteristics: The transfer characteristics can be determined by observing different values of drain current with variation in gate-source voltage provided that the drain-source voltage should be constant. The transfer characteristics are just opposite to drain characteristics. One just needs to remember the concept that in drain characteristics we are keeping the gate-source voltage constant and determining the values of drain current at different values of drain-source voltage while in transfer characteristics we are keeping the value of drain-source voltage constant.

Circuit Diagram:



Procedure:

Drain characteristics:

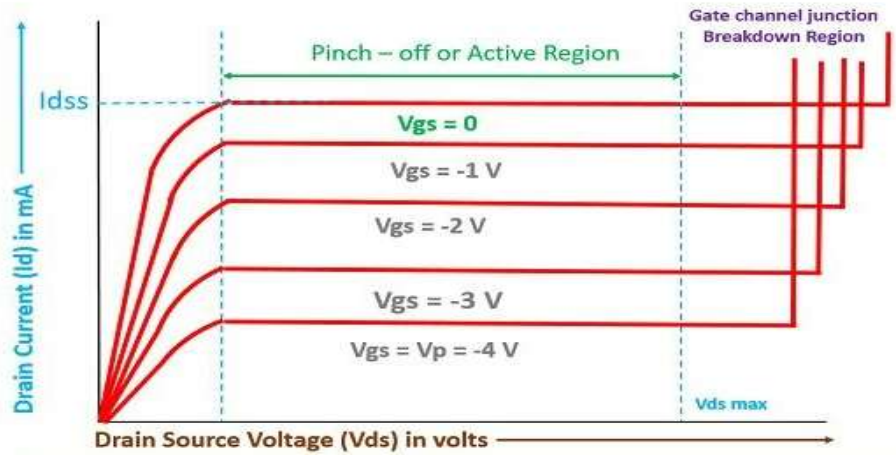
1. Connect the circuit as per the circuit diagram.
2. Keeping VGS as -1V, vary VDS gradually.
3. Note down the drain current Id for each step.
4. Now set VGS to -2V and repeat the above steps and record the readings in the table.
5. Plot the drain characteristics from tabulated readings.

Transfer Characteristics:

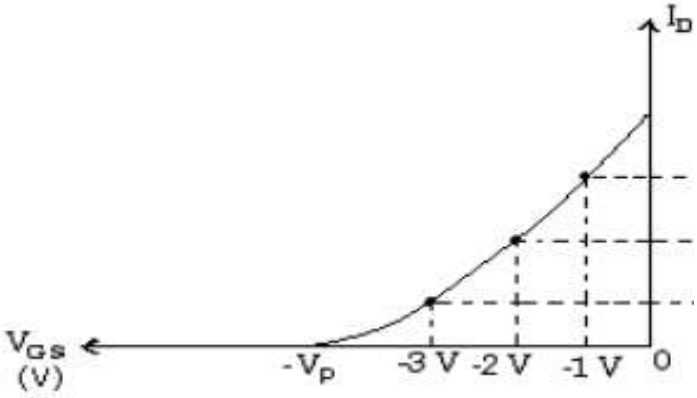
1. Connect the circuit as per the circuit diagram.
2. Keeping VDS as 2V, vary VGS gradually.
3. Note down the drain current Id for each step.
4. Now set VDS as 4Vand repeat the above steps and record the readings in the table.
5. Plot the transfer characteristics from tabulated readings.

Model Graph:

Drain Characteristics:



Transfer Characteristics:



Tabular Form:

Drain Characteristics:

VGS = -1V		VGS = -2V	
VDS in volts	**ID in mA**	**VDS in volts**	**ID in mA**

Transfer Characteristics:

VDS=2V		VDS=4V	
VGS in volts	**ID in mA**	**VGS in volts**	**ID in mA**

Precautions:

1. While doing the experiment don't exceed the ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

Result:

5. Design of voltage shunt feedback amplifier

Aim: To design and draw the frequency response of voltage shunt feedback amplifier with and without feedback.

Components:

S.No.	Name of the item	Quantity
1	Transistor	1
2	Resistor	
3	Capacitor	
4	CRO	1
5	Function Generator	1
6	Bread board	1
7	Connecting Wires	As Required

Theory:

Feedback is a method in which a portion of the output returned to the input to modify the characteristics of the device. Feedback can apply to transistor amplifier circuits to modify their performance characteristics such as gain, bandwidth, input, and output impedance etc. Feedback is of two types:

1. Positive Feedback 2. Negative Feedback

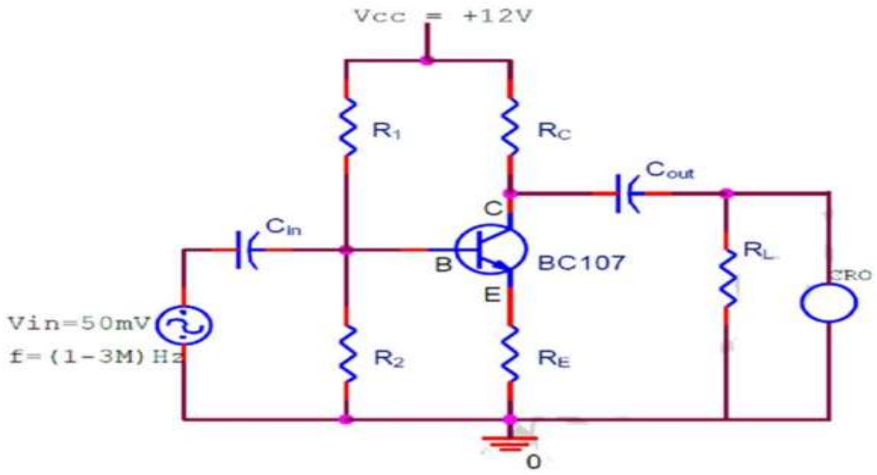
In positive feedback, the feedback energy (voltage or currents), is in phase with the input signal and thus aids it Positive feedback increases gain of the amplifier also increases distortion, noise, and instability. In negative feedback, the feedback energy (voltage or current), is out of phase with the input signal and thus opposes it. Negative feedback reduces gain of the amplifier. It also reduces distortion, noise, and instability. This feedback increases bandwidth and improves input and output impedances. Due to these advantages, the negative feedback is frequently used in amplifiers. A feedback amplifier generally consists of two parts. They are the amplifier and the feedback circuit. The feedback circuit usually consists of resistors.

In voltage shunt feedback amplifier, the feedback signal voltage is given to the base of the transistor in shunt through the base resistor RB. This shunt connection tends to decrease the input resistance and the voltage feedback tends to decrease the output resistance. In the circuit RB appears directly across the input base terminal and output collector terminal. A part of output is feedback to input through RB and increase in IC decreases IB. Thus, negative feedback exists in the circuit. So, this circuit is also called voltage feedback bias circuit. This feedback amplifier is known a transresistance amplifier. It amplifies the input current to required voltage levels. The feedback path consists of a resistor and a capacitor.

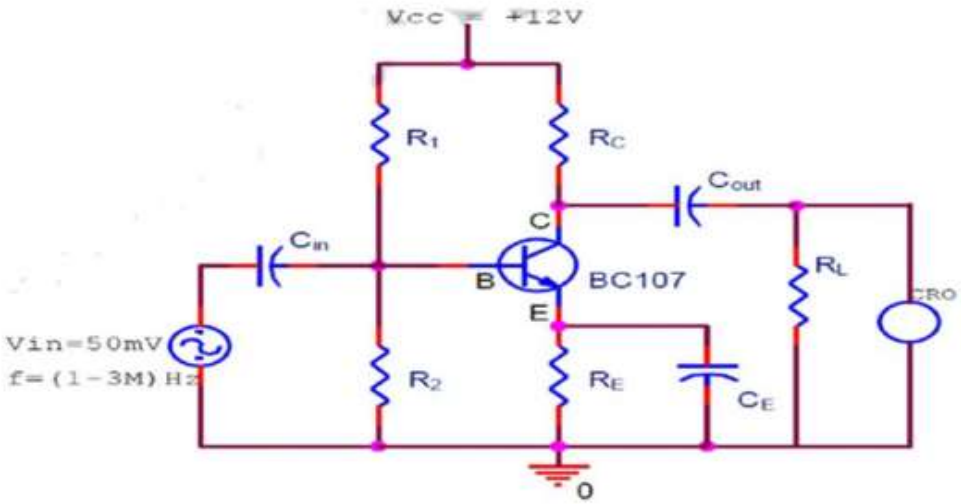
An important piece of information that can be obtained from a frequency response curve is the bandwidth of the amplifier. This refers to the 'band' of frequencies for which the amplifier has a useful gain. Outside this useful band, the gain of the amplifier is insufficient compared with the gain at the centre of the bandwidth. The bandwidth specified for the voltage amplifiers is the range of frequencies for which the amplifiers gain is greater than 0.707 of the maximum gain. Alternatively, decibels are used to indicate gain, the ratio of output to input voltage. The useful bandwidth would be described as extending to those frequencies at which the gain is -3db down compared to the gain at the mid-band frequency.

Circuit Diagram:

Without Feedback:



With Feedback:



Procedure:

1. Connect the circuit as per the circuit diagram.
2. Keeping the input voltage constant, vary the frequency from 50Hz to 3MHz in regular steps and note down the corresponding output voltage.
3. Plot the graph: Gain (dB) Vs Frequency
4. Calculate the bandwidth from the graph. 5. Calculate the input and output impedance.
5. Remove Emitter Capacitance and follow the same procedures.

Tabular Form:

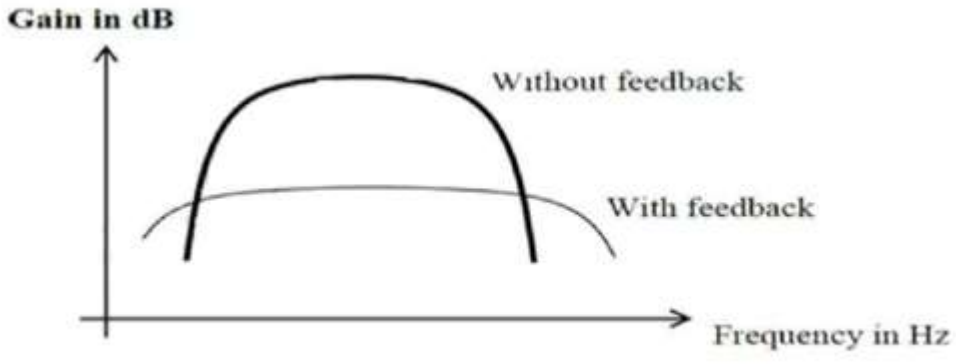
Without Feedback:

Frequency in Hz	Output Voltage (Vo)	Input Voltage (Vi)	Gain=$\frac{V_o}{V_i}$	Gain in db

With Feedback:

Frequency in Hz	Output Voltage (Vo)	Input Voltage (Vi)	Gain=$\frac{V_o}{V_i}$	Gain in db

Model Graph:



Precautions:

1. Connections should be tight.

Result: Frequency response of Voltage shunt feedback amplifier is drawn.

6. Design of RC phase shift oscillator

Aim: To calculate the frequency of the RC phase shift oscillator

Components:

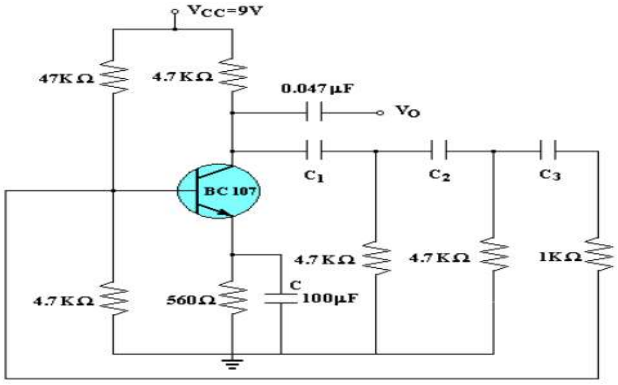
S.No	Name of the component	Quantity
1	Resistor 10Kohm	4
2	Resistor 15Kohm, 33Kohm, 1Kohm, 2.2Kohm	Each 1
3	Capacitor 10μF	1
4	Capacitor 100μF	1
5	RPS	1
6	Transistor	1
7	Bread Board	1
8	Connecting wires	As Required

Theory:

The basic RC Oscillator which is also known as a Phase-shift Oscillator, produces a sine wave output signal using regenerative feedback obtained from the resistor-capacitor combination. This regenerative feedback from the RC network is due to the ability of the capacitor to store an electric charge, (similar to the LC tank circuit). This resistor-capacitor feedback network can be connected as shown above to produce a leading phase shift (phase advance network) or interchanged to produce a lagging phase shift (phase retard network) the outcome is still the same as the sine wave oscillations only occur at the frequency at which the overall phase-shift is 360 . By varying one or more of the resistors or capacitors in the phase-shift network, the frequency can be varied and generally this is done by keeping the resistors the same and using a 3- ganged variable capacitor. If all the resistors, R and the capacitors, C in the phase shift network are equal in value, then the frequency of oscillations produced by the RC oscillator is given as:

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

Circuit Diagram:



Procedure:

1. Make the connection as per the circuit diagram as shown above.
2. Observe the output signal and note down the output amplitude and time period (T).
3. Calculate the frequency of oscillations theoretically and verify it practically (f=1/T).

Theoretical Calculations:

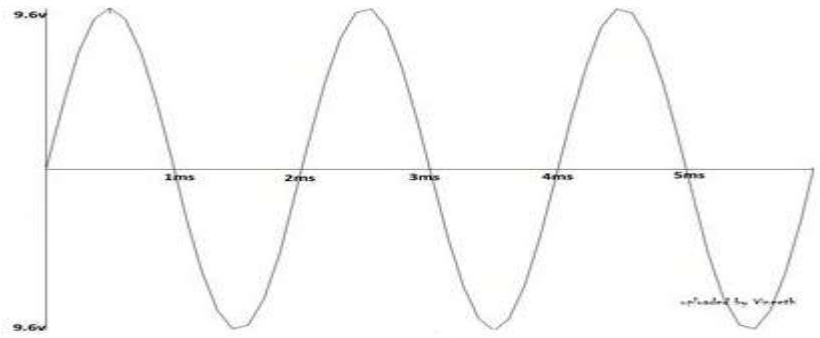
f (practical) = 1/T Hz.

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

Tabular Form:

S.No	Theoretical Frequency	Practical Frequency

Model Graph:



Precautions:

1. Connections should be tight
2. Connect designed values of components in the circuits

Result:

7. Waveform generation using OP-AMP

Aim: To generate Square and triangular waveforms using op-amp.

Components:

S,No.	Name of the Item	Quantity
1	IC 741	2
2	RPS	1
3	Resisors	
4	Capacitors	
5	CRO	1
6	Bread board	1
7	Connecting Wires	As required

Theory:

Square wave Generator:

The basic square wave oscillator is based on the charging and discharging of a capacitor. Op-amps inverting input is the capacitor voltage and the non inverting input is a portion of the output fed back through resistors. When the circuit is first turned on, the capacitor is uncharged, and thus the inverting input is at 0V. This makes the output a positive maximum, and the capacitor begins to charge towards voltage at V_O through resistor R. When the capacitor voltage reaches a value equal to the feedback voltage (V_f) on the non-inverting input, the op-amp switches to the maximum negative state. At this point, the capacitor begins to discharge from $+V_f$ towards $-V_f$. When the capacitor voltage reaches $-V_f$, the op-amp switches back to the maximum positive state. This action repeats and a square wave output voltage is obtained. Expression for period is

$$T = 2RCln\frac{1+\beta}{1-\beta} \; where \; \beta = \frac{R_2}{R_1+R_2}$$

$$The \; frequency \; of \; Oscillations \; if \; R_1 = R_2 \; are \; f = \frac{1}{2RCln3}$$

Triangular-wave oscillator:

This circuit (figure 2) uses two operational amplifiers. Op-amp A_1 functions as a comparator and the op-amp A_2 as an integrator. Comparator compares the voltage at point P continuously with respect to the voltage at the inverting input; which as at ground potential. When the voltage at P goes slightly below zero, the output of A1 will switch to negative saturation. Suppose the output of A_1 is at positive saturation $+V_{sat}$. Since this voltage is the input of the integrator, the output of A_2 will be a negative going ramp. Thus, one end of the voltage divider R_1-R_2 is at $+V_{sat}$ and the other at the negative going ramp. At time $t = t_1$, when

the negative going ramp attains value of $-V_{ramp}$ the effective voltage at point P becomes slightly less than 0 V. This switches output of A_1 from positive saturation to negative saturation level $-V_{sat}$. During the time when the output of A_1 is at $-V_{sat}$, the output of A_2 increases in positive direction. At the instant $t = t_2$, the voltage at point P becomes just above 0 V, thereby switching the output of A1 from $-V_{sat}$ to $+V_{sat}$. The cycle repeats and generates a triangular waveform.

At $t = t_1$ $\quad \dfrac{-V_{ramp}}{R_2} = -\dfrac{+V_{sat}}{R_1}$ $\quad$ ie. $\quad -V_{ramp} = -\dfrac{R_2}{R_1}(+V_{sat})$

Similarly, at $t = t_2$ $\quad +V_{ramp} = -\dfrac{R_2}{R_1}(-V_{sat})$

The peak to peak output of the triangular wave is

$$V_{O(pp)} = +V_{ramp} - (-V_{ramp}) = 2\frac{R_2}{R_1}V_{sat}$$

During the period 0-t_1, The integrator functions as below.

$$V_{O(pp)} = \frac{1}{RC}\int_0^{T/2}(-V_{sat})\,dt = \left(\frac{V_{sat}}{RC}\right)\left(\frac{T}{2}\right)$$

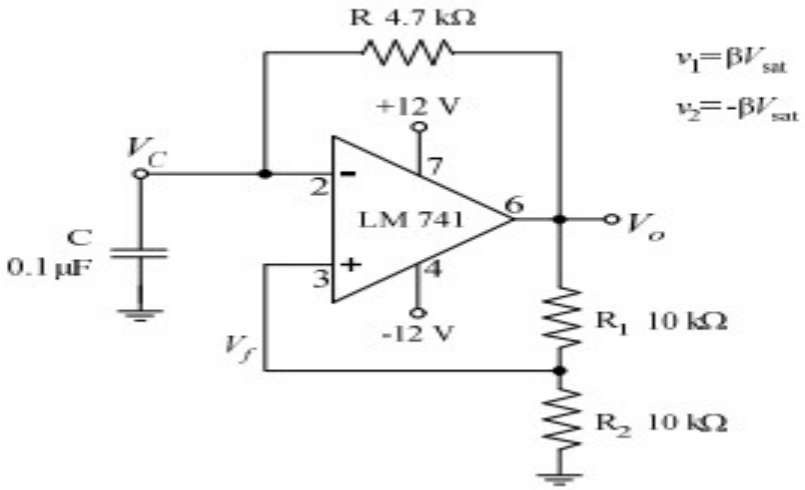
Then, $\quad T = 2RC\left(\dfrac{V_{O(pp)}}{V_{sat}}\right)$

Substituting for $V_{O(pp)}$ $\quad T = \dfrac{4RCR_2}{R_1}$

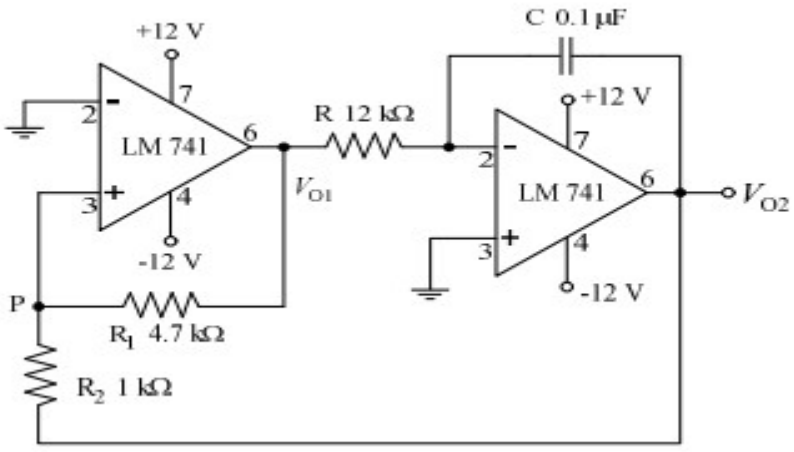
Then, frequency of oscillation, $f = \dfrac{R_1}{4RCR_2}$

Circuit Diagram:

Square wave Generator:



Triangular wave generator:



Tabular form:

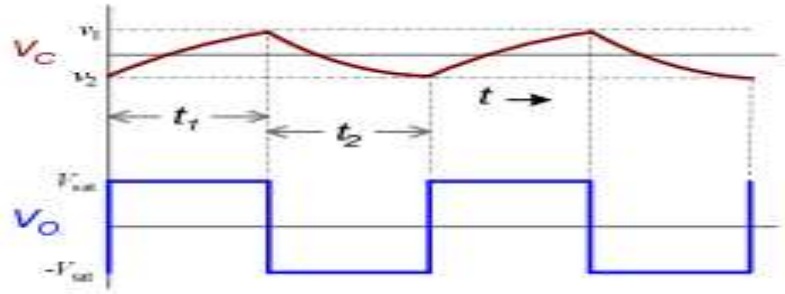
Square wave Generator:

S.No.	Practical Frequency	Theoretical Frequency

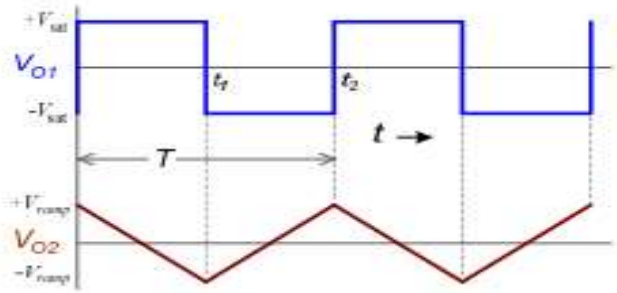
Triangular wave generator:

S.No.	Practical Frequency	Theoretical Frequency

Model graph:
Square wave Generator:



Triangular wave generator:



Precautions:
1. Connections should be tight.

Result: Square and Triangular waveforms are drawn using op-amp.

8. Realization of Gates Using Discrete Components Universal Building Blocks (NAND Only)

Aim: To construct logic gates **OR, AND, NOT, NOR, NAND** gates using discrete components, universal building blocks and verify their truth tables.

Components:

S.No	Name of the item	Quantity
1	Resistors 10 K ohm	1
2	Resistors 1 K ohm	1
3	Transistor	1
4	Diodes	2
5	Electronic circuit designer	
6	Connecting wires	As Required

Theory:

Logic gates:

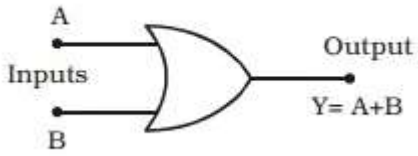
Circuits which are used to process digital signals are called logic gates. They are binary in nature. Gate is a digital circuit with one or more inputs but with only one output. The output appears only for certain combination of input logic levels. Logic gates are the basic building blocks from which most of the digital systems are built up. The numbers 0 and 1 represent the two possible states of a logic circuit. The two states can also be referred to as 'ON and OFF' or 'HIGH and LOW' or 'TRUE and FALSE'.

Basic logic gates using discrete components:

The basic elements that make up a digital system are 'OR', 'AND' and 'NOT' gates. These three gates are called basic logic gates. All the possible inputs and outputs of a logic circuit are represented in a table called TRUTH TABLE. The function of the basic gates are explained below with circuits and truth tables.

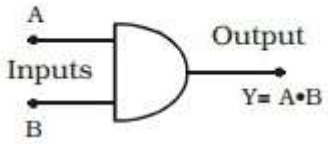
OR Gate:

An OR gate has two or more inputs but only one output. It is known as OR gate, because the output is high if any one or all the inputs are high. The logic symbol of a two input OR gate is shown below. The Boolean expression to represent OR gate is given by Y= A+B (+ symbol should be read as OR)



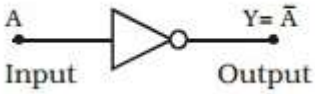
AND gate:

An AND gate has two or more inputs but only one output. It is known as AND gate because the output is high only when all the inputs are high. The logic symbol of a two input AND gate is shown below. Y = A·B (· should be read as AND)



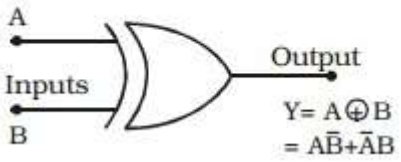
NOT gate (Inverter)

The NOT gate is a gate with only one input and one output. It is so called, because its output is complement to the input. It is also known as inverter. The Boolean expression to represent NOT operation is Y = $\bar{A}$.



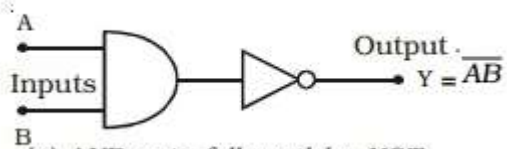
Exclusive OR gate (EXOR gate)

The logic symbol for exclusive OR (EXOR) gate is shown below. The Boolean expression to represent EXOR operation is Y = A ⊕ B. EXOR gate has an output 1, only when the inputs are complement to each other.

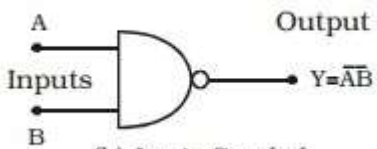


NAND gate

This is a NOT-AND gate. It can be obtained by connecting a NOT gate at the output of an AND gate. NAND gate function is reverse of AND gate function. A NAND gate will have an output, only if both inputs are not 1. In other words, it gives an output 1, if either A or B or both are 0.



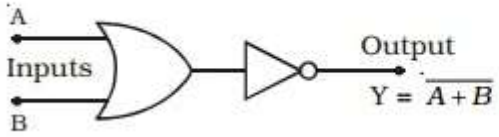
(a) AND gate followed by NOT

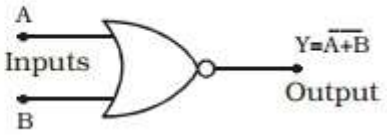


(b) Logic Symbol

NOR gate

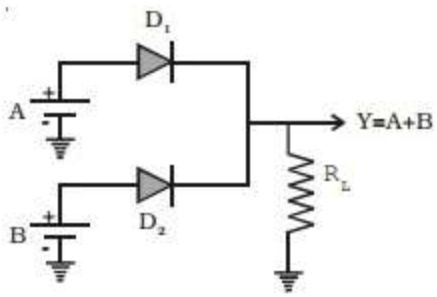
This is a NOT-OR gate. It can be made out of an OR gate by connecting an inverter at its output. The NOR gate function is the reverse of OR gate function. A NOR gate will have an output, only when all inputs are 0. In a NOR gate, output is high, only when all inputs are low.





Circuit Diagram: Discrete Components

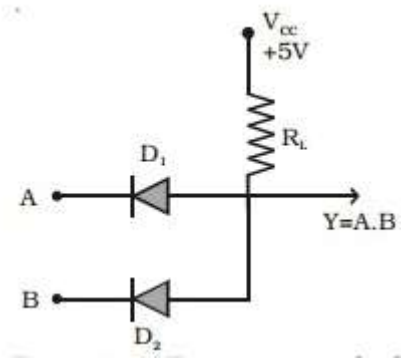
OR Gate:



Truth Table

A	B	Y=(A+B)
0	0	0
0	1	1
1	0	1
1	1	1

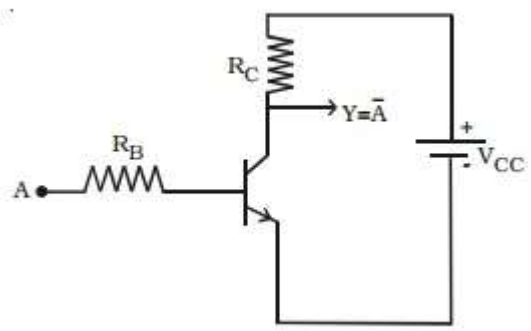
AND Gate:



Truth Table

A	B	Y=(A.B)
0	0	0
0	1	0
1	0	0
1	1	1

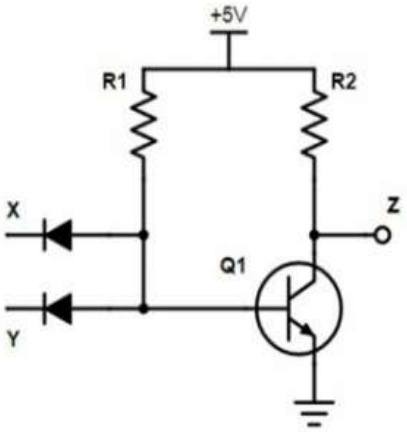
NOT Gate:



Truth Table

A	Y
0	1
1	0

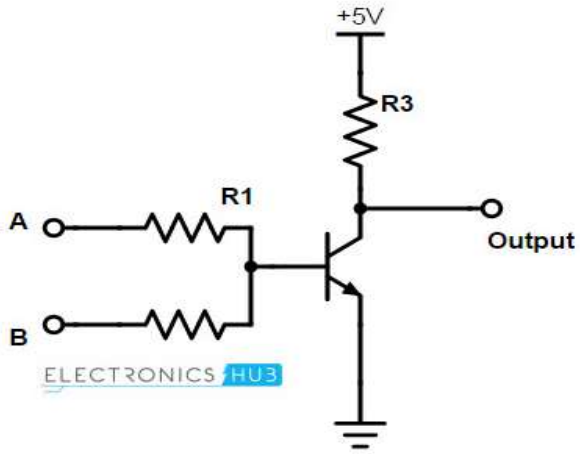
NAND Gate:



Truth Table

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate:

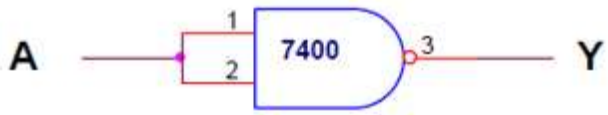


Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Circuit Diagram: Universal Building Blocks

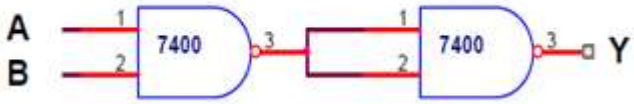
NOT Gate:



Truth Table

A	Y
0	1
1	0

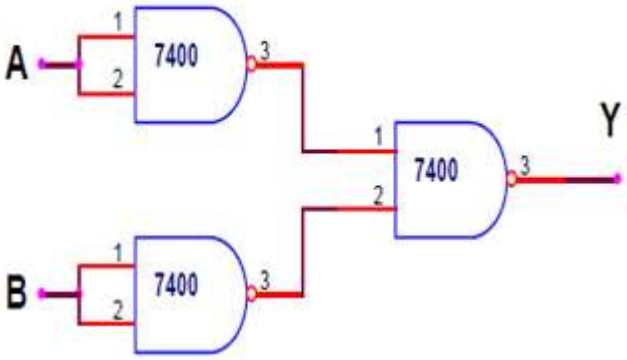
AND Gate:



Truth Table

A	B	Y=(A.B)
0	0	0
0	1	0
1	0	0
1	1	1

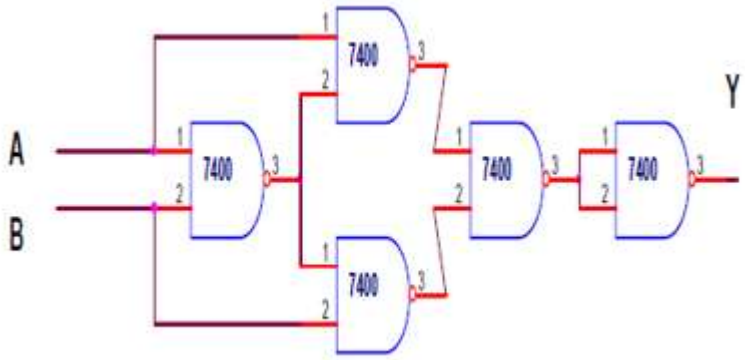
OR Gate:



Truth Table

A	B	Y=(A+B)
0	0	0
0	1	1
1	0	1
1	1	1

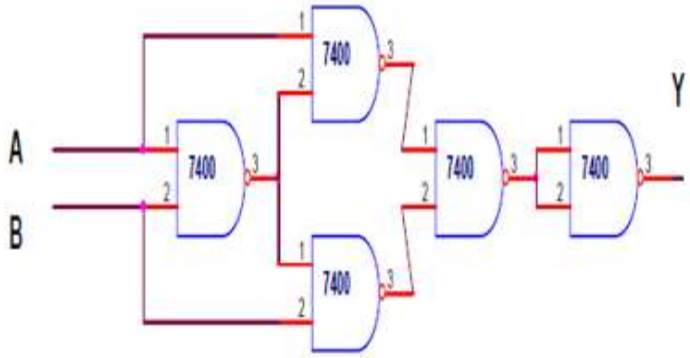
EX-OR Gate:



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

EX-NOR:



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Procedure:

1. Connections are made as per the circuit diagram
2. Switch on the power supply
3. Apply different combinations of inputs and observe the outputs; compare the outputs with the truth tables.

Precautions:

1. All the connections should be made properly.

Result: Code converters are designed and their truth tables are verified.

9. Design of Combinational Logic Circuits

Aim: To design and construct Half-adder, Full-adder, Half-subtractor, Full- subtractor

Consumables:

S.No	Name	Quantity
1	IC 7432	1
2	IC 7408	1
3	IC 7486	1
4	IC 7400	1
5	Electronic circuit Designer	
6	Patch chords	

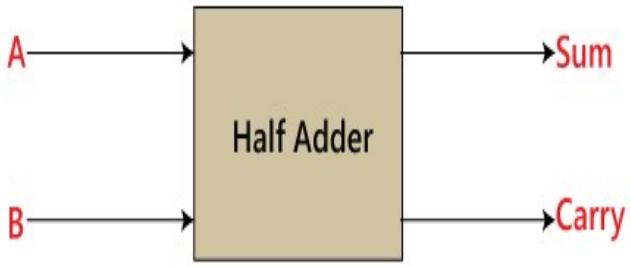
Theory:

Combinational circuit is a circuit in which we combine the different gates in the circuit, for example encoder, decoder, multiplexer and demultiplexer. Some of the characteristics of combinational circuits are

1. The output of combinational circuit at any instant of time depends only on the levels present at input terminals.
2. The combinational circuit do not use any memory. The previous state of input does not have any effect on the present state of the circuit.
3. A combinational circuit can have an n number of inputs and m number of outputs.

Half Adder:

The Half-Adder is a basic building block of adding two numbers as two inputs and produce out two outputs. The adder is used to perform OR operation of two single bit binary numbers. The augent and addent bits are two input states, and **'carry'** and **'sum** 'are two output states of the half adder.



Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

In the above table,

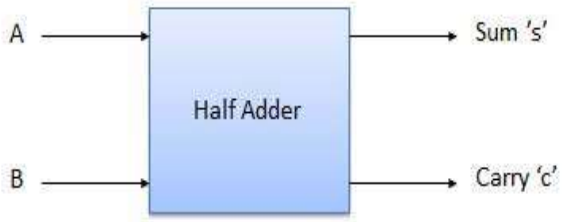
1. 'A' and' B' are the input states, and 'sum' and 'carry' are the output states.
2. The carry output is 0 in case where both the inputs are not 1.
3. The least significant bit of the sum is defined by the 'sum' bit.
4. The SOP form of the sum and carry are as follows:

   Sum=x'y+xy'

   Carry = xy

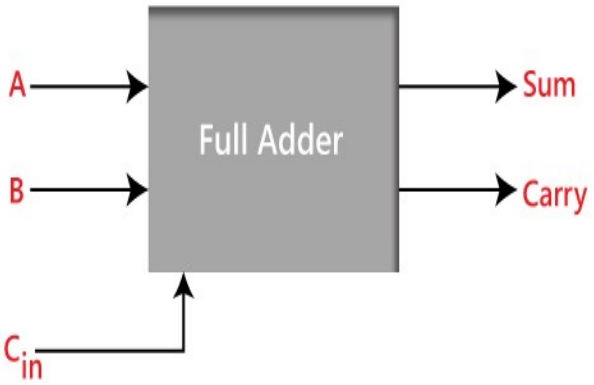
Half Adder:

Half adder is a combinational logic circuit with two inputs and two outputs. The half adder circuit is designed to add two single bit binary number A and B. It is the basic building block for addition of two **single** bit numbers. This circuit has two outputs **carry** and **sum**.



Full Adder:

The half adder is used to add only two numbers. To overcome this problem, the full adder was developed. The full adder is used to add three 1-bit binary numbers A, B, and carry C. The full adder has three input states and two output states i.e., sum and carry.



Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

In the above table,

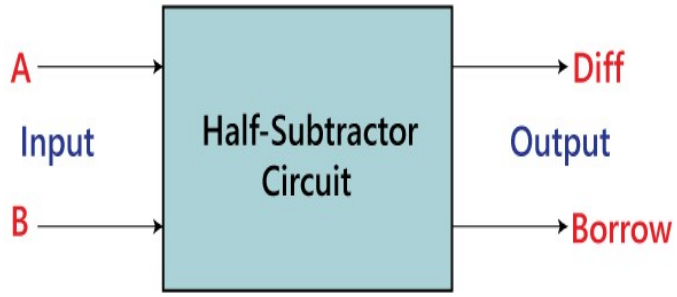
1. 'A' and' B' are the input variables. These variables represent the two significant bits which are going to be added
2. 'C_{in}' is the third input which represents the carry. From the previous lower significant position, the carry bit is fetched.
3. The 'Sum' and 'Carry' are the output variables that define the output values.
4. The eight rows under the input variable designate all possible combinations of 0 and 1 that can occur in these variables.

Sum = x' y' z+x' yz+xy' z'+xyz

Carry = xy+xz+yz

Half Subtractor:

The half subtractor is also a building block for subtracting two binary numbers. It has two inputs and two outputs. This circuit is used to subtract two single bit binary numbers A and B. The 'diff' and 'borrow' are two output states of the half subtractor.



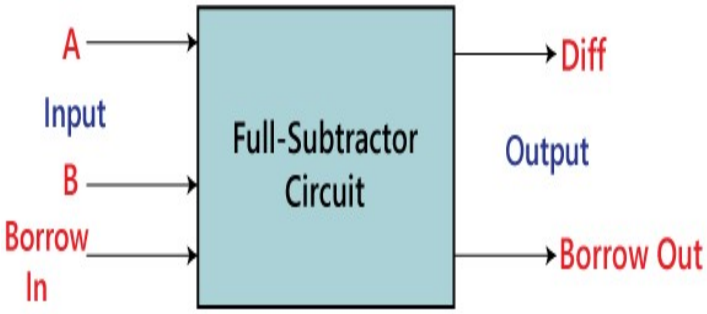
Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The SOP form of the **Diff** and **Borrow** is as follows:

Diff=A'B+AB'
Borrow = A'B

Full Subtractor

The Half Subtractor is used to subtract only two numbers. To overcome this problem, a full subtractor was designed. The full subtractor is used to subtract three 1-bit numbers A, B, and C, which are minuend, subtrahend, and borrow, respectively. The full subtractor has three input states and two output states i.e., diff and borrow.



Inputs			Outputs	
A	B	$Borrow_{in}$	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

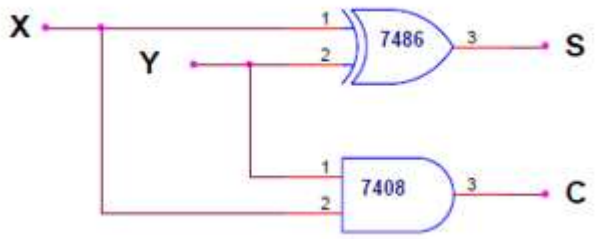
In the above table,

1. 'A' and' B' are the input variables. These variables represent the two significant bits that are going to be subtracted.
2. 'Borrow' is the third input which represents borrow.
3. The 'Diff' and 'Borrow' are the output variables that define the output values.
4. The eight rows under the input variable designate all possible combinations of 0 and 1 that can occur in these variables.

Diff=xy' z'+x' y' z+xyz+x'yz'
Borrow=x' z+x' y+yz

Circuit Diagram:

Half Adder: **Truth Table**

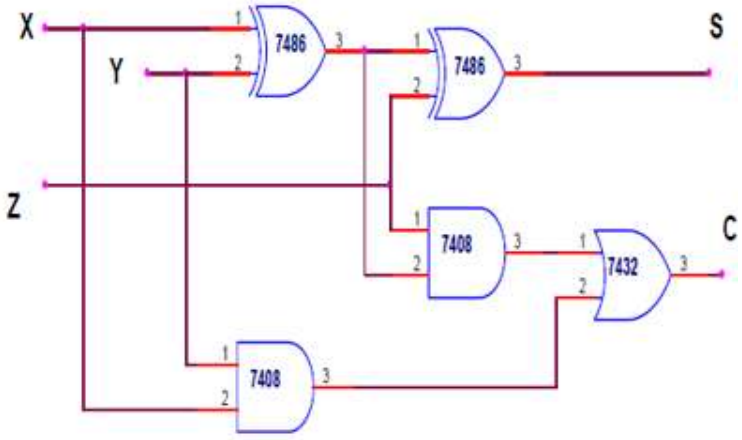


A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder:

Truth Table

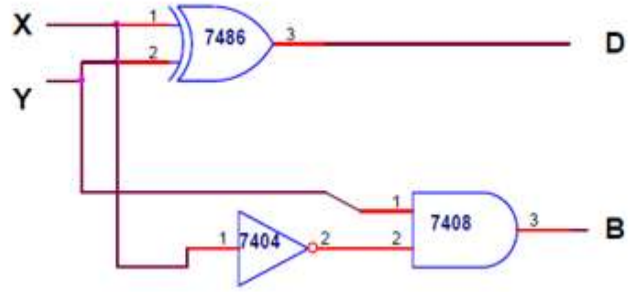
A	B	C	Sum	Carry
0	0	0	0	0
0	1	0	1	0
0	0	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Half Subtractor:

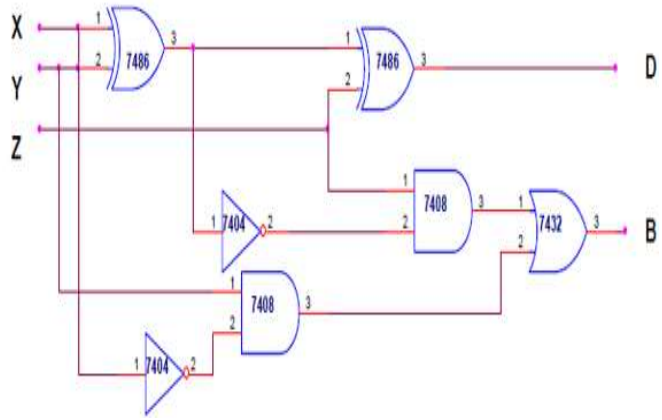
Truth Table

A	B	Difference	Barrow
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Full Subtractor:

Truth Table



A	B	C	Difference	Barrow
0	0	0	0	0
0	1	0	1	1
0	0	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Procedure:

1. Connections are made as per the circuit diagram
2. Switch on the power supply
3. Apply different combinations of inputs and observe the outputs; compare the outputs with the truth tables.

Precautions:

1. All the connections should be made properly.

Result: Code converters are designed and their truth tables are verified.

10. Design of Code Convertors

Aim: To design code converters and verify their truth tables

Components:

S.No	Name	Quantity
1	IC 7486	2
2	Electronic circuit Designer	
3	Patch chords	

Theory:

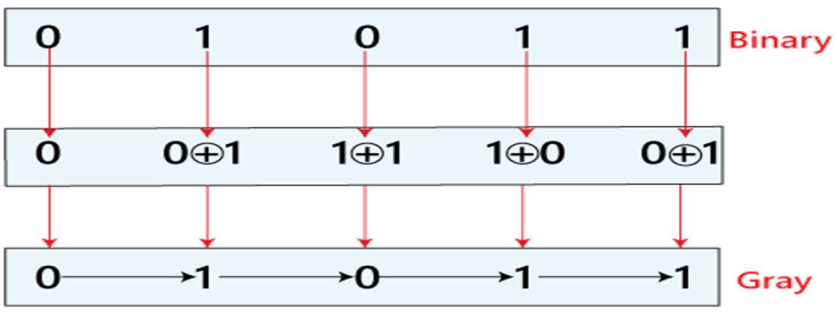
The Binary to Gray code converter is a logical circuit that is used to convert the binary code into its equivalent Gray code. By putting the MSB of 1 below the axis and the MSB of 1 above the axis and reflecting the (n-1) bit code about an axis after 2^{n-1} rows, we can obtain the n-bit gray code.

Gray code – also known as **Cyclic Code**, **Reflected Binary Code** (RBC), **Reflected Binary** (RB) or **Grey code** – is defined as an ordering of the binary number system such that each incremental value can only differ by one bit. In gray code, while traversing from one step to another step only one bit in the code group changes. That is to say that two adjacent code numbers differ from each other by only one bit.

Gray code is the most popular of the unit distance codes, but it is not suitable for arithmetic operations. Gray code has some applications in analog to digital converters, as well as being used for error correction in digital communication.

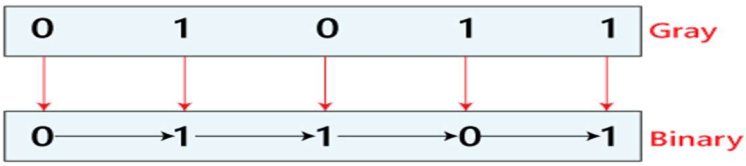
How to Convert Binary to Gray Code:

1. The MSB (Most Significant Bit) of the gray code will be exactly equal to the first bit of the given binary number.
2. The second bit of the code will be exclusive-or (XOR) of the first and second bit of the given binary number, i.e if both the bits are same the result will be 0 and if they are different the result will be 1.
3. The third bit of gray code will be equal to the exclusive-or (XOR) of the second and third bit of the given binary number. Thus the binary to gray code conversion goes on.



Gray code to binary conversion is again a very simple and easy process. Following steps can make your idea clear on this type of conversions.

1. The MSB of the binary number will be equal to the MSB of the given gray code.
2. Now if the second gray bit is 0, then the second binary bit will be the same as the previous or the first bit. If the gray bit is 1 the second binary bit will alter. If it was 1 it will be 0 and if it was 0 it will be 1.
3. This step is continued for all the bits to do **Gray code to binary conversion**.

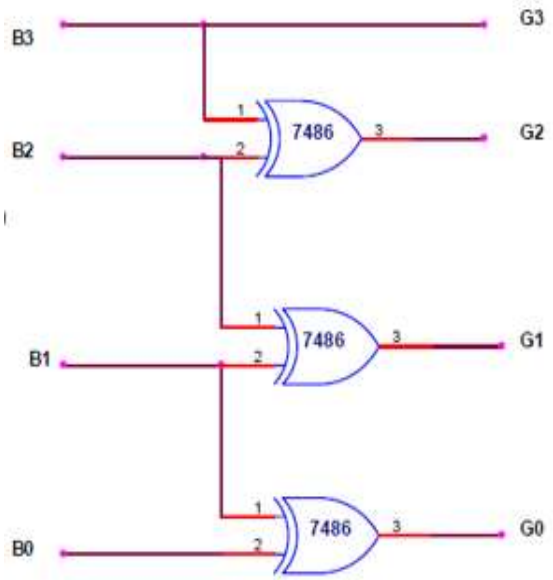


Circuit Diagram:

Binary to Gray:

Truth Table

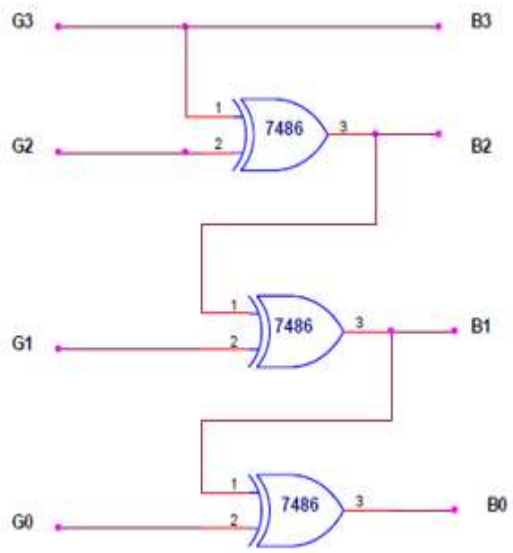
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0



Gray to Binary:

Truth Table

G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0



Procedure:

1. Connections are made as per the circuit diagram
2. Switch on the power supply
3. Apply different combinations of inputs and observe the outputs; compare the outputs with the truth tables.

Precautions:

1. All the connections should be made properly.

Result: Code converters are designed and their truth tables are verified.

11. Design of 4X1 Multiplexer and 1x4 Demultiplexer

Aim: To design multiplexers and demultiplexers and verify their truth tables.

Components:

S.No	Name of the item	Quantity
1	IC 7404	1
2	IC 7432	1
3	IC 7411	2
4	IC 7408	1
5	Electronic circuit designer	
6	Connecting wires	As Required

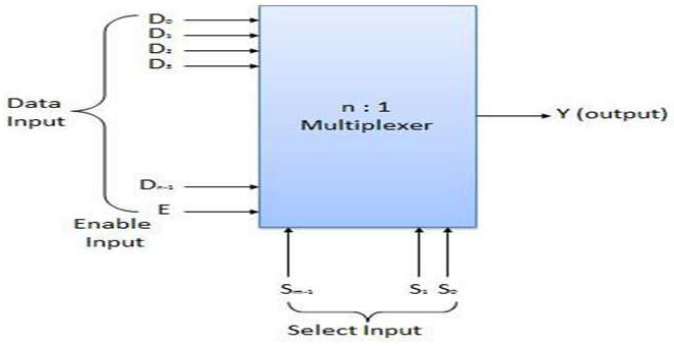
Theory:

***Multiplexers*:**

Amultiplexer (or MUX) is a circuit with many inputs but only one output and acts like a very fast acting rotary switch. It selects one of many analog or digital input signals (2, 4, 8,16andsoon) and forwards the selected input into a single line output. The selection of a particular input channel is controlled by a set of select inputs. A digital multiplexer of 2^n input channels can be controlled by n number of select lines.

A4-to-1 line multiplexer, for example, consists of 4 input channels and2 selection inputs. Its circuit diagram and truth table are shown below. The data input channels D_0 to D_3 are selected by combinations of select inputs A and B. To understand its operation, let us consider that the select input combination AB is 01. The AND gate associated with D_1 will have two inputs of logic 1 and the third input is D_1. Thus the output of this AND gate will follow D_1.

The other three AND gates have at least one of their inputs at logic 0 to make their output 0, irrespective of the rest of the data inputs X (0 or 1). Hence the OR output will follow D_1 only.



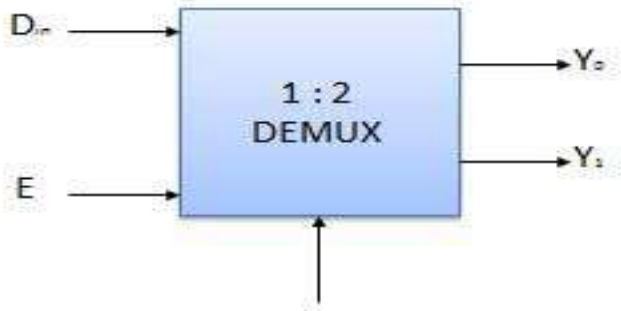
Understanding 4-to-1 Multiplexer:

The 4-to-1 multiplexer has 4 input bits, 2 control or select bits, and 1 output bit. The four input bits are D0, D1, D2 and D3. Only one of this is transmitted to the output Y. The output depends on the values of A and B, which are the control inputs. The control input determines which of the input data bit is transmitted to the output.

For instance, as shown in figure, when A B = 0 0, the upper AND gate is enabled, while all other AND gates are disabled. Therefore, data bit D0 is transmitted to the output, giving Y = Do.

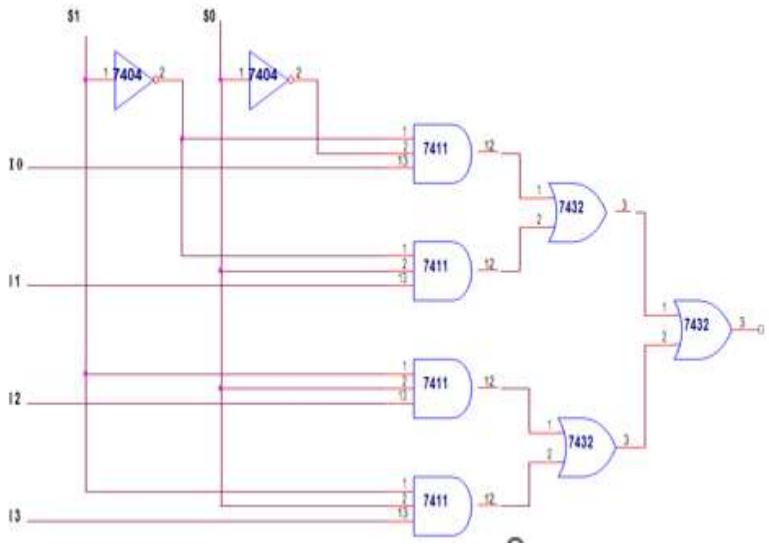
Demultiplexers:

A demultiplexer circuit is the reverse of a multiplexer circuit. Demultiplexing is the process that receives information from one channel, i.e. single input and distributes the data over several output channels. Selection of a specific output line is controlled by the selection input lines. A 1-to-4 demultiplexer circuit is shown in the circuit diagram along with its characteristic table. The selection input lines A and B activate an AND gate according to its bit combination. The input line D (0 or 1) is common to one of the inputs of all AND gates. So the input D is passed to that particular output line which is activated by the particular AND gate. As an example, for the selection input combination 00, input D is transmitted to Y_0.



The input bit is labeled as Data D. This data bit is transmitted to the selected output lines, which depends on the values of A and B, the control or Select Inputs. When A B = 0 1, the second AND gate from the top is enabled while other AND gates are disabled. Therefore, data bit D is transmitted to the output Y1, giving Y1 = Data. If D is LOW, Y1 is LOW. If D is HIGH, Y1 is HIGH. The value of Y1 depends upon the value of D. All other outputs are in low state. If the control input is changed to A B = 1 0, all the gates are disabled except the third AND gate from the top. Then, D is transmitted only to the Y2 output, and Y2 = Data.

Circuit Diagram:

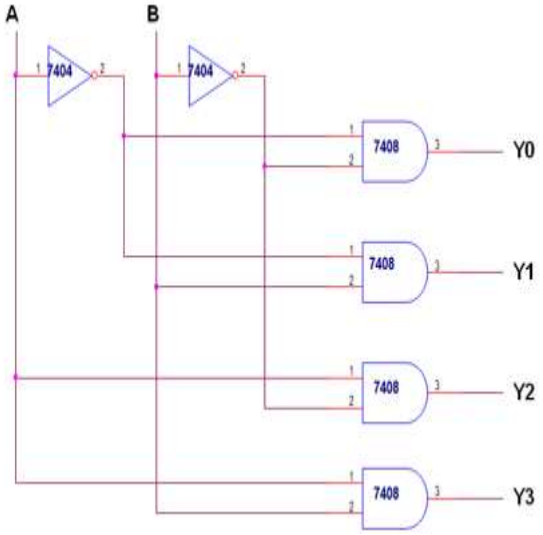


***Multiplexers*: Truth Table**

Selection Inputs		Input Channels				Output
A	**B**	**D_0**	**D_1**	**D_2**	**D_3**	**Y**
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

Demultiplexers:

Truth Table:



D = 0 or 1

Selection inputs		Output Channels			
A	B	Y_0	Y_1	Y_2	Y_3
0	0	D	0	0	0
0	1	0	D	0	0
1	0	0	0	D	0
1	1	0	0	0	D

Procedure:

1. Connections are made as per the circuit diagram
2. Switch on the power supply
3. Apply different combinations of inputs and observe the outputs; compare the outputs with the truth tables.

Precautions:

1. All the connections should be made properly.

Result:

12. Realization of RS - JK & D flip-flop using logic gates.

Aim: To design and construct basic flip-flops R-S, J-K, J-K Master slave flip-flops using gates and verify their truth tables.

Consumables:

Name	Quantity
IC 7404	1
IC 7402	1
IC 7400	1
Electronic circuit Designer	
Patch chords	

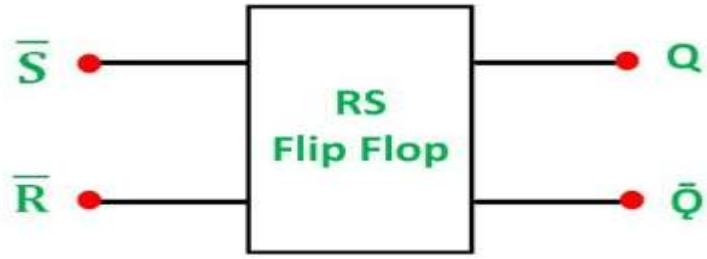
Theory:

RS Flip-Flop:

The RS Flip Flop is considered as one of the most basic sequential logic circuits. The Flip Flop is a one-bit memory bi-stable device. It has two inputs, one is called **"SET"** which will set the device (output = 1) and is labelled S and another is known as **"RESET"** which will reset the device (output = 0) labelled as R. The RS stands for **SET/RESET.**

The flip-flop is reset back to its original state with the help of RESET input and the output is Q that will be either at logic level "1" or logic"0". It depends upon the set/reset condition of the flip-flop. Flip flop word means that it can be **"FLIPPED"** into one logic state or **"FLOPPED"** back into another. The basic NAND gate RS Flip Flop circuit is used to store the data and thus provides feedback from both of its outputs again back to its inputs.

The RS Flip Flop actually has three inputs, SET, RESET and its current output Q relating to its current state.

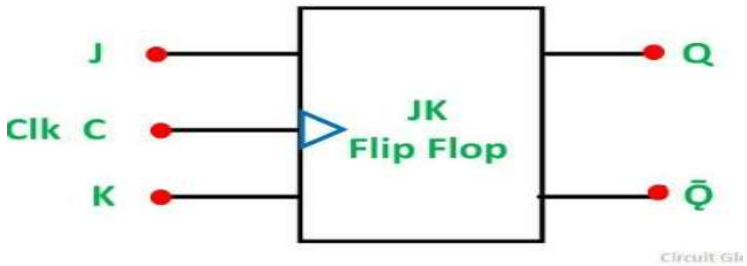


The NAND Gate RS Flip Flop:

A pair of cross-coupled 2 unit NAND gates is the simplest way to make any basic one-bit set/reset RS Flip Flop. It forms Set/Reset bi-stable or an active LOW RS NAND gate latch. The feedback is fed from each output to one of the other NAND gate input. The device consists of two inputs; one is known as SET, (S) and the other is called as RESET, (R).

JK Flip Flop:

The **JK Flip Flop** is the most widely used flip flop. It is considered to be a universal flip-flop circuit. The sequential operation of the JK Flip Flop is the same as for the RS flip-flop with the same **SET** and **RESET** input. The difference is that the JK Flip Flop does not the invalid input states of the RS Latch (when S and R are both 1). The JK Flip Flop name has been kept on the inventor name of the circuit known as **Jack Kilby.** The basic **symbol** of the JK Flip Flopis.



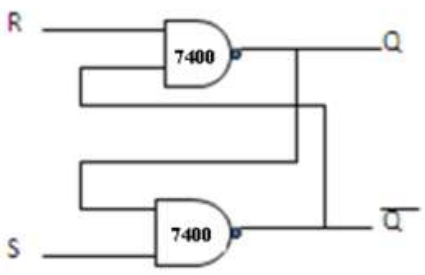
The basic NAND gate RS flip-flop suffers from two main problems. Firstly, the condition when S = 0 and R = 0 should be avoided. Secondly, if the state of S or R changes its state while the input which is enabled is high, the correct latching action does not occur. Thus to overcome these two problems of the RS Flip-Flop, the JK Flip Flop was designed. The JK Flip Flop is basically a gated RS flip flop with the addition of the clock input circuitry.

When both the inputs S and R are equal to logic "1", the invalid condition takes place. Thus, to prevent this invalid condition, a clock circuit is introduced. The JK Flip Flop has four possible input combinations because of the addition of the clocked input. The four inputs are "logic 1", 'logic 0". "No change' and "Toggle".

JK flip-flop has a drawback of timing problem known as **"RACE".** The condition of RACE arises if the output Q changes its state before the timing pulse of the clock input has time to go in OFF state.

Circuit Diagram:

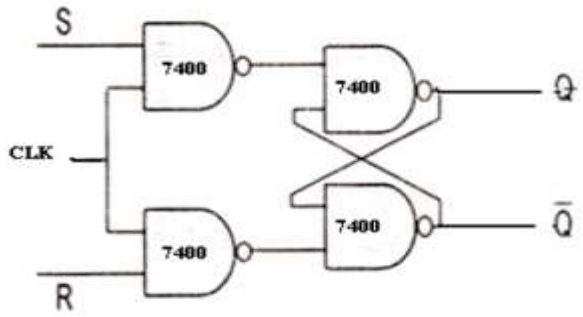
Basic Flip flop using NAND Gate:



Truth Table

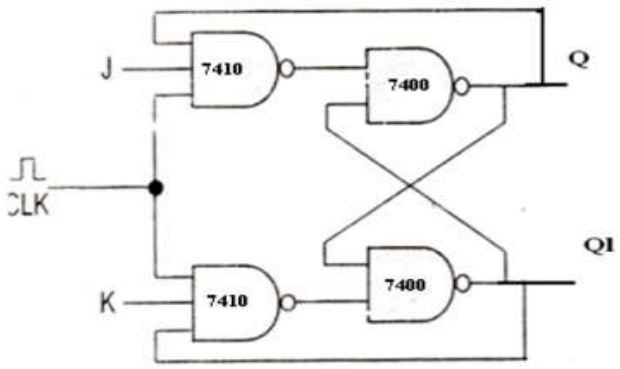
S	R	Q
0	0	Forbidden
0	1	1
1	0	0
1	1	No change

R-S Flip flop using NAND Gate: **Truth Table**



S	R	Q
0	0	No change
0	1	0
1	0	1
1	1	Forbidden

J-K Flip flop using NAND Gate: **Truth Table**



J	K	Q
0	0	No change
0	1	0
1	0	1
1	1	Race around

Procedure:

1. Connections are made as per the circuit diagram
2. Switch on the power supply
3. Apply different combinations of inputs and observe the outputs; compare the outputs with the truth tables.

Precautions:

1. All the connections should be made properly.

Result:

13. Design of synchronous counter, mod counter, up counter, down counter and up/down counter Using flip flops

Aim: To design and construct of 3-bit Synchronous up and down counters, 2-bit up/down counter.

Consumables:

Name	Quantity
IC 7408	1
IC 7476	1
IC 7400	1
IC 7400	1
Electronic Circuit Designer	
Patch chords	

Theory:

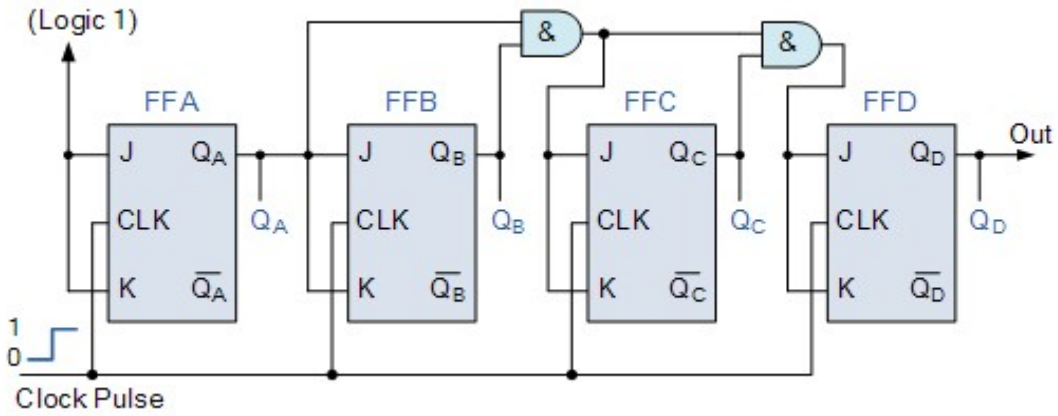
A counter is a device which can count any particular event on the basis of how many times the particular event(s) is occurred. In a digital logic system or computers, this counter can count and store the number of time any particular event or process have occurred, depending on a clock signal. Most common type of counter is sequential digital logic circuit with a single clock input and multiple outputs. The outputs represent binary or binary coded decimal numbers. Each clock pulse either increase the number or decrease the number.

Synchronous Counter:

Synchrounous generally refers to something which is coordinated with others based on time. Synchronous signals occur at same clock rate and all the clocks follow the same reference clock. In synchronous counter**,** the clock input across all the flip-flops use the same source and creates the same clock signal at the same time. So, a counter which is using the same clock signal from the same source at the same time is called Synchronous counter**.**

Synchronous UP Counter:

The basic Synchronous counter design is shown which is Synchronous up counter**.** A 4-bit Synchronous up counter start to count from 0 (0000 in binary) and increment or count upwards to 15 (1111 in binary) and then start new counting cycle by getting reset. Its operating frequency is much higher than the same range Asynchronous counter. Also, there is no propagation delay in the synchronous counter just because all flip-flops or counter stage is in parallel clock source and the clock triggers all counters at the same time.

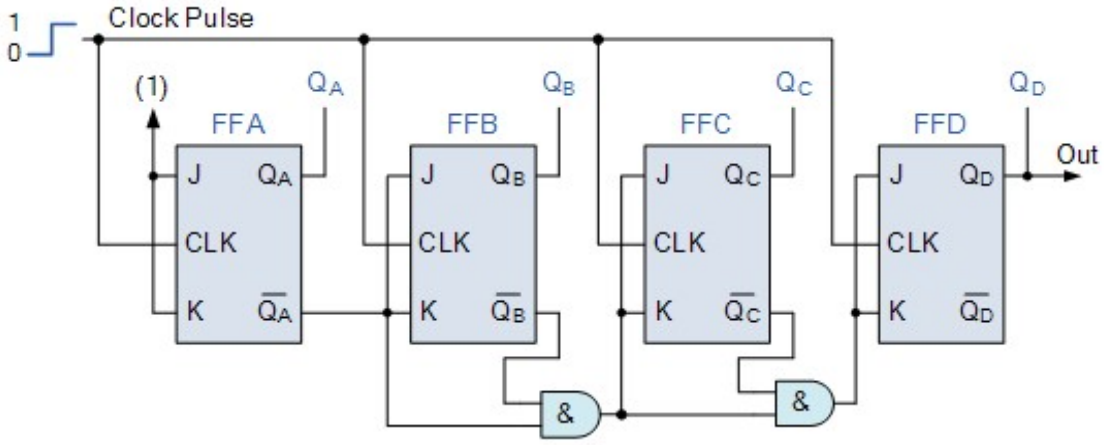


The external clock is directly provided to all J-K Flip flops at the same time in a parallel way. If we see the circuit, the first flip-flop**,** FFA which is the least significant bit in this 4-bit synchronous counter, is connected to a Logic 1 external input via J and K pin. Due to this connection, HIGH logic across the Logic 1 signal, change the state of first flip-flop on every clock pulse.

Next stage, the second flip-flop FFB, input pin of J and K is connected across the output of the first Flip-flop. For the case of FFC and FFD, two separate AND gate provide the necessary logic across them. Those AND gates create logic using the input and output from the previous stage flip-flops.

We can create the same counting sequence used in the Asynchronous counter by making a situation where each flip-flops change its state depending on whether all preceding flip-flops output is HIGH in logic. But in this scenario, there will be no ripple effect just because all flip-flops are clocked at the same time.

Synchronous Down Counter:

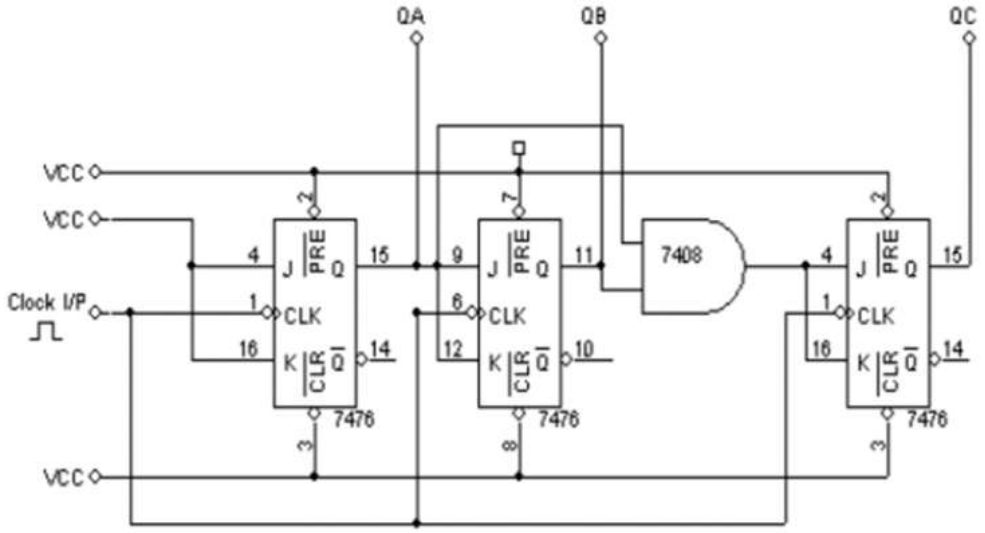


Slight changes in AND section, and using the inverted output from J-K flip-flop, we can create Synchronous down Counter**.** A 4-bitSynchronous down counter start to count from 15 (1111 in binary) and decrement count downwards to 0 or 0000 and after that it will start a new counting cycle by getting reset. In synchronous down counter**,** the AND Gate input is changed. First Flip-flop FFA input is same as we used in previous Synchronous up counter. Instead of

directly feeding the output of the first flip-flop to the next subsequent flip-flop, we are using inverted output pin which is used to give J and K input across next flip-flop FFB and used as input pin across the AND gate. Same as like the previous circuit, two AND gates are providing necessary logic to the next two Flip-flops FFC and FFD.

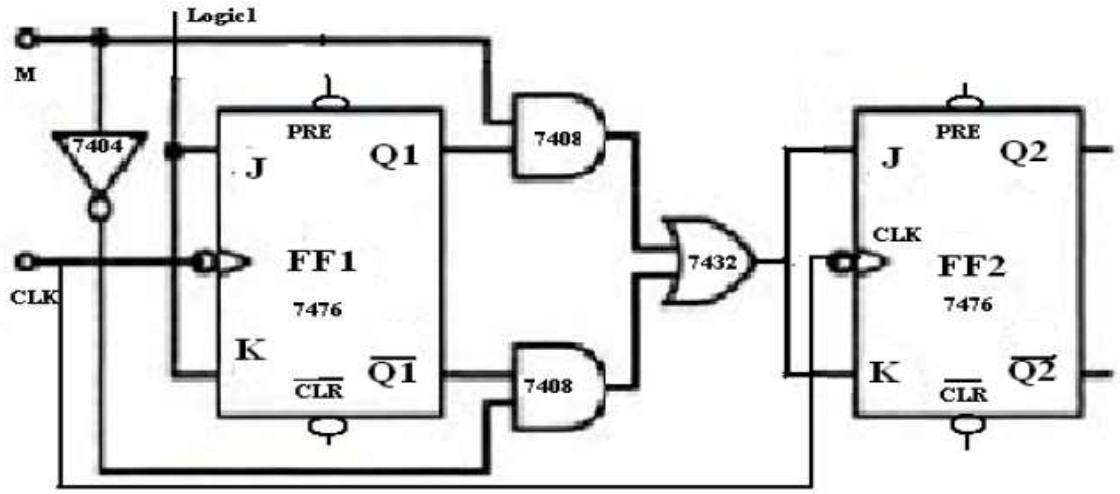
Circuit Diagram:

3-bit synchronous counter:



3 bit Synchronous up counter			
Clock	**QC**	**QB**	**QA**
0	**0**	**0**	**0**
1	**0**	**0**	**1**
2	**0**	**1**	**0**
3	**0**	**1**	**1**
4	**1**	**0**	**0**
5	**1**	**0**	**1**
6	**1**	**1**	**0**
7	**1**	**1**	**1**
8	**0**	**0**	**0**

Two Bit up/Down Counter using negative edge-triggered flip-flops:



Truth Table:

When M=1

CLK	Q2	Q1
0	0	0
1	0	1
2	1	0
3	1	1

When M=0

CLK	Q2	Q1
0	1	1
1	1	0
2	0	1
3	0	0

Procedure:

1. Connections are made as per the circuit diagram
2. Switch on the power supply
3. Apply different combinations of inputs and observe the outputs; compare the outputs with the truth tables.

Precautions:

1. All the connections should be made properly.

Result:

14. Design and testing of monostable and astable Multi Vibrators Using 555 Timers.

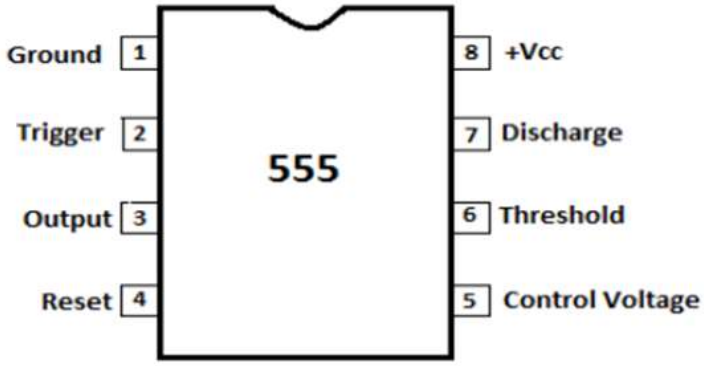
Aim: To generate a pulse using monostable multivibrator and to generate unsymmetrical square and symmetrical square waveforms using IC555

Components:

S.No	Components	Range
1	Electronic circuit designer	
2	IC	555
3	Connecting wires	
4	Resistors	3.6KΩ, 7.2 KΩ,10 KΩ
5	Capacitors	0.1µf, 0.01µf
6	Diode	IN4001
7	RPS	(0-30) V
8	CRO	(0-1)MHZ

Theory:

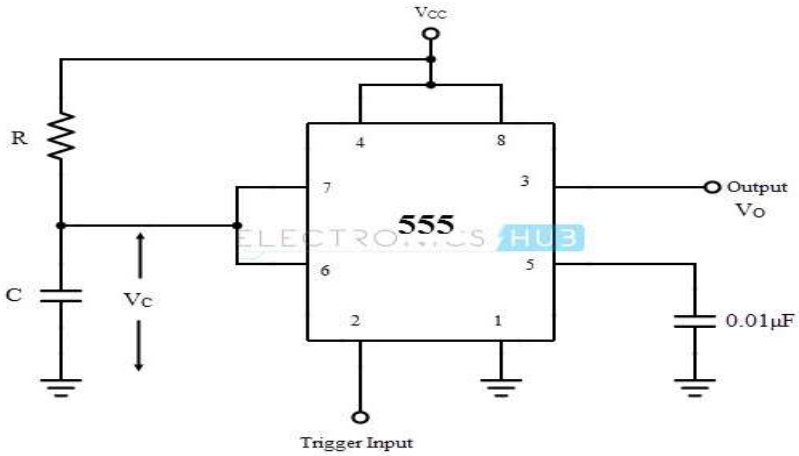
The 555 IC available as an 8-pin metal can as given below:



Monostable operation:

A Monostable Multivibrator, often called a one-shot Multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby mode the output of the circuit is approximately Zero or at logic-low level. When an external trigger pulse is obtained, the output is forced to go high (≅ VCC). The time the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The Monostable circuit has only one stable state (output low),

hence the name monostable. Normally the output of the Monostable Multivibrator is low. When the power supply VCC is connected, the external timing capacitor 'C" charges towards VCC with a time constant (RA+RB) C. During this time, pin 3 is high (≈VCC) as Reset R=0, Set S=1 and this combination makes Q =0 which has unclamped the timing capacitor 'C'.



Astable operation:

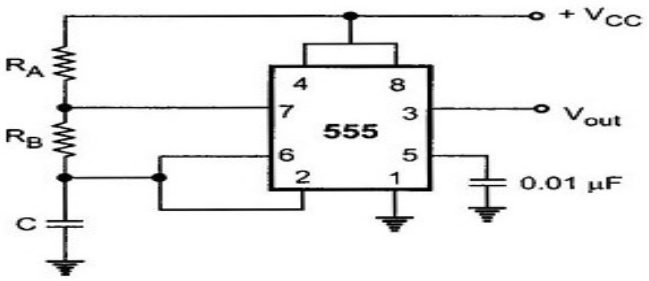
When the capacitor voltage equals 2/3 VCC, the UC triggers the control flip flop on that Q =1. It makes Q1 ON and capacitor 'C' starts discharging towards ground through RB and transistor Q1 with a time constant RBC. Current also flows into Q1 through RA. Resistors RA and RB must be large enough to limit this current and prevent damage to the discharge transistor Q1. 52 The minimum value of RA is approximately equal to VCC/0.2 where 0.2A is the maximum current through the ON transistor Q1. During the discharge of the timing capacitor C, as it reaches VCC/3, the LC is triggered and at this stage S=1, R=0 which turns Q =0. Now Q =0 unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between 2/3 VCC and 1/3 VCC respectively. The length of time that the output remains HIGH is the time for the capacitor to charge from 1/3 VCC to 2/3 VCC.

The capacitor voltage for a low pass RC circuit subjected to a step input of VCC volts is given by VC = VCC (1- e-t/RC)

Total time period T = 0.69 (RA + 2 RB) C

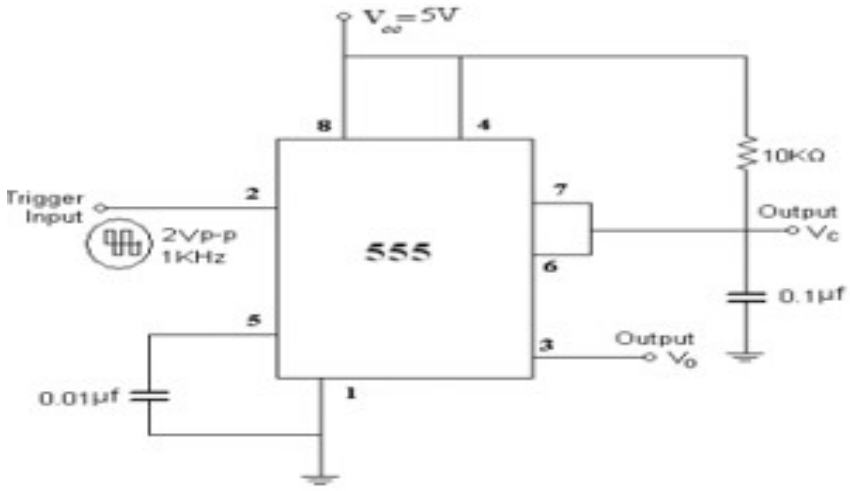
$$f = \frac{1}{T} = \frac{1}{0.693(R_A + 2R_B)C}$$

$$f = \frac{1.44}{(R_A + 2R_B)C} \text{ Hz}$$

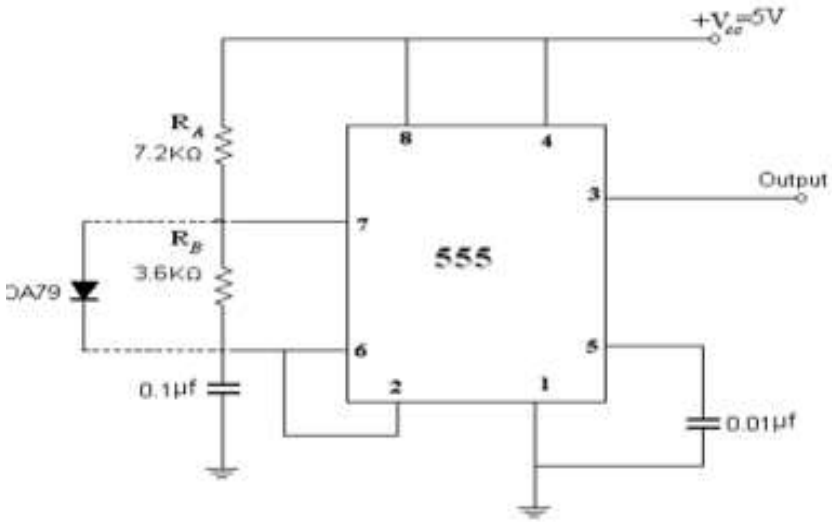


Circuit Diagram:

Monostable Multivibrator:



Astable Multivibrator:



Procedure:

Monostable operation:

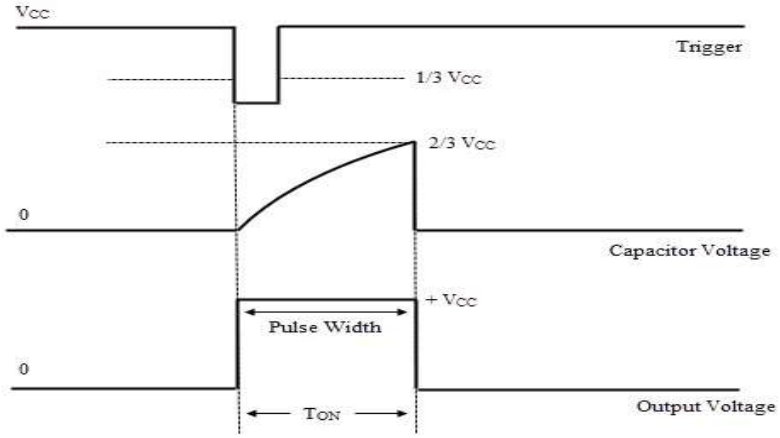
1. Connect the circuit as shown in the circuit diagram.
2. Apply Negative triggering pulses at pin 2 of frequency 1 KHz.
3. Observe the output waveform and capacitor voltage and measure the pulse duration
4. Theoretically calculate the pulse duration as T=1.1. RC
5. Compare it with experimental values.

Astable operation:

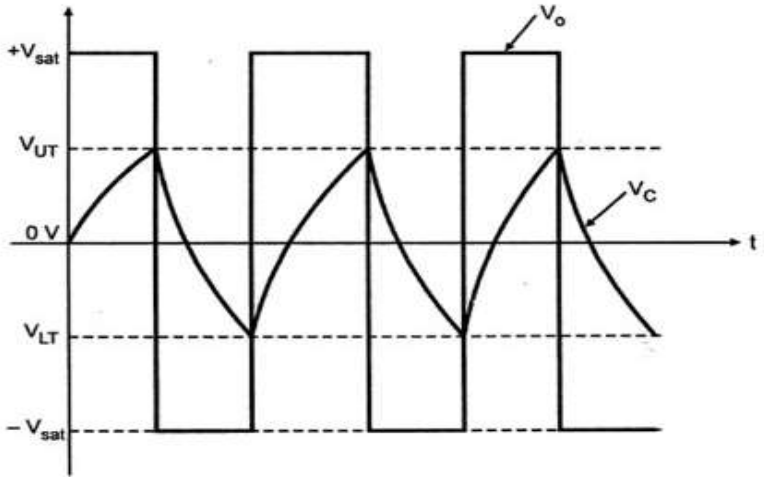
1. Connect the circuit as per the circuit diagram.
2. Observe and note down the output waveform at pin 3 and across timing capacitor.
3. Measure the frequency of oscillations and duty cycle and then compare with the given values.
4. Sketch both the waveforms to the same time scale

Expected Waveform:

Monostable Multivibrator:



Astable Multivibrator:



Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Result: The input and output waveforms of 555 timer as Monostable multivibrator and Astable multivibrator are drawn.

15. Design a 4-Bit R-2R Ladder type of digital to Analog Converter.

Aim: To design R-2R ladder type digital to Analog converter

Apparatus:

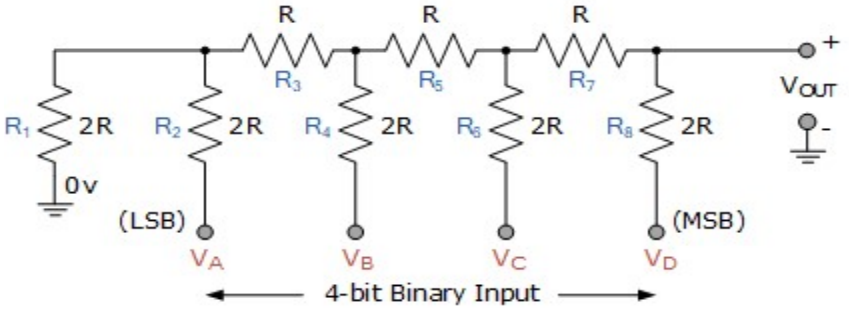
S.NO.	COMPONENTS	RANGE
1	Electronic circuit designer	
2	IC	741
3	Connecting wires	
4	Resistors	1KΩ, 2 KΩ
5	RPS	(0-30) V
6	Multimeter	

THEORY:

The R-2R resistive ladder network uses just two resistive values. One resistor has the base value "R", and the second resistor has twice the value of the first resistor, "2R", no matter how many bits are used to make up the ladder network.

So for example, we could just use a standard 1kΩ resistor for the base resistor "R", and therefore a 2kΩ resistor for "2R" (or multiples thereof as the base value of R is not too critical). Thus the resistive value of 2R will always be twice the value of the base resistor, R. That is 2R = 2*R. This means that it is much easier for us to maintain the required accuracy of the resistors along the ladder network c

Input voltages are applied to the ladder network at various points along its length and the more input points the better the resolution of the R-2R ladder. The output signal as a result of all these input voltage points is taken from the end of the ladder which is used to drive the inverting input of an operational amplifier. Then a R-2R resistive ladder network is nothing more than long strings of parallel and series connected resistors acting as interconnected voltage dividers along its length, and whose output voltage depends soley on the interaction of the input voltages with each other.

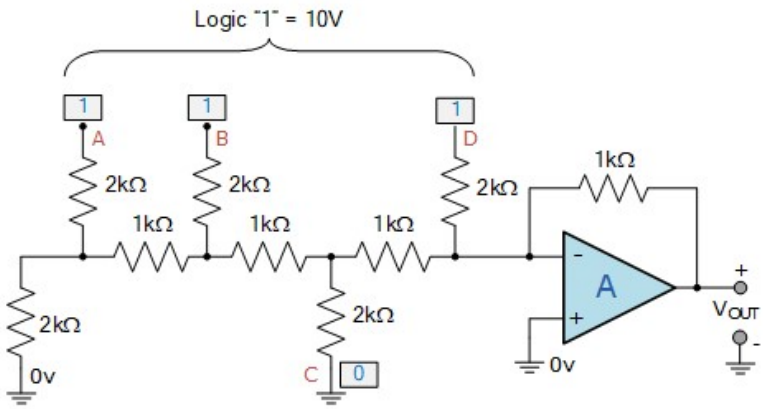


For R-2R ladder type DAC output voltage expressions given by

$$V_{OUT} = \frac{V_A + 2V_B + 4V_C + 8V_D}{16}$$

Where: "n" represents the number of digital inputs within the R-2R resistive ladder network of the DAC.

Circuit Diagrams:



Procedure:

1. Connect the circuit as shown
2. Vary the inputs A, B, C, D from the digital trainer board and note down the output at pin 6. For logic '1', 5 V is applied and for logic '0', 0 V is applied.
3. Repeat the above two steps for R – 2R ladder DAC for different logic inputs and not down the analog output voltage

Tabular form:

S.No	D	C	B	A	Theoretical Voltage (V)	Practical Voltage (V)

Model Graph:

Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Results: Outputs of R-2R ladder DAC are observed.