Lab Code:20ECL401
Electronic Circuits
Lab Manual

Department of Electronics & Communication Engineering

Bapatla Engineering College :: Bapatla

(Autonomous)

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Contents

Bapatla Engineering College :: Bapatla
(Autonomous)

Vision

- To build centers of excellence, impart high quality education and instill high standards of ethics and professionalism through strategic efforts of our dedicated staff, which allows the college to effectively adapt to the ever changing aspects of education.

- To empower the faculty and students with the knowledge, skills and innovative thinking to facilitate discovery in numerous existing and yet to be discovered fields of engineering, technology and interdisciplinary endeavors.

Mission

- Our Mission is to impart the quality education at par with global standards to the students from all over India and in particular those from the local and rural areas.

- We continuously try to maintain high standards so as to make them technologically competent and ethically strong individuals who shall be able to improve the quality of life and economy of our country.

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Department of Electronics and Communication Engineering

Vision

To produce globally competitive and socially responsible Electronics and Communication Engineering graduates to cater the ever changing needs of the society.

Mission

- To provide quality education in the domain of Electronics and Communication Engineering with advanced pedagogical methods.

- To provide self-learning capabilities to enhance employability and entrepreneurial skills and to inculcate human values and ethics to make learners sensitive towards societal issues.

- To excel in the research and development activities related to Electronics and Communication Engineering.

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Department of Electronics and Communication Engineering

Program Educational Objectives (PEO's)

PEO-I: Equip Graduates with a robust foundation in mathematics, science and Engineering Principles, enabling them to excel in research and higher education in Electronics and Communication Engineering and related fields.

PEO-II: Impart analytic and thinking skills in students to develop initiatives and innovative ideas for Start-ups, Industry and societal requirements.

PEO-III: Instill interpersonal skills, teamwork ability, communication skills, leadership, and a sense of social, ethical, and legal duties to promote lifelong learning and Professional growth of the students.

Program Outcomes (PO's)

Engineering Graduates will be able to:

PO1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6. Engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7.Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. Individual and Teamwork: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. Life-long learning: Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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Department of Electronics and Communication Engineering

Program Specific Outcomes (PSO's)

PSO1: Develop and implement modern Electronic Technologies using analytical methods to meet current as well as future industrial and societal needs.

PSO2: Analyze and develop VLSI, IoT and Embedded Systems for desired specifications to solve real world complex problems.

PSO3: Apply machine learning and deep learning techniques in communication and signal processing.

Electronic Circuits Lab
II B.Tech – II Semester (Code: 20ECL401)

Lectures	0	Tutorial	0	Practical	3	Credits	1
Continuous Internal Assessment			50	Semester End Examination (3 Hours)			50

Prerequisites: Fundamentals of EDC Lab

Course Objectives: Students will

- Acquire a basic knowledge in solid state electronics including diodes, BJT, FET and their applications.
- Develop the ability to analyze and design analog electronic circuits using discrete Components.
- Generate simulations for the desired circuits using OrCAD PSpice circuit design software.

Course Outcomes: At the end of the course, student will be able to

CO1	Illustrate the characteristics of the diodes and its diverse applications including rectifiers and clippers and compare with the simulated outputs.
CO2	Design small signal amplifiers for given specifications using discrete components and verify using PSpice circuit design software
CO3	Distinguish the working of small signal amplifiers and power amplifiers.
CO4	Design the different types of oscillator circuits using BJT.

Mapping of Course Outcomes with Program Outcomes & Program Specific Outcomes

	PO's												**PSO's**		
CO	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
CO1	3	3		3	3				3				3		
CO2	3	3		3	3				3				3		
CO3	3	3		3					3				3		
CO4	3	3		3					3				3		
AVG	3	3		3	3				3				3		

LIST OF LAB EXPERIMENTS

1. Full Wave Rectifier with Centre tapped Transformer (Simulation/Hardware).
2. Bridge Rectifier (Simulation/Hardware).
3. Clippers (Simulation/Hardware).
4. Clampers (Simulation/Hardware).
5. Frequency response of CE amplifier (Simulation/Hardware).
6. Frequency response of Common-Source Amplifier Using FET (Simulation/Hardware).
7. Frequency response of Two stage RC-coupled amplifier (Simulation/Hardware).
8. Class-A Power Amplifier (Simulation/Hardware)
9. Complementary Symmetry Push-pull amplifier (Hardware).
10. Voltage shunt feedback amplifier (Hardware).
11. RC Phase Shift Oscillator (Hardware).
12. Colpitt"s Oscillator (Hardware).
13. Hartley Oscillator (Hardware).
14. BJT Darlington Emitter Follower (Hardware)
15. BJT Voltage Series Regulator/ Voltage Shunt Regulator(Hardware).

NOTE: A minimum of 10 (Ten) experiments has to be performed and recorded by the candidate to attain eligibility for Semester End Examination.

1.a FULL WAVE RECTIFIER WITH CENTRE TAPPED TRANSFORMER

Aim:

1. To observe the output waveforms of full wave rectifier without and with filter.
2. To find ripple factor and percentage regulation of FWR without and with filter.

Apparatus:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Bread board		1
2	Diodes	BY125 or IN4007	2 & 4
3	Resistor	1KΩ	1
4	Capacitor	470µF	1
5	Center tapped transformer	12V-0-12V	1
6	Digital multimeter/Digital voltmeter	0-20V	1
7	Cathode ray oscilloscope	0-20MHz	1
8	Connecting wires		Few

Circuit Diagram:

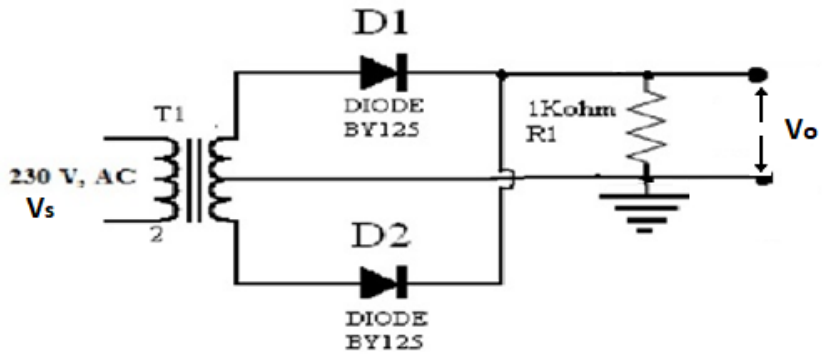


Fig 1: Full-wave rectifier without filter

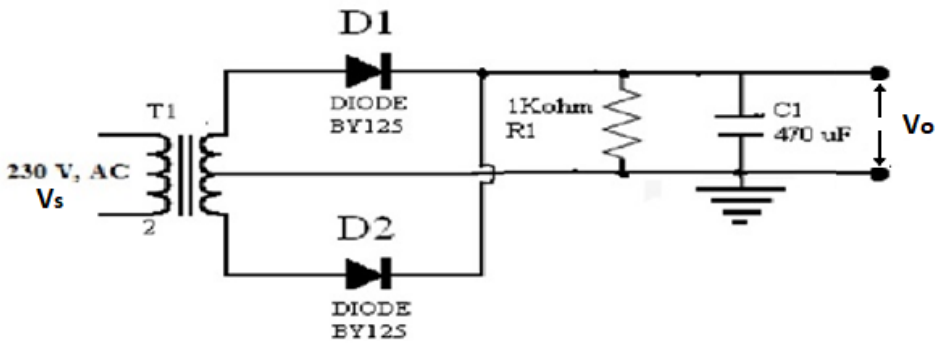


Fig 2: Full-wave rectifier with filter

Theory:

The full wave rectifier consists of two half wave rectifier circuits with common load. These are connected in such a way that conduction takes place through two diodes in alternate half-cycles and current through the load is sum of two currents. Thus, the output voltage waveform contains two half sinusoids in the two half-cycles of the AC input signal. The output of a rectifier is a pulsating DC consisting of a DC component and superimposed ripple. A way to eliminate or reduce the ripple to the required level is to use a filter.

Procedure:

(a) Full-wave rectifier without filter:

1. Connect the circuit as per the circuit diagram.
2. Connect the CRO across the load resistor R_1.
3. Note down the peak value V_m of the signal observed on the CRO.
4. Switch the CRO into DC mode and observe the waveform. Note down the DC shift.
5. Calculate V_{rms} and V_{dc} values by using the equation (1) and (2):

$$V_{rms} = \frac{V_m}{\sqrt{2}}, I_{rms} = \frac{I_m}{\sqrt{2}} \quad (1)$$

$$V_{dc} = \frac{2V_m}{\pi}, I_{dc} = \frac{2I_m}{\pi} \quad (2)$$

6. Calculate the ripple factor by using the equation (3):

$$Ripple\ factor = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} \quad (3)$$

7. Remove the load circuit (R_1 and C_1) and measure the voltage between the diode's cathode terminals and center tap of the transformer and represent as V_{NL}. Also note the voltage across the R_1 and C_1 and represent as V_{FL} and then calculate the percentage of voltage regulation using the equation (4):

$$\%\ Regulation = \frac{V_{NL} - V_{FL}}{V_{FL}}\ X\ 100 \quad (4)$$

(b) Full-wave rectifier with filter:

1. Connect the capacitor filler across the load R_1 in the above circuit diagram.
2. Proceed with the same procedure mentioned above to measure the V_m value and dc shift from the CRO.
3. Calculate $V_{r,rms}$ & $V_{dcshift}$ by using the equation (5):

$$V_{r,rms} = \frac{V_m}{2\sqrt{3}}, \quad (or) \quad V_{r,rms} = \frac{V_{dc}}{4\sqrt{3}fC_1R_1}, \tag{5}$$

Where V_m is the peak to peak amplitude of filter output.

4. Calculate ripple factor and % regulation by using equation (6):

$$Ripple\ factor = \frac{V_{r,rms}}{V_{dcshift}}, \tag{6}$$

$$\%\ of\ Regulation = \frac{V_{NL} - V_{FL}}{V_{NL}}\ X\ 100, \tag{7}$$

Model Graphs

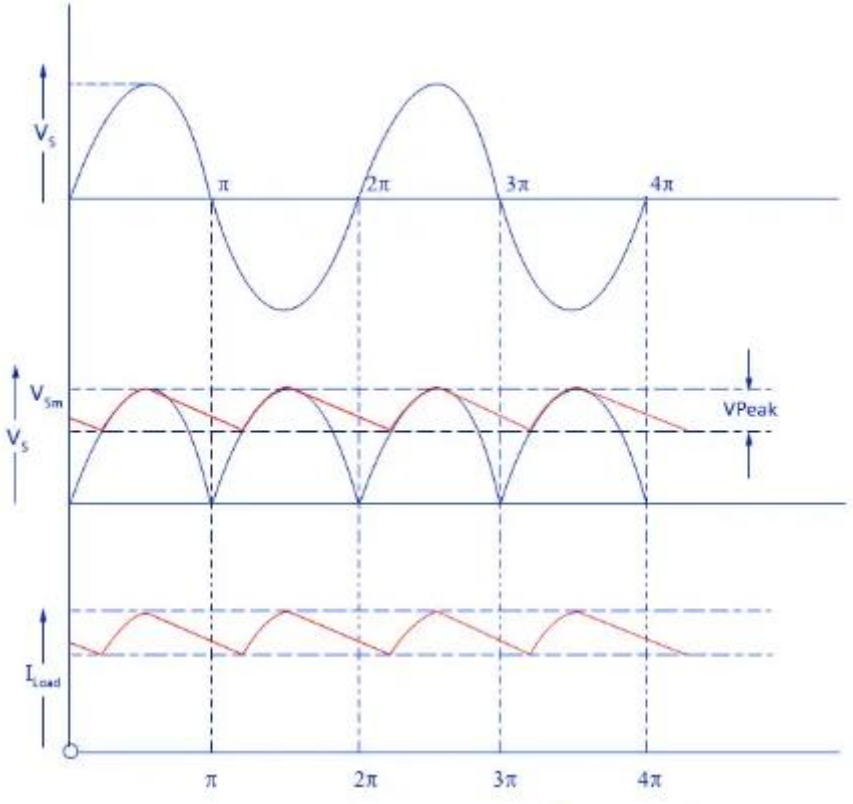


Fig 3: (a) Input signal (b) Rectified output waveform (c) Filtered output

Precautions:

1. Wires should be checked for good continuity.
2. Carefully note down the readings without any errors.

Result:

1.b Simulations of Full Wave Rectifier with Centre tapped Transformer

Aim: To design full wave rectifier with and without filter using pspice

Software Required: OrCAD Pspice 9.1

Full Wave Rectifier
Circuit Diagram:

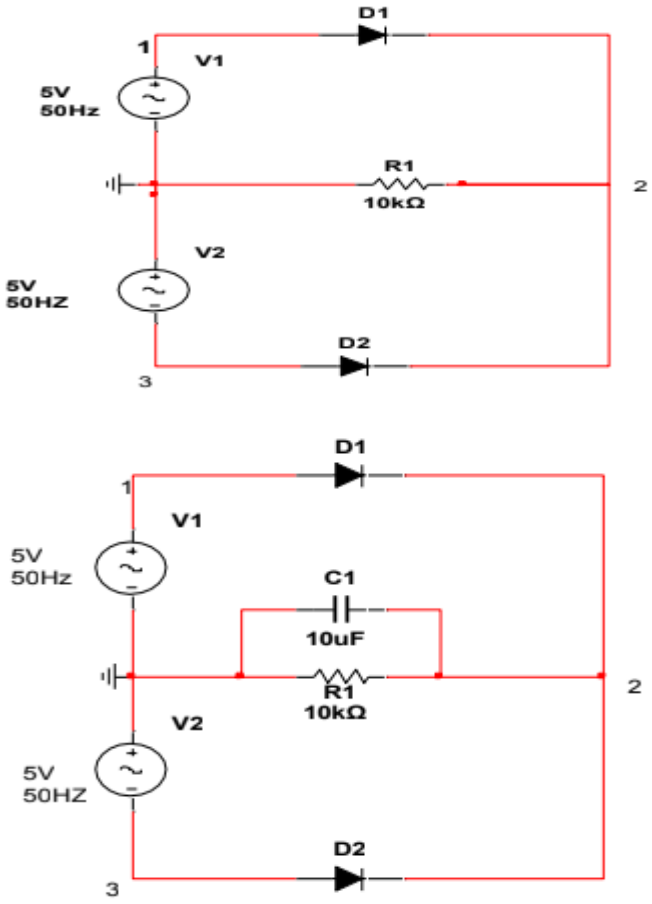


Fig 4: Full-wave bridge rectifier without and with filter

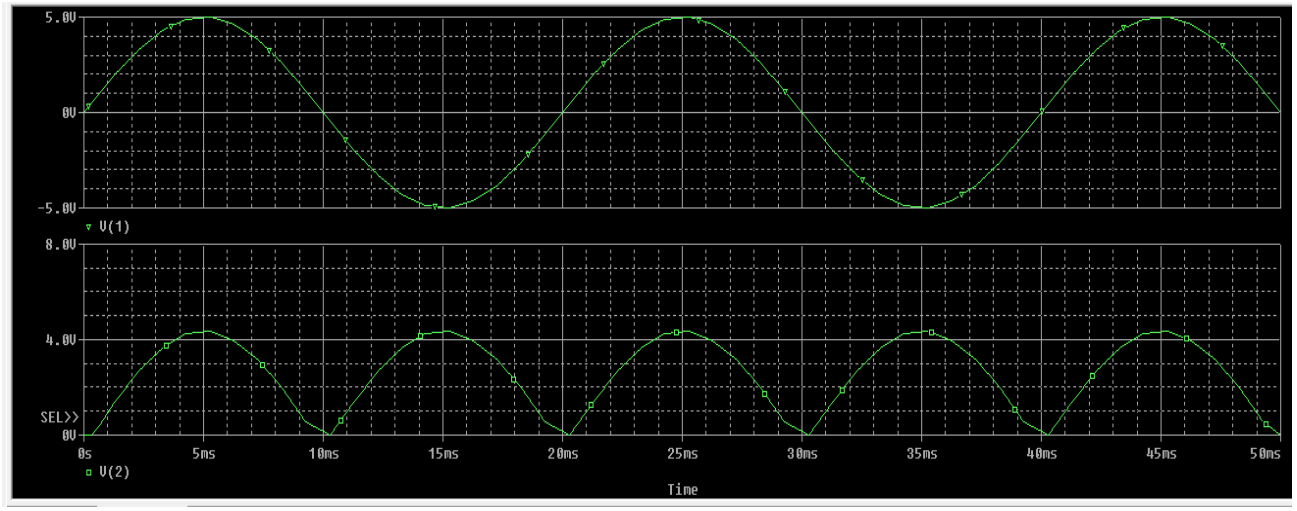
Center tapped Full wave rectifier PSPICE Program:

```
* WITHOUT FILTER
V1 1 0 sin(0 5 50)
D1 1 2 mod1
V2 0 3 sin(0 5 50)
D2 3 2 mod1
R1 0 2 10k
.MODEL mod1 D
```

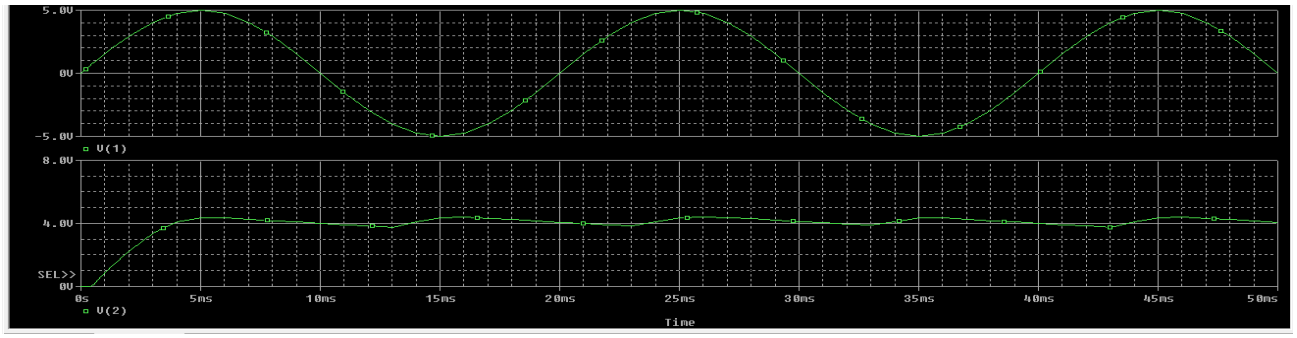
```
.TRAN 0 50ms
.PROBE
.END

* WITH FILTER
V1 1 0 sin(0 5 50)
V2 0 3 sin(0 5 50)
D1 1 2 mod1
D2 3 2 mod1
R1 0 2 10k
C1 0 2 5uf
.MODEL mod1 D
.TRAN 0 50ms
.PROBE
.END
```

Output:

WITHOUT FILTER:



WITH FILTER:



Result:

Hence the design of full wave Rectifier is simulated using OrCAD Pspice 9.1

2.a. BRIDGE RECTIFIER

Aim:

1. To observe the output waveforms of bridge rectifier without and with filter.
2. To find ripple factor and percentage regulation of bridge without and with filter.

Apparatus:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Bread board		1
2	Diodes	BY125 or IN4007	4
3	Resistor	1KΩ	1
4	Capacitor	470μF	1
5	Center tapped transformer	230V/12V	1
6	Digital multimeter/Digital voltmeter	0-20V	1
7	Cathode ray oscilloscope	0-20MHz	1
8	Connecting wires		Few

Circuit Diagram:

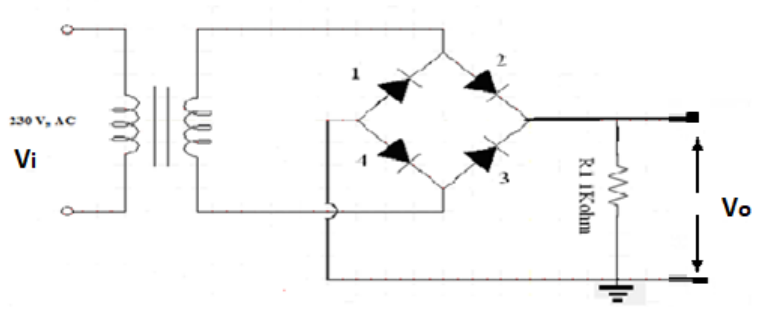


Fig 1: Full-wave bridge rectifier without filter

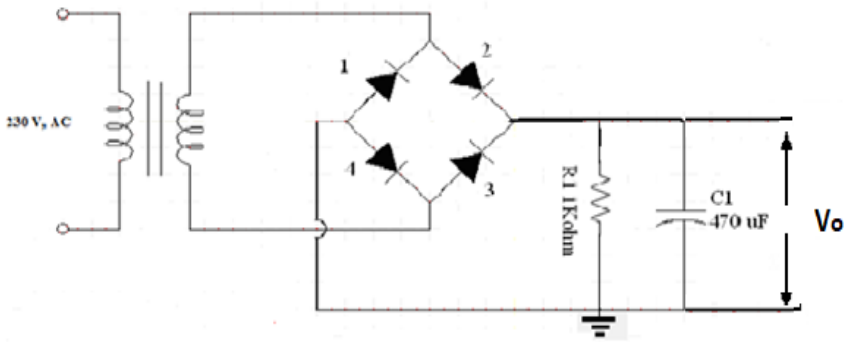


Fig 2: Full-wave bridge rectifier with filter

Theory:

The bridge rectifier consists of four diodes connected with their arrowhead symbols all pointing toward the positive output terminal of the circuit. During the positive half cycle of input voltage, the load current flows from the positive input terminal through D_1 to R_L and then through R_L and D_4 back to the negative input terminal. During this time, the positive input terminal is applied to the cathode of D_2, so it is reversed biased and similarly D_3 is also reverse biased. These two diodes are forward biased during negative half cycle; D_1 & D_4 are reverse biased during this cycle. And finally, both half cycles are rectified.

Procedure:

(a) Bridge Rectifier without filter:

1. Connect the circuit as per the circuit diagram.
2. Connect CRO across the load resistor R_1.
3. Note down the peak value V_m of the signal observed on the CRO.
4. Switch the CRO into DC mode and observe the waveform. Note down the DC shift.
5. Calculate V_{rms} and V_{dc} values by using the Equation (1) and (2):

$$V_{rms} = \frac{V_m}{\sqrt{2}}, I_{rms} = \frac{I_m}{\sqrt{2}} \quad (1)$$

$$V_{dc} = \frac{2V_m}{\pi}, I_{dc} = \frac{2I_m}{\pi} \quad (2)$$

6. Calculate the ripple factor by using the Equation (3):

$$Ripple\ factor = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} \quad (3)$$

7. Remove the load circuit (R_1 and C_1) and measure the voltage across the output terminals and represent as V_{NL}. Also note the voltage across the R_1 and C_1 and represent as V_{FL} and then calculate the percentage of voltage regulation using the Equation (4):

$$\%\ Regulation = \frac{V_{NL} - V_{FL}}{V_{FL}}\ X\ 100 \quad (4)$$

(b) Bridge Rectifier with filter:

1. Connect the capacitor filler across the load R_1 in the above circuit diagram.
2. Proceed with the same procedure mentioned above to measure the V_m value and dc shift from the CRO.
3. Calculate $V_{r,rms}$ & $V_{dcshift}$ by using the Equation (5):

$$V_{r,rms} = \frac{V_m}{2\sqrt{3}}, \quad (or) \quad V_{r,rms} = \frac{V_{dc}}{4\sqrt{3}fC_1R_1}, \tag{5}$$

Where V_m is the peak to peak amplitude of filter output.

4. Calculate ripple factor and % regulation by using Equation (6):

$$Ripple\ factor = \frac{V_{r,rms}}{V_{dcshift}}, \tag{6}$$

$$\%\ of\ Regulation = \frac{V_{NL} - V_{FL}}{V_{NL}}\ X\ 100, \tag{7}$$

Model Graph:

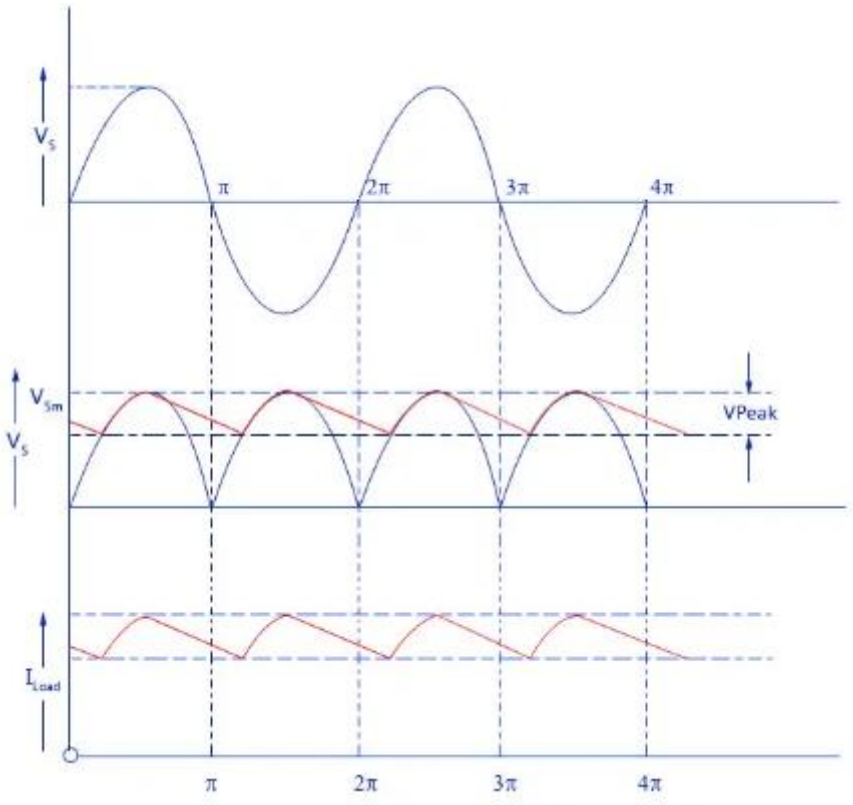


Fig 3: (a) Input Signal (b) Rectified output Waveform (c) Filtered output

Precaution:

1. Wires should be checked for good continuity.
2. Carefully note down the readings without any errors.

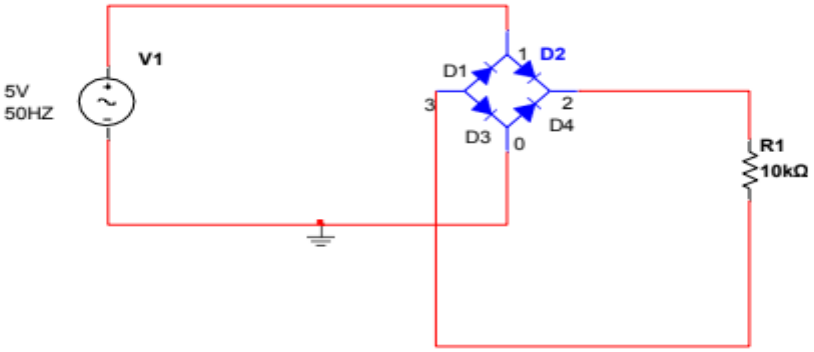
Result:

2.b. Simulation of Bridge Rectifier

Aim: To design full wave rectifier with and without filter using pspice

Software Required: OrCAD Pspice 9.1

Bridge Rectifier Circuit Diagram:
Without filter



With filter:

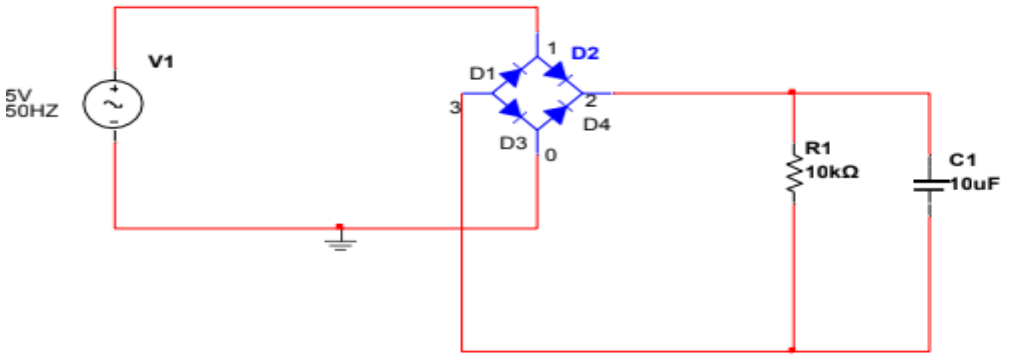


Fig 4: Full-wave bridge rectifier without and with filter

Bridge rectifier PSPICE Program:

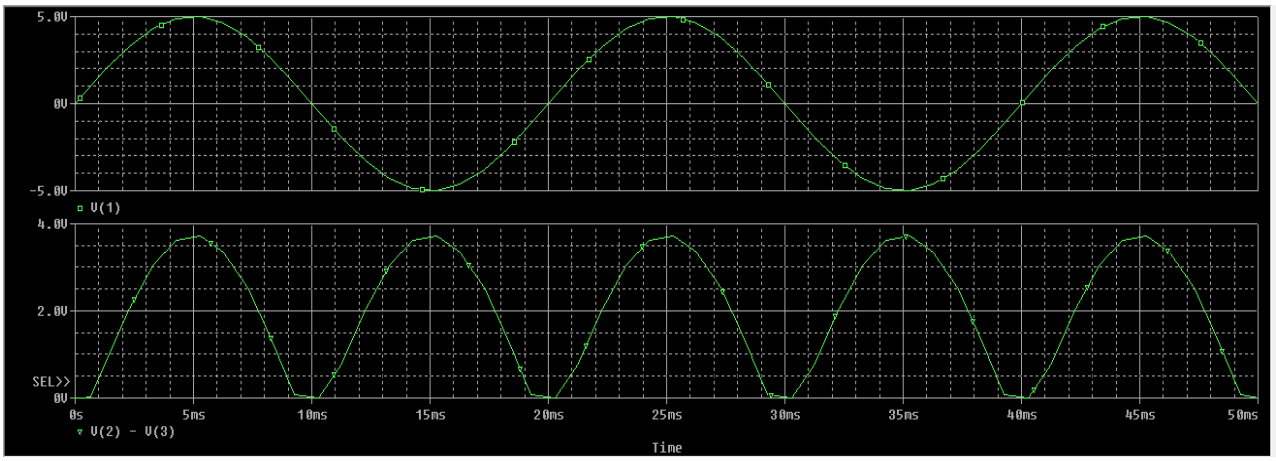
```
* WITHOUT FILTER
V1 1 0 sin(0 5 50)
D1 3 1 mod1
D2 1 2 mod1
D3 3 0 mod1
D4 0 2 mod1
R1  3 2 10k
.MODEL mod1 D
.TRAN 0 50ms
.PROBE
.END
```

```
* WITH FILTER
V1 1 0 sin(0 5 50)
D1 3 1 mod1
D2 1 2 mod1
D3 3 0 mod1
D4 0 2 mod1
R1 3 2 10k
C1 3 2 5Uf
.MODEL mod1  D
.TRAN 0 50ms
.PROBE
.END
```

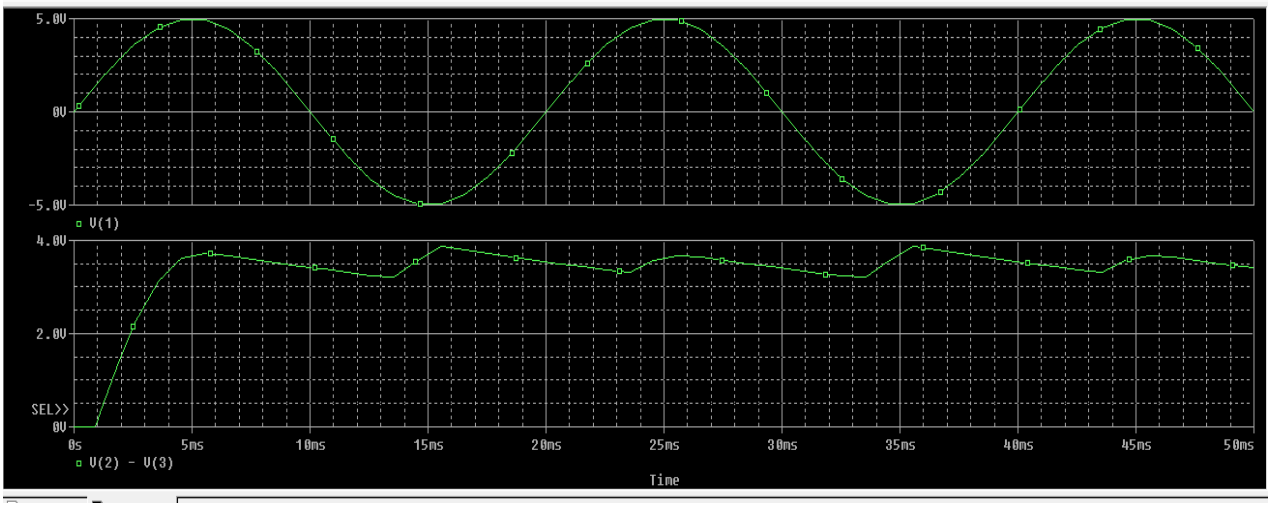
Output:

BRIDGE RECTIFIER

WITHOUT FILTER:



WITH FILTER:



Result: Hence the bridge rectifiers is simulated using OrCAD Pspice 9.1

3.a.CLIPPERS

Aim: To construct and study the operation of clipper circuits.

Apparatus Required:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Bread board		1
2	Diodes	IN4001	1
3	Resistor	4.7KΩ, 10KΩ	1 each
4	Function generator	1MHz	1
5	Digital multimeter/Digital voltmeter	0-20V	1
6	Cathode ray oscilloscope	0-20MHz	1
7	Regulated power supply	(0-30) V	1

Theory:

The basic action of a clipper circuit is to remove certain portions of the waveform, above or below certain levels as per the requirements. Thus, the circuits which are used to clip off unwanted portions of the waveform, without distorting the remaining part of the waveform are called clipper circuits or Clippers. The clipper circuits are also called limiters or slicers.

Procedure:

Clipper Circuit

1. Connect the components and apparatus as shown in the circuit diagram.

2. Set input, sinusoidal signal of 8Vp-p and 1 KHz frequency and the reference voltage as 2V using RPS.

3. Observe the output across the diode using CRO.

4. By reversing the diode in the circuit we can obtain the output of positive peak clipper.

5.Plot the input and output signal in a linear graph.

Circuit Diagram:

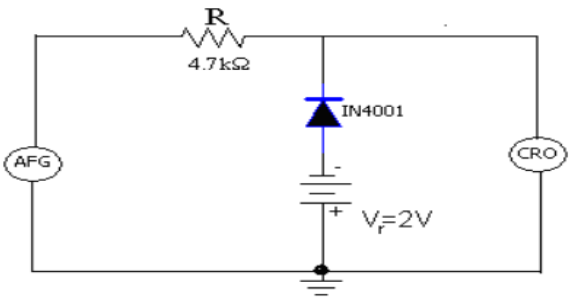


Fig 1: Negative peak clipper

Model Waveform

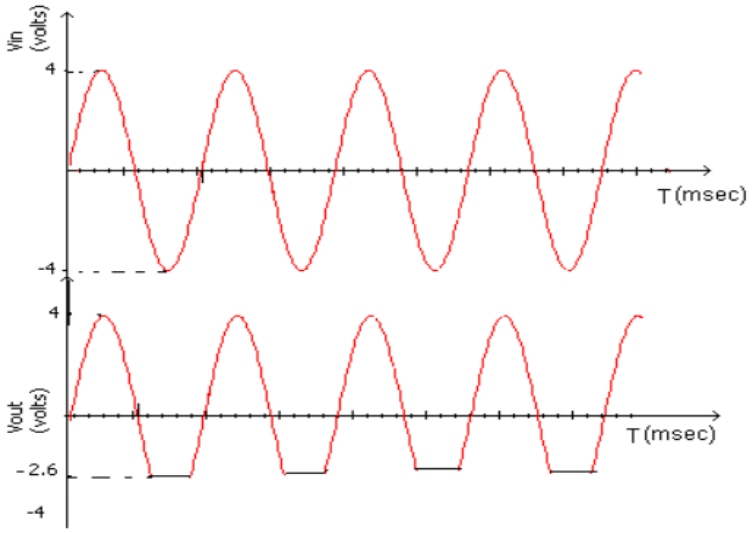


Fig 2: Input and output waveforms of negative peak clipper

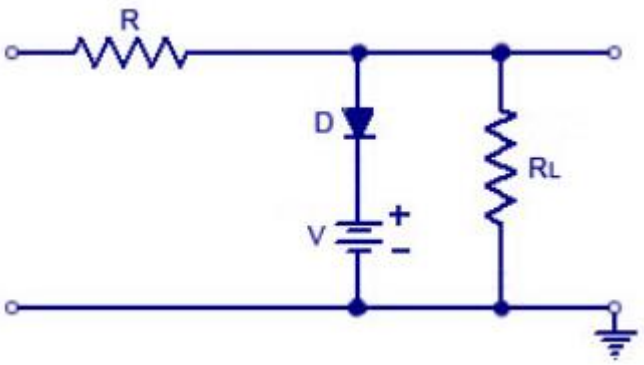


Fig 3: Positive peak clipper

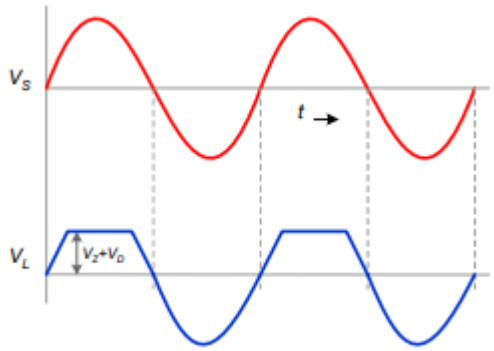


Fig 4: Input and output waveforms of positive peak clipper

Theoretical calculations:

Vr=2v, Vγ=0.6v When the diode is forward biased Vo =-(Vr+ Vγ) = -(2v+0.6v)= -2.6v When the diode is reverse biased the Vo=Vi

Result

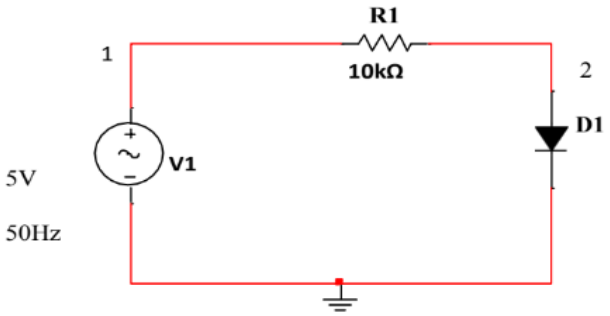
3.b Simulation of Clippers

Aim: To verify the characteristics of clippers and clampers

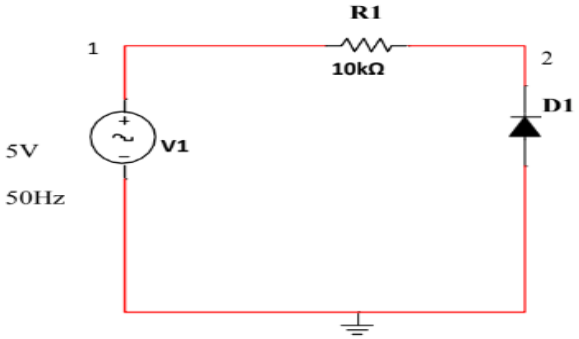
Software Required: OrcadPspice 9.1

Circuit Diagram:

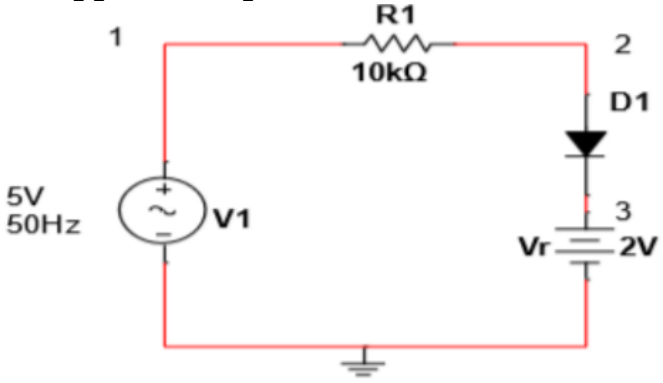
Unbiased Positive Clipper:



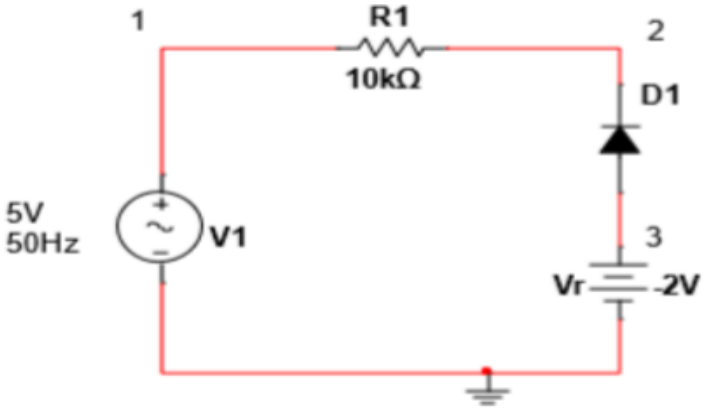
Unbiased Negative Clipper:



Biased Positive Peak Clipper with positive reference:



Biased negative Peak Clipper with negative reference



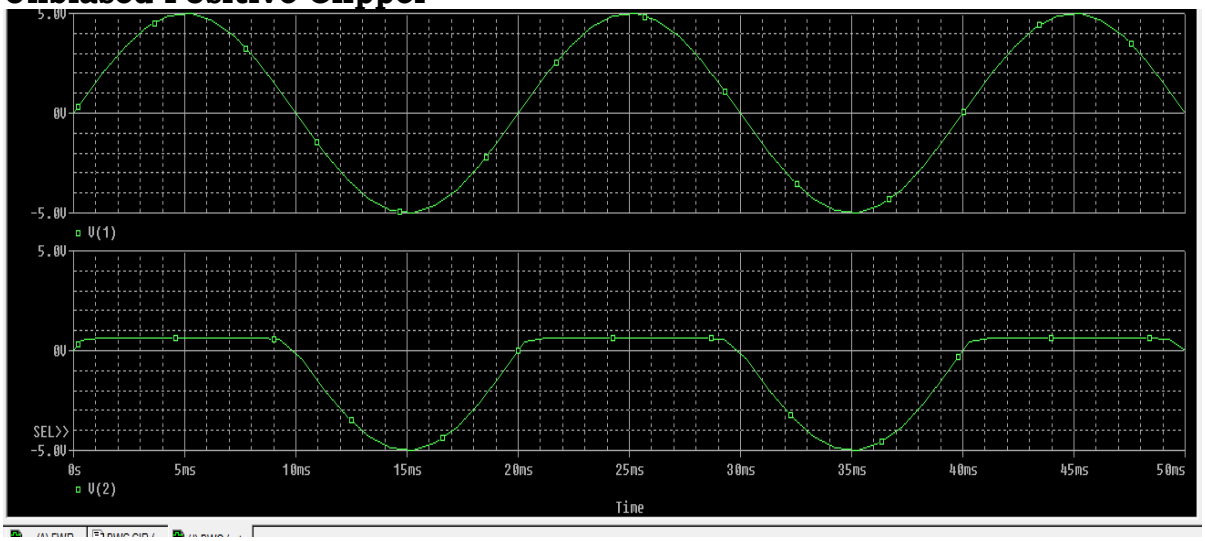
PSPICE Program:

```
*POSITIVE PEAK CLIPPER
V1 1 0 sin(0 5 50)
R 1 2 10k
D 2 0 mod1
.MODEL mod1 D
.TRAN 0 50ms
.PROBE V[1]  V[2]
.END

*NEGATIVE PEAK CLIPPER
V1 1 0 sin(0 5 50)
R1 1 2 10k
D1 0 2 mod1
.MODEL mod1 D
.TRAN 0 50ms
.PROBE V[1] V[2]
.END

*POSITIVE PEAK CLIPPER WITH POSITIVE REFERENCE
V1 1 0 sin(0 5 50)
R 1 2 10k
D 2 3 mod1
VR 3 0 2v
.MODEL mod1 D
.TRAN 0 50ms
.PROBE V[1] V[2]
.E
```

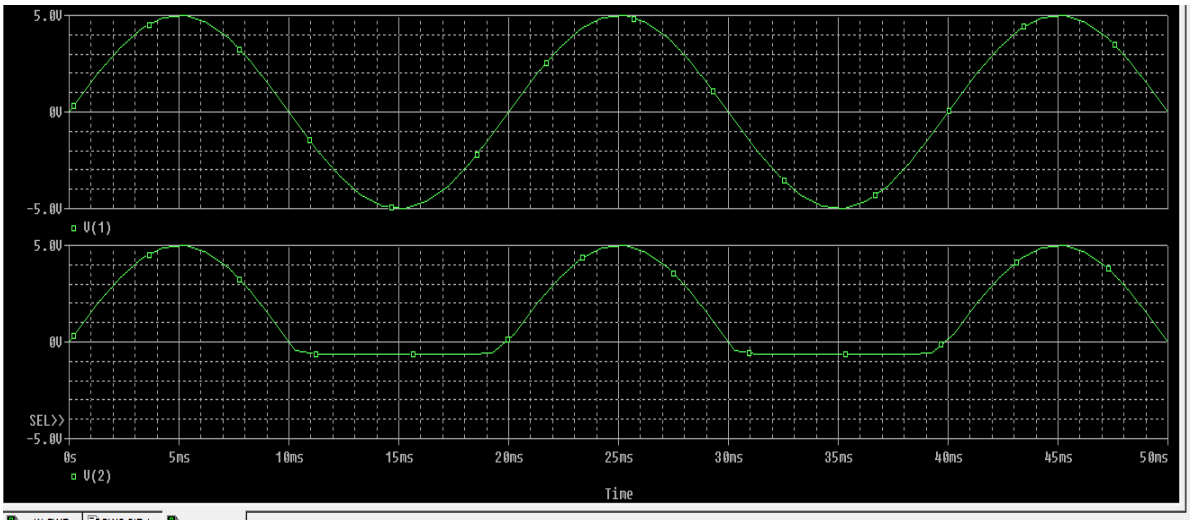
```
*NEGATIVE PEAK CLIPPER WITH NEGATIVE REFERENCE
V1 1 0 sin(0 5 50)
R1 1 2 10k
D1 3 2 mod1
VR 3 0 -2v
.MODEL mod1 D
.TRAN 0 50ms
.PROBE V[1] v[2]
.END
```

Output:

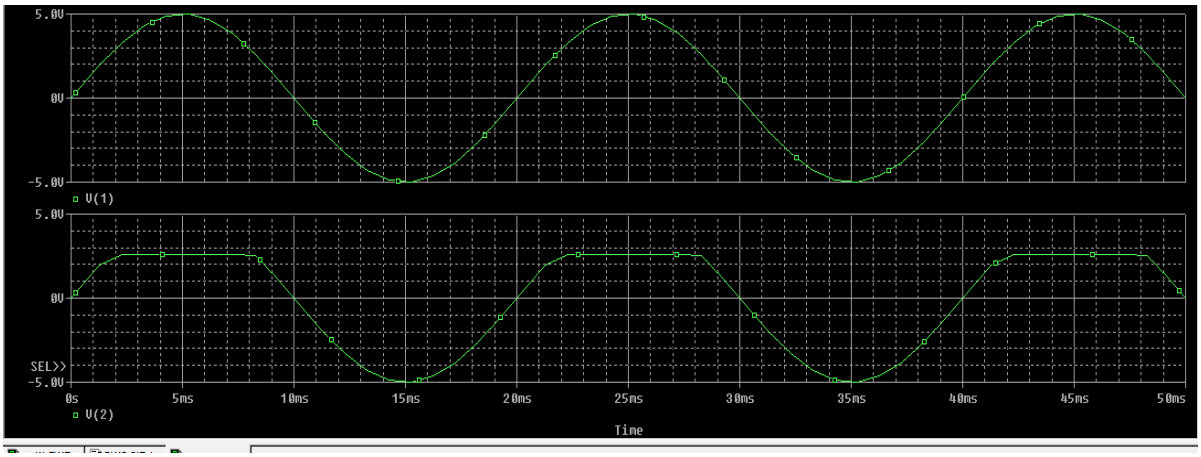
Unbiased Positive Clipper



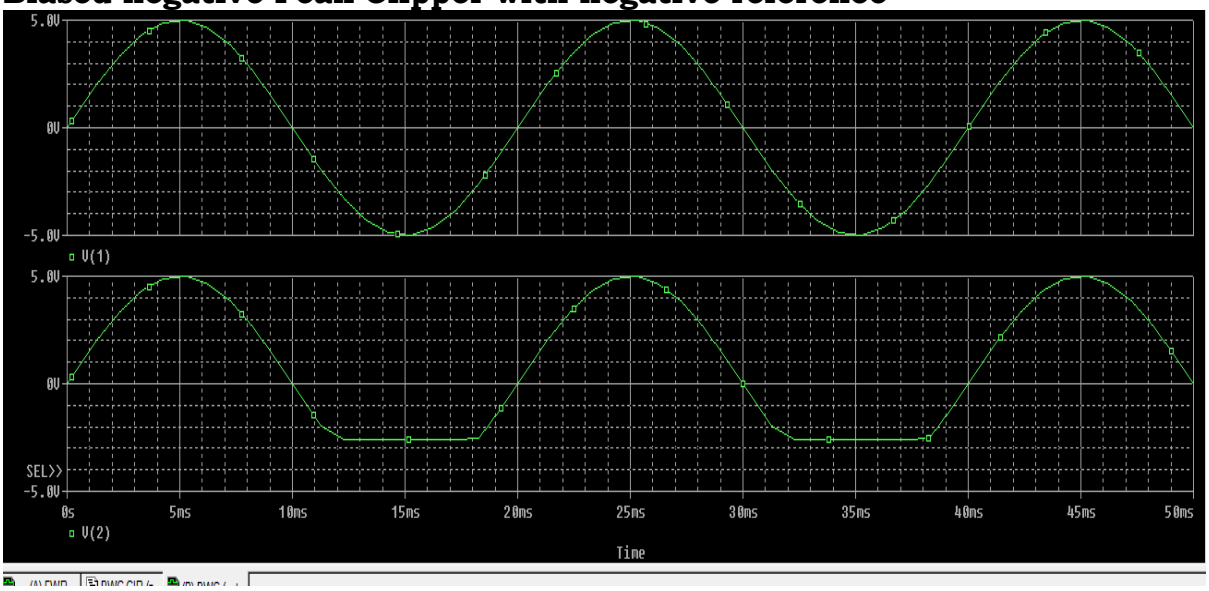
Unbiased Negative Clipper



Biased Positive Peak Clipper with positive reference



Biased negative Peak Clipper with negative reference



Result:

Hence the design of Clippers is simulated using OrCAD Pspice 9.1

4 a.CLAMPERS

Aim: To construct and study the operation of clamper circuits.

Apparatus Required:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Bread board		1
2	Diodes	IN4001	1
3	Resistor	4.7KΩ, 10KΩ	1 each
4	Capacitor	0.1μF	1
5	Function generator	1MHz	1
6	Digital multimeter/Digital voltmeter	0-20V	1
7	Cathode ray oscilloscope	0-20MHz	1
8	Regulated power supply	(0-30) V	1

Theory:

Clampers are known as *clampers* or *DC restorers*. These circuits clamp a peak of a waveform to a specific DC level compared with a capacitively coupled signal which swings about its average DC level (usually 0V). If the diode is removed from the clamper, it defaults to a simple coupling capacitor– no clamping

Procedure:

Clamper Circuit

1. Connect the components and apparatus as shown in the circuit diagram.
2. Set input, sinusoidal signal of 8Vp-p and 1kHz frequency
3. Observe the output across the load resistance using CRO.
4. Plot the input and output signal in a linear graph.

Circuit Diagram:

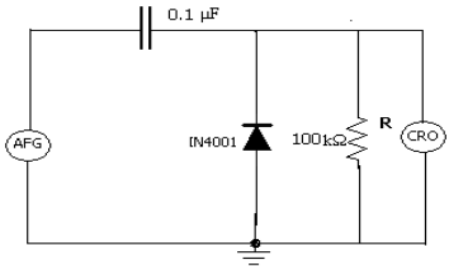


Fig 1: Positive Clamper

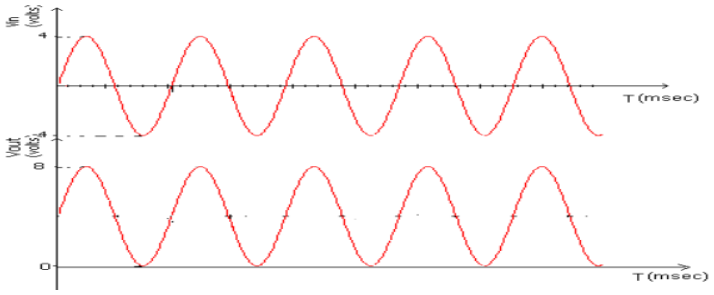


Fig 2: Input and output waveforms of positive clamper

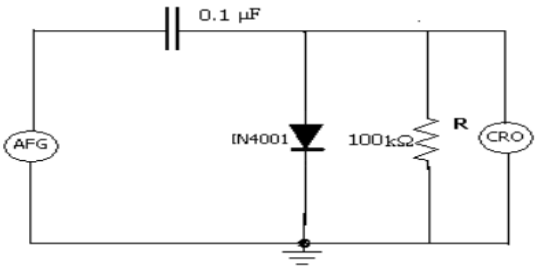


Fig 3: Negative Clamper

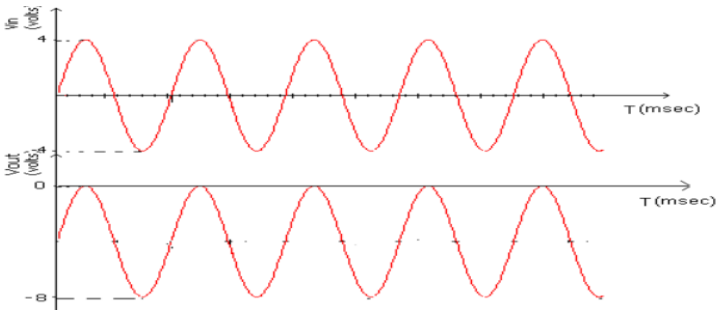


Fig 4: Input and output waveforms of positive clamper

Result

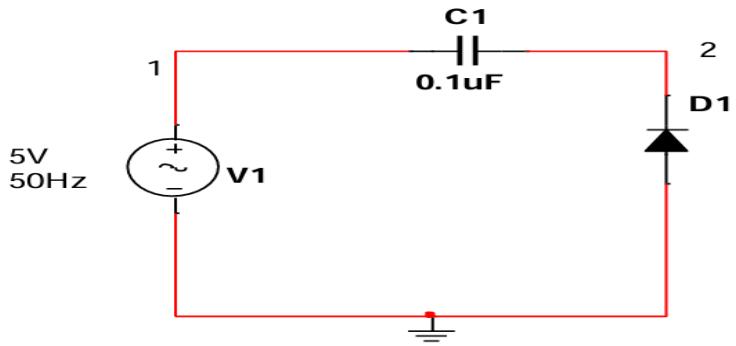
4.b Simulation of Clampers

Aim: To verify the characteristics of clampers

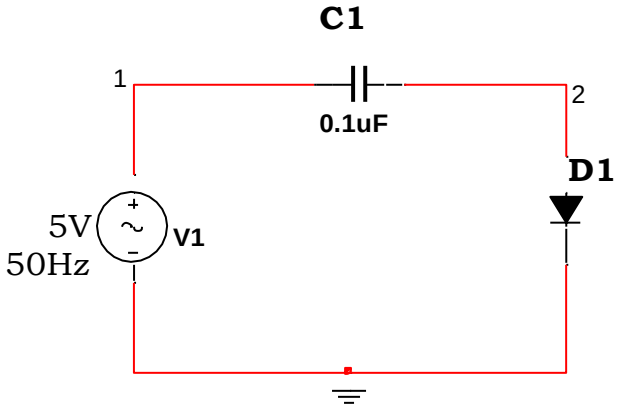
Software Required: OrCAD Pspice 9.1

Circuit Diagram:

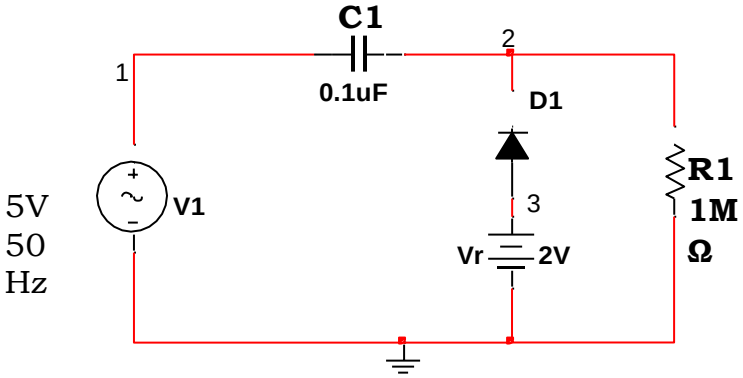
Unbiased Positive Clamper



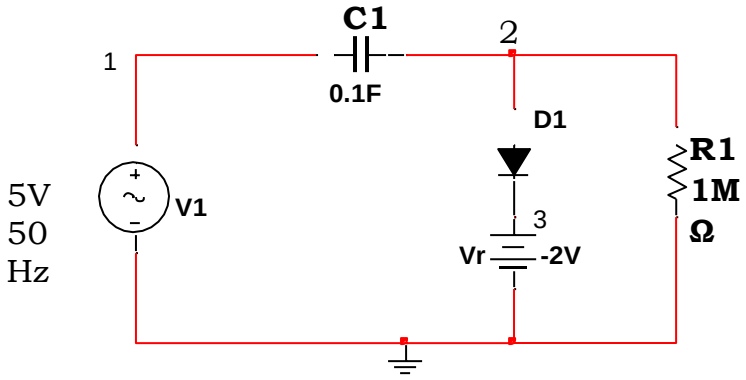
Unbiased Negative Clamper



Biased Positive Peak Clamper with positive reference



Biased negative Peak Clamper with negative reference



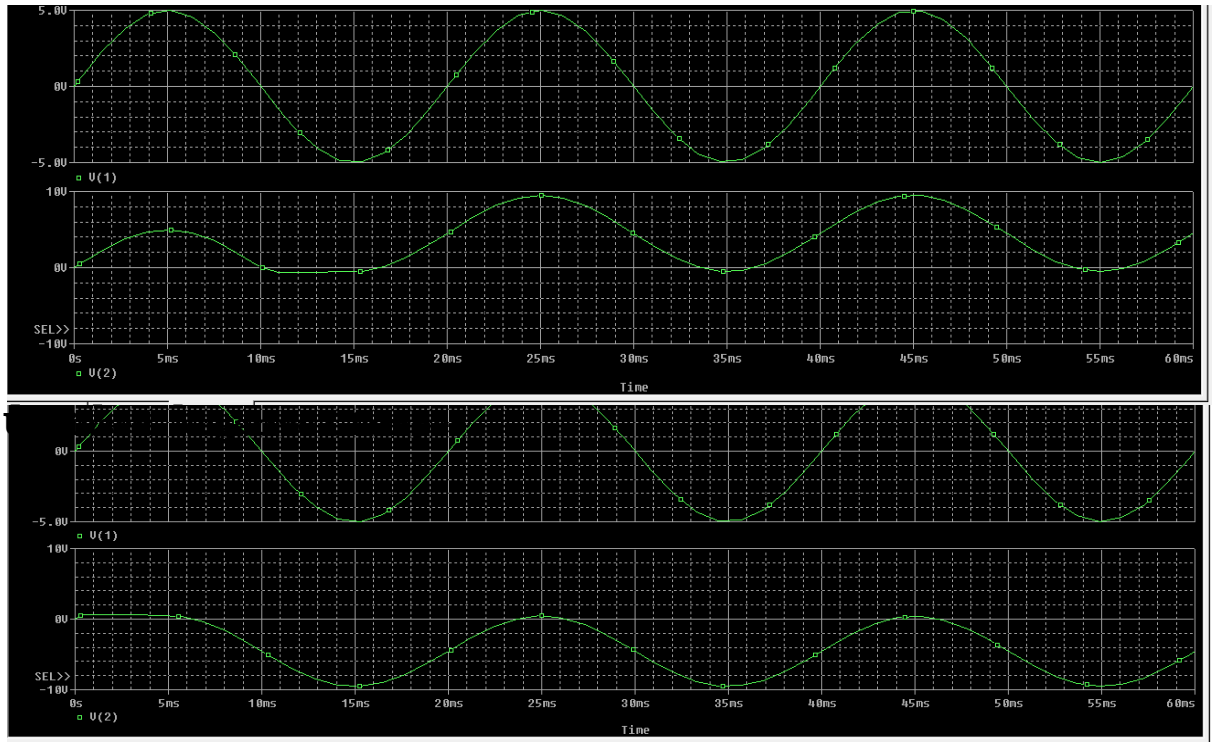
PSPICE Program:

```
*CLAMPING POSITIVE PEAK
V1 1 0 sin(0 5 50)
C1 1 2 0.1uf
D1 0 2 mod1
.MODEL mod1 D
.TRAN 0 60ms
.PROBE V[1] V[2]
.END

*CLAMPING NEGATIVE PEAK
V1 1 0 sin(0 5 50)
C1 1 2 0.1uf
D1 2 0 mod1
.MODEL mod1 D
.TRAN 0 60ms
.PROBE V[1] V[2]
.END

*POSITIVE CLAMPING WITH POSITIVE REFERENCE
V1 1 0 sin(0 5 50)
C 1 2 0.1uf
D1 3 2 mod1
VR 3 0 2V
R1 2 0 1MEG
.MODEL mod1 D
.TRAN 0 75ms
.PROBE V[1] V[2]
.END
```

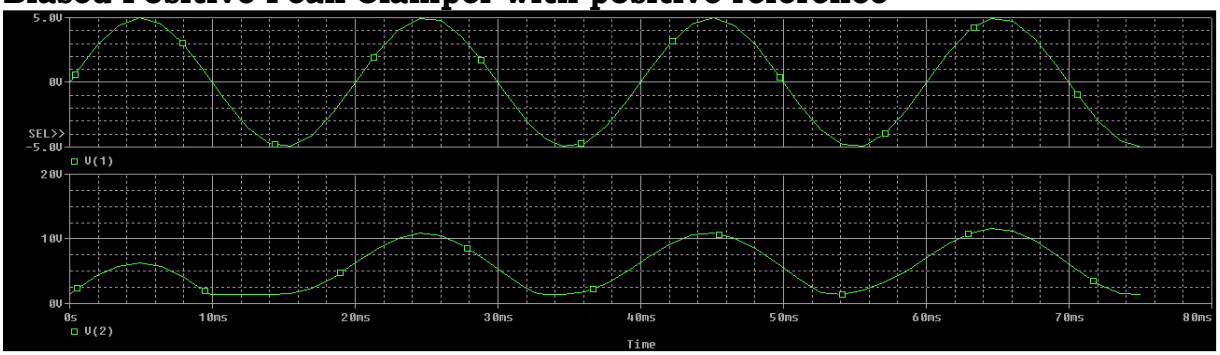
```
*NEGATIVE CLAMPING WITH NEGATIVE REFERENCE
V1 1 0 sin(0 5 50)
C1  1 2 0.1uf
D1  2 3 mod1
VR  3 0  -2V
R1 2 0 1MEG
.MODEL mod1 D
.TRAN 0 60ms
.PROBE V[1] V[2]
.END
```

Output:

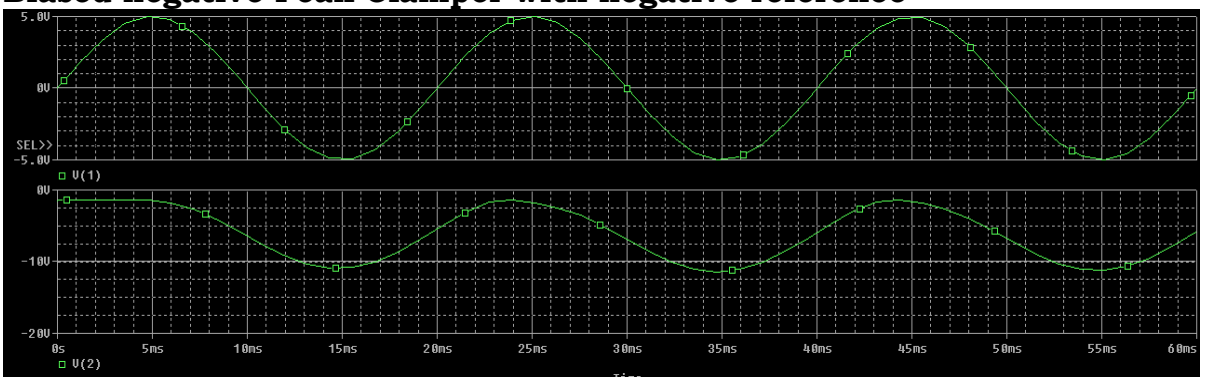
Unbiased Positive Clamper and Negative Clamper



Biased Positive Peak Clamper with positive reference



Biased negative Peak Clamper with negative reference



Result:

Hence the design of biased and unbiased clampers is simulated using OrCADPspice 9.1

5.a FREQUENCY RESPONSE OF CE AMPLIFIER

Aim:

To study the frequency response of a common emitter (CE) amplifier and to find its voltage gain and bandwidth.

Apparatus:

S.No.	Components and Equipment	Quantity
1	Bread Board	1
2	Transistor (BC547 or BC107)	1
3	Resistors (47KΩ, 10KΩ, 1KΩ, 220Ω, 100Ω)	1 (each one)
4	Capacitors (10μF)	2
5	Regulated Power Supply(0-30V)	1
6	Digital Storage Oscilloscope(0-20MHz)	1
7	Function Generator (0-5MHz)	1
8	Connecting Wires	Few

Circuit Diagram:

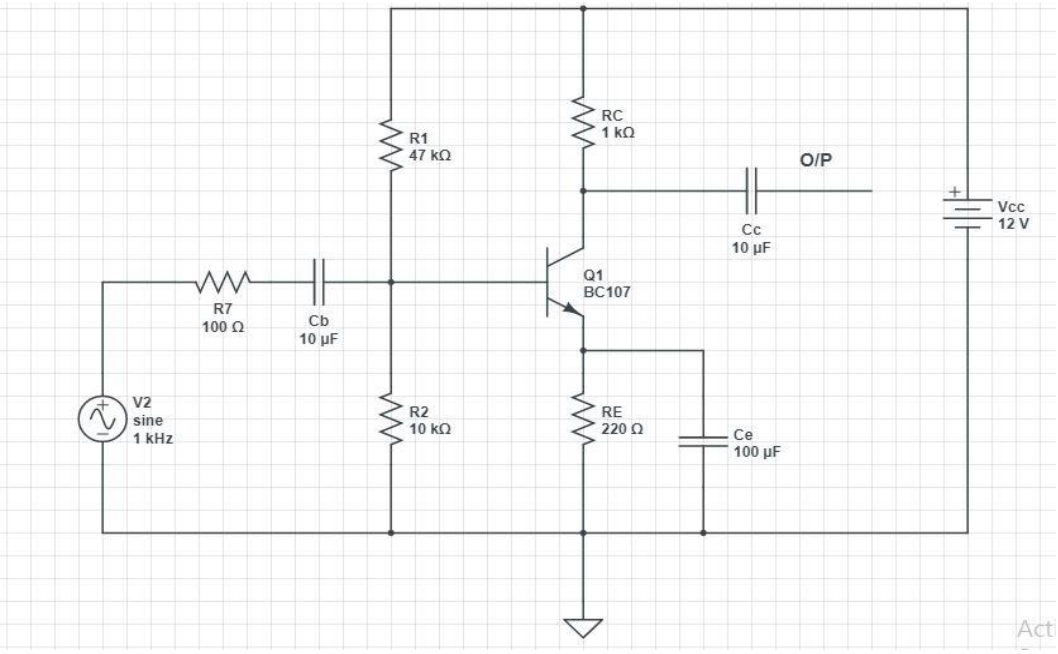


Fig 1: CE Amplifier

Theory:

The CE amplifier is a small signal amplifier. This small signal amplifier accepts low voltage ac inputs and produces amplified outputs. A single stage BJT circuit may be employed as a small signal amplifier; has two cascaded stages give much more amplification.

Designing for a particular voltage gain requires the use of ac negative feedback to stabilize the gain. For good bias stability, the emitter resistor voltage drop should be much larger than the base-emitter voltage. And R_e resistor will provide the required negative feedback to the circuit. C_E is provided to provide necessary gain to the circuit. All bypass capacitors should be selected to have the smallest possible capacitance value, both to minimize the physical size of the circuit for economy. The coupling capacitors should have a negligible effect on the frequency response of the circuit.

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Give l00Hz sinusoidal signal with 20mV(p-p) amplitude (V_i) from the signal generator.
3. Observe the output on CRO and note down the output voltage.
4. Keeping input voltage constant (i.e. 20mV) and by varying the frequency in steps from 100Hz to 1MHz, note down the corresponding output voltages.
5. Calculate the gain in dB and plot the frequency response on semi log graph.
6. Calculate the bandwidth from lower and higher cut-off frequencies.

Tabular Form:

Input voltage (V_i)=20mV(p-p)

S.No	Frequency (Hz)	Output Voltage (V_o)	Gain Av=Vo/Vi	Gain in (dB)

Model Graph:

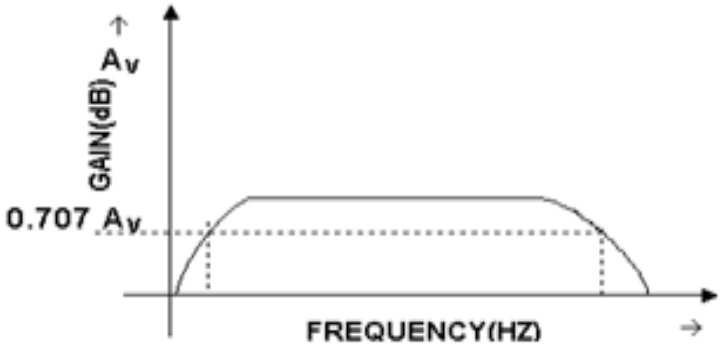


Fig 2: Frequency response of CE Amplifier

Precautions:

1.Wires should be checked for good continuity.

2.Transistor terminals must be identified and connected carefully.

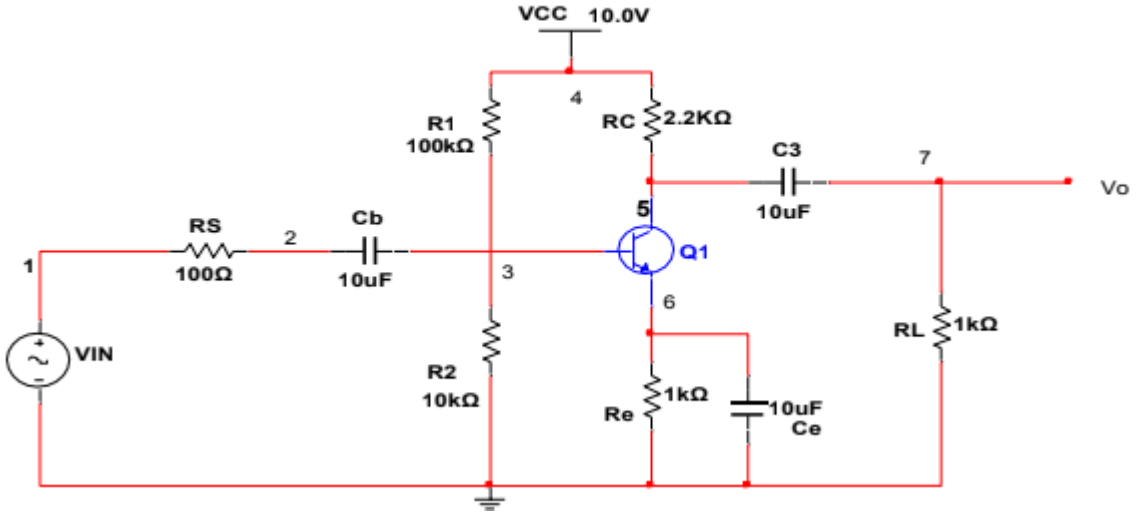
Result:

5.b Simulation of Frequency response of CE Amplifier

Aim: To verify the characteristics and frequency response of CE Amplifier

Software Required: Orcad Pspice 9.1

Circuit Diagram:

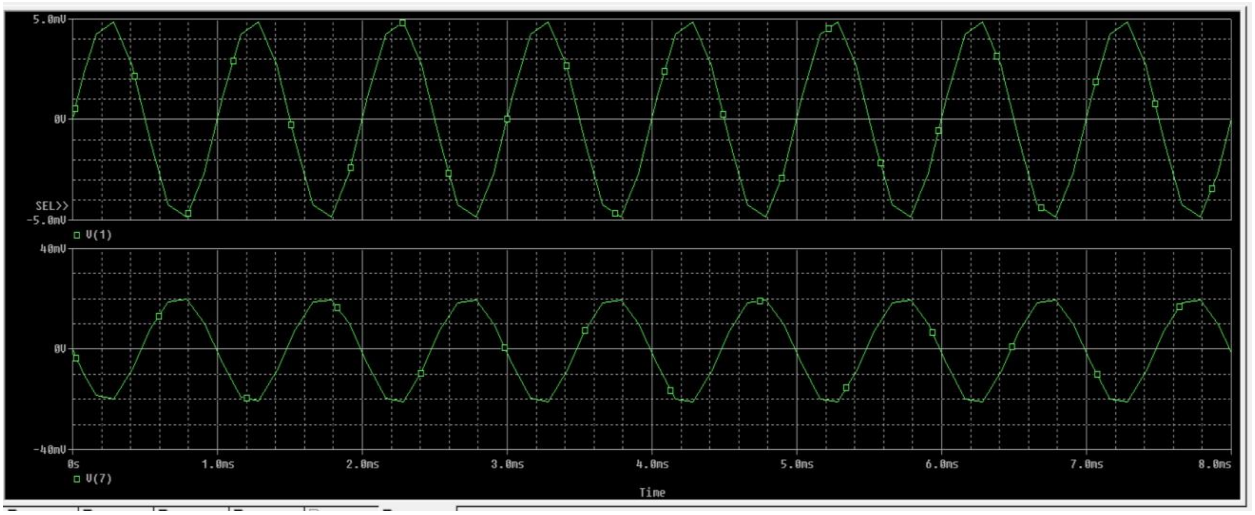


PSPICE Program:

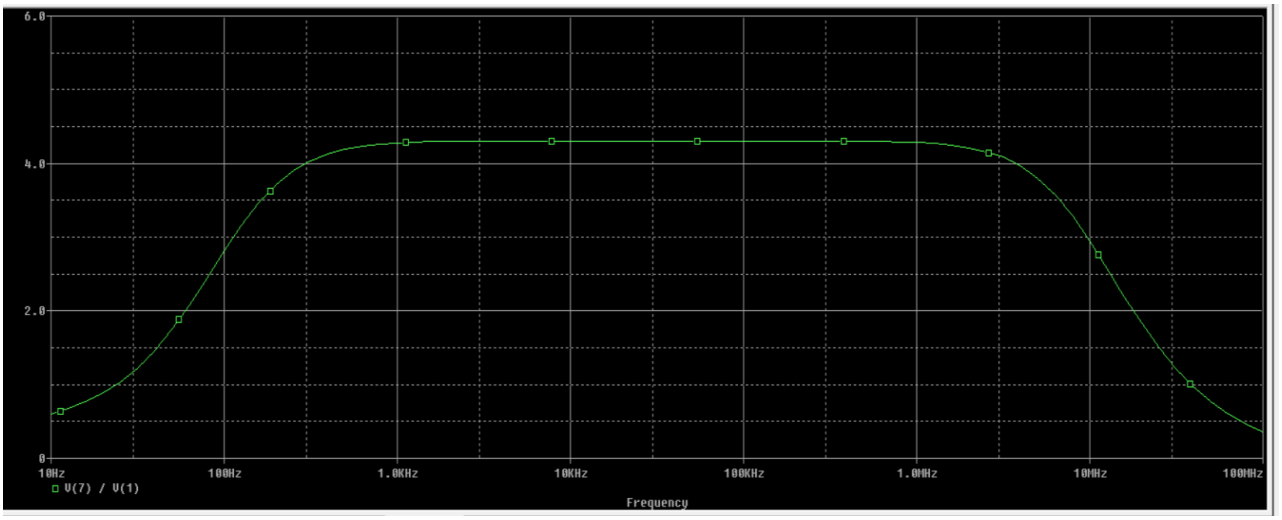
```
*CE AMPLIFIER
Vin 1 0 AC 5mV  SIN(0 5m 1K)
Rs 1 2 100
R1 3 4 100K
R2 3 0 10K
RC 4 5 2.2K
RE 6 0 1K
RL 7 0 1K
Cb 2 3 10U
Ce 6 0 10U
Cc 5 7 10U
 Vcc 4 0 10v
Q1 5 3 6 MOD1
.MODEL MOD1 NPN(Cjc=80PF,Cje=3PF)
.AC DEC 10 10 100MEG
.TRAN 0 8m
.PROBE
.END
```

Output:

COMMON EMITTER AMPLIFIER TRANSIENT ANALYSIS



COMMON EMITTER AMPLIFIER AC ANALYSIS



Result:

Hence the design of CE Amplifier is simulated using OrCAD PSPICE 9.1and their characteristics were observed.

6.a FREQUENCY RESPONSE OF CS AMPLIFIER

Aim:

To find the voltage gain of a common source (CS) amplifier and to find its frequency response.

Apparatus:

S.No.	Components and Equipment's	Quantity
1	Bread Board	1
2	Transistor (FET BFW10)	1
3	Resistors (1MΩ, 1KΩ, 2.2KΩ, 100Ω)	1(each one)
4	Capacitors (10μF, 100μF)	2&1(respectively)
5	Regulated Power Supply (0-30V)	1
6	Cathode Ray Oscilloscope (0-20MHz)	1
7	Function Generator (0-5MHz)	1
8	Connecting Wires	Few

Circuit Diagram:

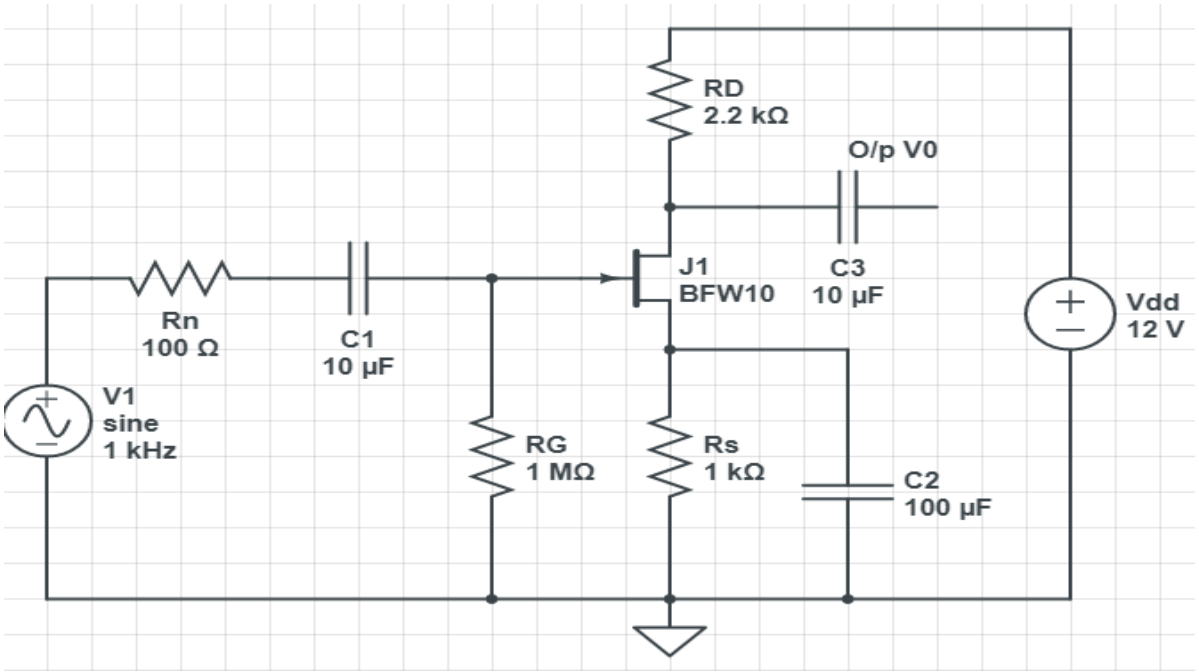


Fig 1: CS Amplifier

Theory:

The CS amplifier is a small signal amplifier. For good bias stability, the source resistor voltage drop should be as large as possible. Where the supply voltage is small, Vs may be reduced to a minimum to allow for the minimum level of Vds.R2 is usually selected as 1MΩ or less as for BJT capacitor coupled circuit, coupling and bypass capacitors should be selected to have the smallest possible capacitance values. The largest capacitor in the circuit sets the circuit low 3dB frequency (capacitor C2). Generally, to have high input impedance FET is used. As in BJT circuit RL is usually much larger than Zo and Zi is often much larger than Rs.

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Give 100 Hz sinusoidal signal and 50 mV (P-P) as V_i from signal generator.
3. Observe the output on CRO for proper working of the amplifier.
4. After ensuring the amplifier function, vary signal frequency in steps from 10 Hz to 1MHz.
5. Keeping the V_i constant at 20mV(P-P) at every frequency, note down the output voltage and tabulate in a table.
6. Calculate gain in dB and plot the graph between gain(dB) and frequency.

Tabular Form: Input Voltage =20mV(p-p)

S.No	Frequency (Hz)	Output Voltage (V_o)	Gain Av=Vo/Vi	Gain in (dB)

Model Graph:

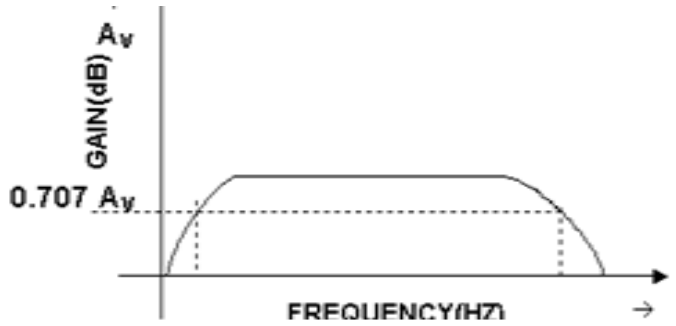


Fig 2: Frequency response of CS Amplifier

Precautions:

1.Wires should be checked for good continuity.
2.FET terminals must be identified and connected carefully.

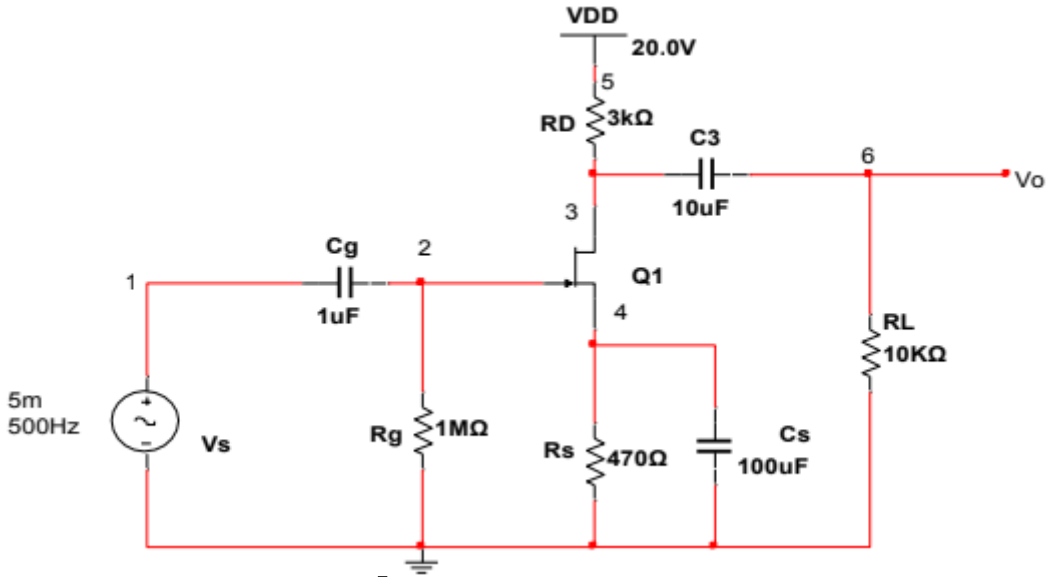
Result:

6.b Simulation of Frequency response of CS Amplifier

Aim: To verify the characteristics of CS Amplifier

Software Required: Orcad Pspice 9.1

Circuit Diagram:

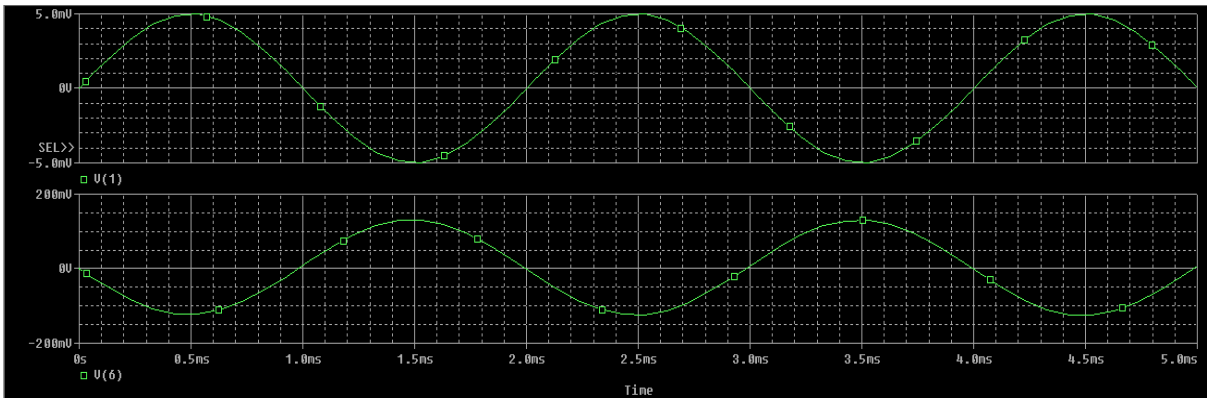


PSPICE Program:

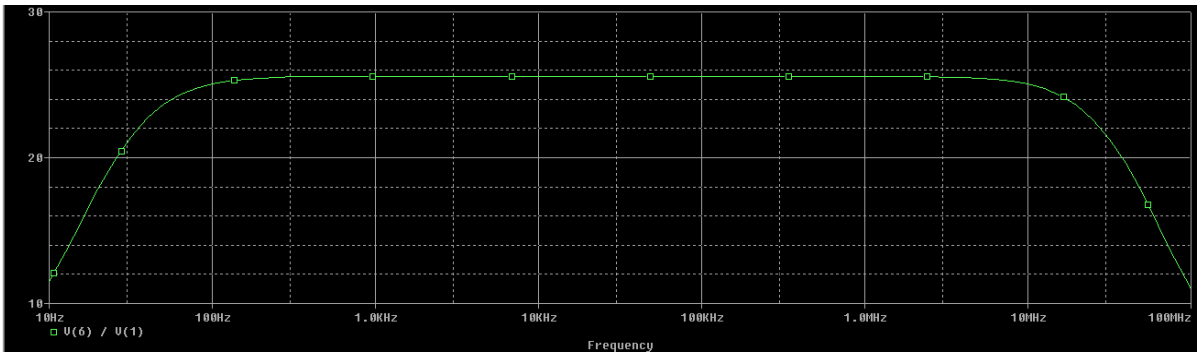
```
*CS AMPLIFIER
Vs 1 0 AC 5MV SIN(0 5m 500)
VDD 5 0 20V
Rg 2 0 1MEG
Rs 4 0 470
RL 6 0 10K
Rd 3 5 3K
Cs 4 0 100UF
Cd 3 6 10UF
Cg 1 2 1UF
J 3 2 4 MOD1
.MODEL MOD1 NJF(Cgs=5PF,Cgd=5PF,Beta=0.01)
.TRAN 0 5MS
.AC DEC 10 10 100MEG
.PROBE
.END
```

Output:

COMMON SOURCE AMPLIFIER TRANSIENT ANALYSIS



COMMON SOURCE AMPLIFIER AC ANALYSIS



Result:

Hence the design of CS Amplifier is simulated using OrCAD Pspice 9.1 and their characteristics was observed

7.a. FREQUENCY RESPONSE OF TWO-STAGE RC COUPLED AMPLIFIER

Aim:

To obtain the frequency response of' a two stage RC coupled amplifier.

Apparatus:

S.No.	Components and Equipment	Quantity
1	Bread Board	1
2	Transistor (BJT BC107)	2
3	Resistors 10KΩ 47KΩ 470Ω 2.2KΩ 680Ω	 2 2 2 2
4	Capacitors: 22μF 33μF	 3 2
5	Regulated Power Supply(0-30V)	1
6	Cathode Ray Oscilloscope(0-20MHz)	1
7	Function Generator(0-5MHz)	1
8	Digital Multimeter	1
9	Connecting Wires	

Circuit Diagram:

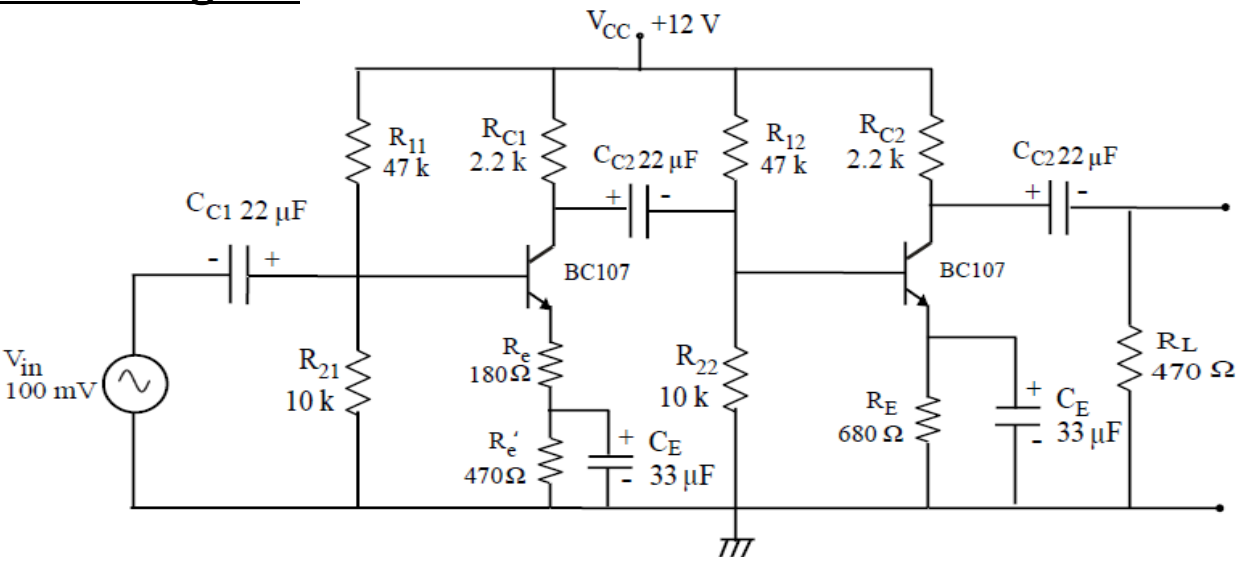


Fig 1: Two stage RC Coupled Amplifier

Theory:

The output from a single stage amplifier is usually insufficient to drive an output device. To achieve more gain, the output of one stage is given as the input to the other stage which forms multistage amplifier. If the two stages are coupled by R and C, then the amplifier is called RC-coupled amplifier. The performance of an amplifier can be determined from the following terms**.**

Gain:

The gain is defined as ratio of output to input. The gain of multistage amplifier is equal to the product of gains of individual stages i.e $G=G_1.G_2.G_3$.

Frequency Response:

At low frequencies (<50Hz) the reactance of coupling capacitor C_c is high, and hence very small part of signal will pass from one stage to next stage. This increases the loading effect of next stage and reduces the voltage gain. At high frequencies, capacitance reduces. Due to this base emitter junction is low which increases the base current. This reduces the amplification factor. At mid frequencies, the voltage gain of the amplifier is constant. In this range, as frequency increases, reactance of C_c reduces which tends to increase the gain. At the same time, lower reactance means higher reactance of first stage and lower gain, these two factors cancel each other resulting in a uniform gain at mid frequency.

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Give 1 KHz sinusoidal signal with 25 mV (p-p) amplitude as V_i from signal generator.
3. Observe the output on CRO for proper working of the amplifier.
4. After ensuring the amplifier action, Vary the input signal frequency from 100Hz to 1MHz in steps up to 15 to 20 readings with input signal amplitude V_{in} = 20mVp-p.
5. Calculate gain in dB and plot the graph between frequency and gain dB on semi-log graph paper.

Model Graphs:

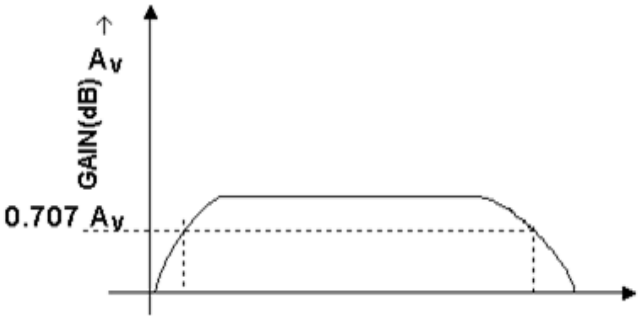


Fig 2: Frequency response of two stage RC coupled Amplifier

Tabular Form: Input Voltage =25mV(p-p)

S.No	Frequency (Hz)	Output Voltage (V_o)	Gain Av=Vo/Vi	Gain in (dB)

Precautions:

1.Wires should be checked for good continuity.
2.Transistor terminals must be identified and connected carefully.

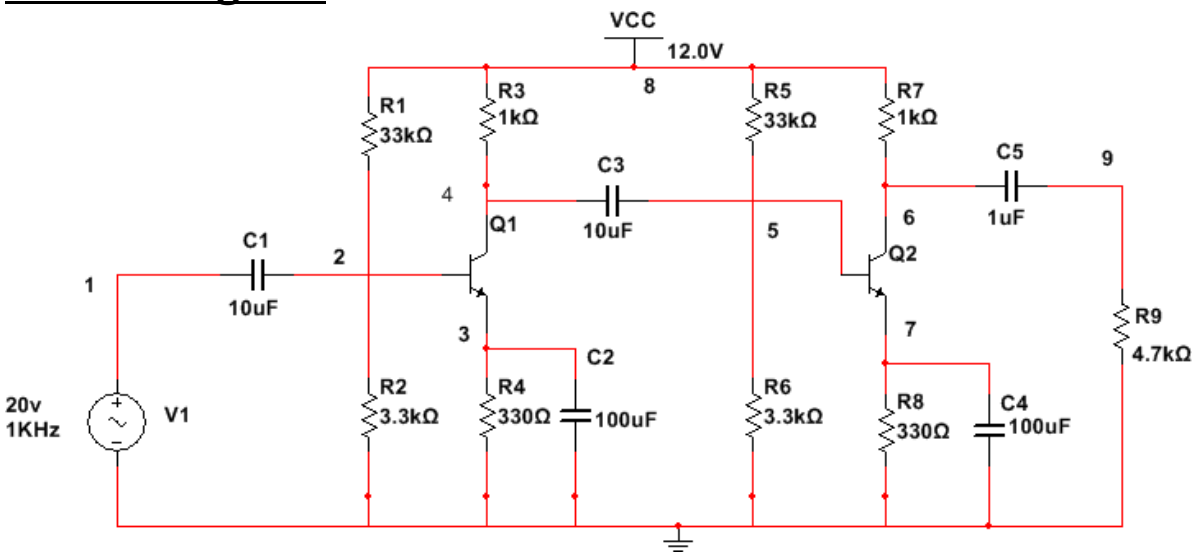
Result:

7.b Simulation of Frequency response of two stage RC coupled Amplifier

Aim: To verify the characteristics of RC Coupled Amplifier

Software Required: OrCAD Pspice 9.1

Circuit Diagram:



PSPICE Program:

*RC COUPLED AMPLIFIER

V1 1 0 AC 5MV SIN(0 50M

5K)R1 1 8 33k

R2 2 0 3.3k

R3 4 8 1k

R4 3 0 330

R5 5 8 33k

R6 5 0 3.3K

R7 6 8 1k

R8 7 0 330

R9 9 0 4.7k

C1 1 2 10UF

C2 3 0 100UF

C3 4 5 10UF

C4 7 0 100UF

C5 6 9 10UF

Q1 4 2 3 MOD1

Q2 6 5 7 MOD1

VCC 8 0 12V

.MODEL MOD1 NPN

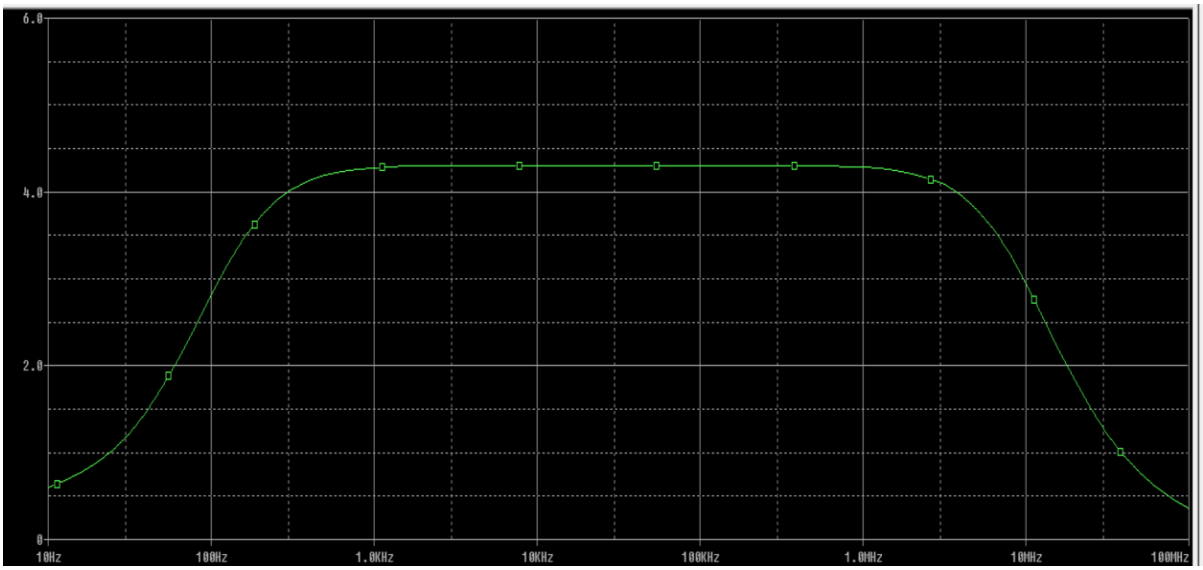
.TRAN 0 5m

.AC DEC 10 10 1000MEG

.PROBE

.END

Output:



Result:

Hence the design of RC coupled Amplifier is simulated using OrCAD PSPICE 9.1 and their characteristics were observed.

8.a. CLASS-A POWER AMPLIFIER.

Aim:

To construct a Class A power amplifier and observe the waveform and to compute maximum output power and efficiency.

Apparatus Required:

S.No.	Components and Equipment	Quantity
1	Transistor SL100	1
2	Resistor (47KΩ, 330Ω, 2.2KΩ)	2,1
3	Capacitor(47µF)	2
4	Signal Generator(0-3MHz)	1
5	CRO(30MHz)	1
6	Regulated power supply(0-30V)	1
7	Bread Board	1

Circuit Diagram:

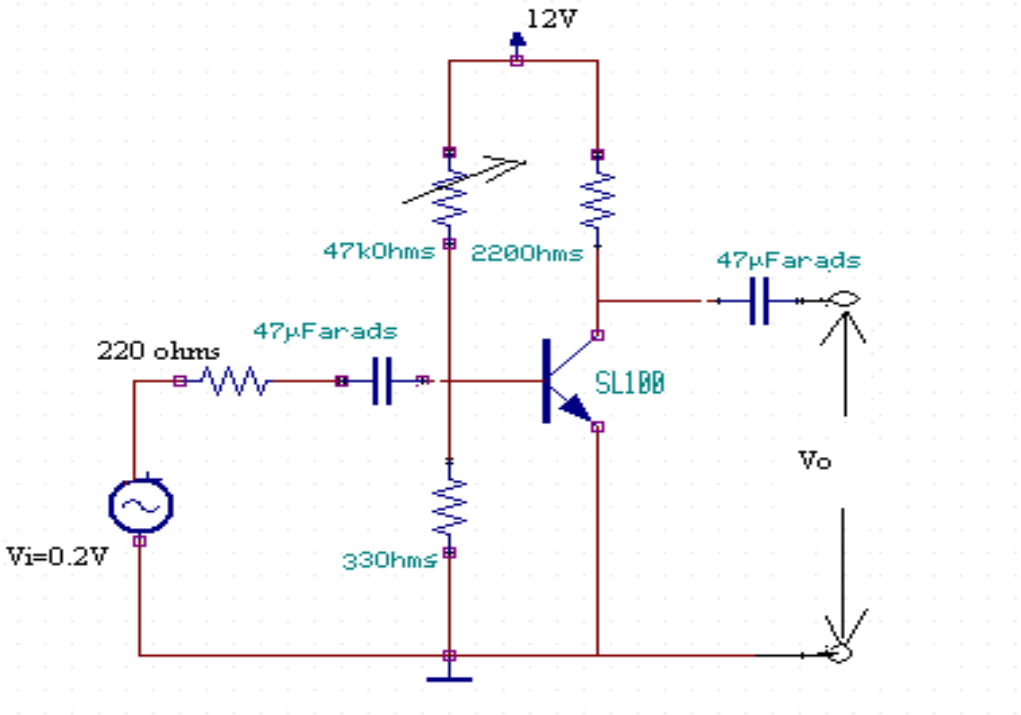


Fig 1: Class A power Amplifier

Theory:

The power amplifier is said to be Class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input signal cycle.

For all values of input signal, the transistor remains in the active region and

never enters into cut-off or saturation region. When an a.c signal is applied, the collector voltage varies sinusoidally, hence the collector current also varies sinusoidally. The collector current flows for 360^0 (full cycle) of the input signal. i.e., the angle of the collector current flow is 360^0 .

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set V_i =200 mV, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 1 kHz to 1M Hz regular steps and observe the corresponding output voltages.
3. At a particular frequency of input signal, the output may be clipped. Then note down the corresponding output voltage.
4. Otherwise keep the input signal at 10 kHz and increase the amplitude. At a particular amplitude of input signal the output may be clipped. Then stop and note down the corresponding output signal amplitude.

Calculations:

output voltage (V_0) =

Maximum output power = $P_o,max = V_o^2/R_L$

Keep the input voltage constant, V_{in} = 200mV

P_{in} =

Effeciency, $\eta = P_{o,max} / P_{in}$

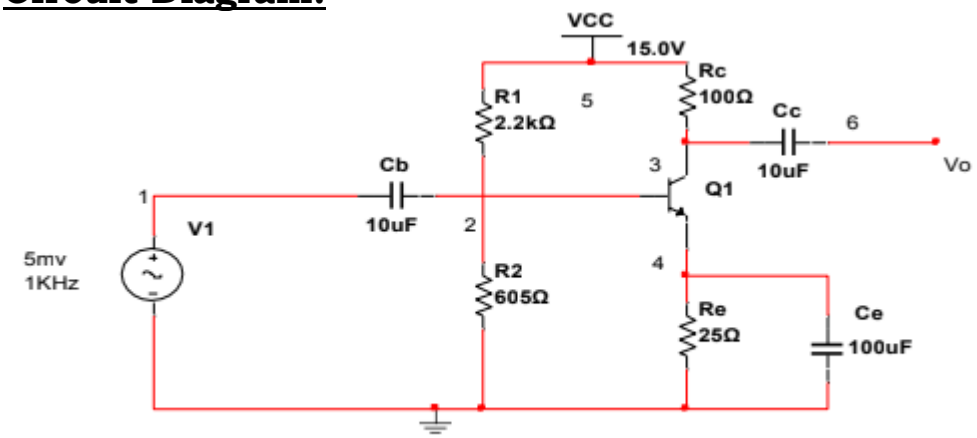
Result:

8.b Simulation of Class A power amplifier

Aim: To verify the characteristics of CLASS A Power Amplifier

Software Required: Orcad Pspice 9.1

Circuit Diagram:

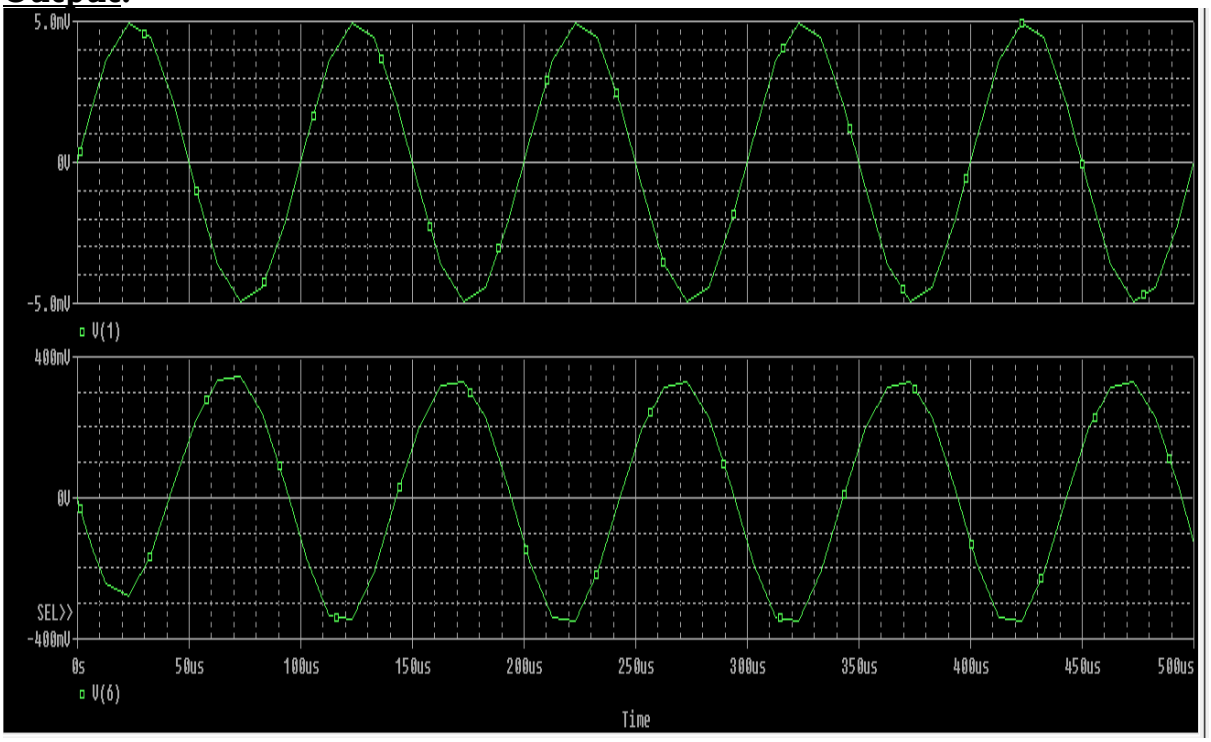


PSPICE Program:

*CLASS -A AMPLIFIER

VS 1 0 SIN(0 5MV 10KHZ)
VCC 5 0 15V
CB 1 2 10UF
CC 3 6 10UF
CE 4 0 100UF
R1 5 2 2.7K
R2 2 0 605
RC 5 3 100
RE 4 0 25
RL 6 0 47
Q1 3 2 4 SL100
.MODEL SL100 NPN
.TRAN 0.1MS 0.5MS
.PROBE
.END

Output:



Result:

Hence the design of Class-A power Amplifier is simulated using OrCAD Pspice 9.1 and their characteristics was observed.

9. COMPLEMENTARY SYMMETRY PUSH-PULL AMPLIFIER.

Aim:

To construct a Class B complementary symmetry power amplifier and observe the waveforms with and without cross-over distortion and to compute maximum output power and efficiency.

Apparatus Required:

S.No	Components and Equipment	Quantity
1	Transistors CL100 ,BC 558	1,1
2	Resistor (4.7KΩ, 15KΩ)	2,1
3	Capacitor(100μF)	2
4	Signal Generator (0-3MHz)	1
5	CRO (0-20MHz)	1
6	Regulated power supply (0- 30V)	1
7	Bread Board	1

Circuit Diagram

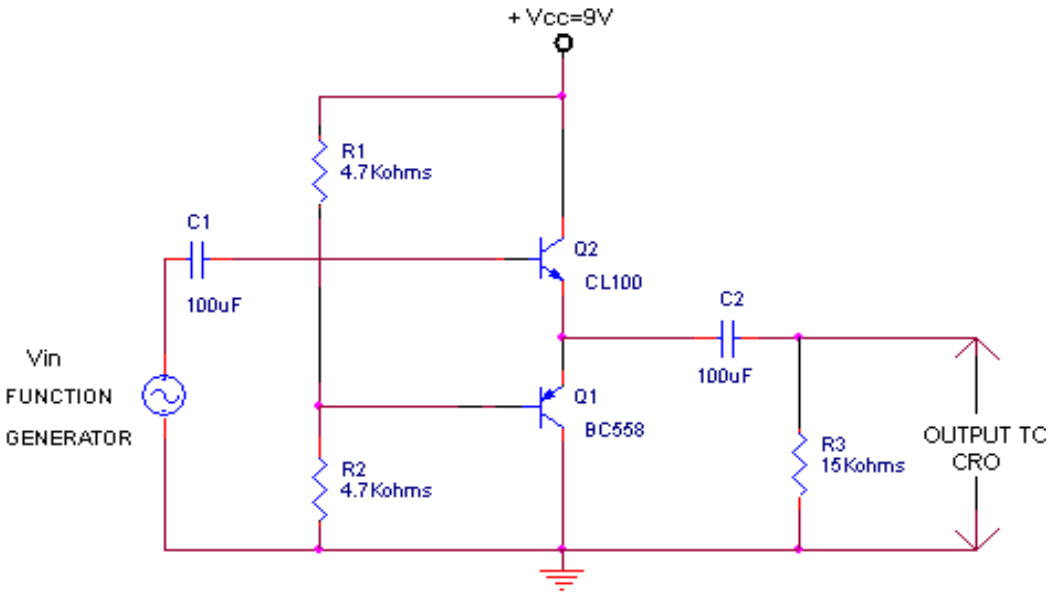


Fig 1: Complementary Symmetry Push-pull amplifier.

FORMULA:

Input power, $P_{in}=2V_{cc}I_m/\Pi$

Output power, $P_{out}=V_mI_m/2$

Power Gain or efficiency, $\eta=\pi/4(V_m/V_{cc})$ 100

Theory:

A power amplifier is said to be Class B amplifier if the Q-point and the input signal are selected such that the output signal is obtained only for one half cycle for a full input cycle. The Q-point is selected on the X-axis. Hence, the transistor remains in the active region only for the positive half of the input signal.

There are two types of Class B power amplifiers: Push Pull amplifier and complementary symmetry amplifier. In the complementary symmetry amplifier, one n-p-n and another p-n-p transistor is used. The matched pair of transistor are used in the common collector configuration. In the positive half cycle of the input signal, the n-p-n transistor is driven into active region and starts conducting and in negative half cycle, the p-n-p transistor is driven into conduction. However there is a period between the crossing of the half cycles of the input signals, for which none of the transistor is active and output, is zero

Procedure:

1. Connections are given as per the circuit diagram without diodes.
2. Observe the waveforms and note the amplitude and period of the input signal and distorted waveforms.
3. Connections are made with diodes.
4. Observe the waveforms and note the amplitude and time period of the input signal and output signal.
5. Draw the waveforms for the readings.
6. Calculate the maximum output power and efficiency.

OBSERVATIONS:

OUTPUT SIGNAL =

AMPLITUDE =

TIME PERIOD =

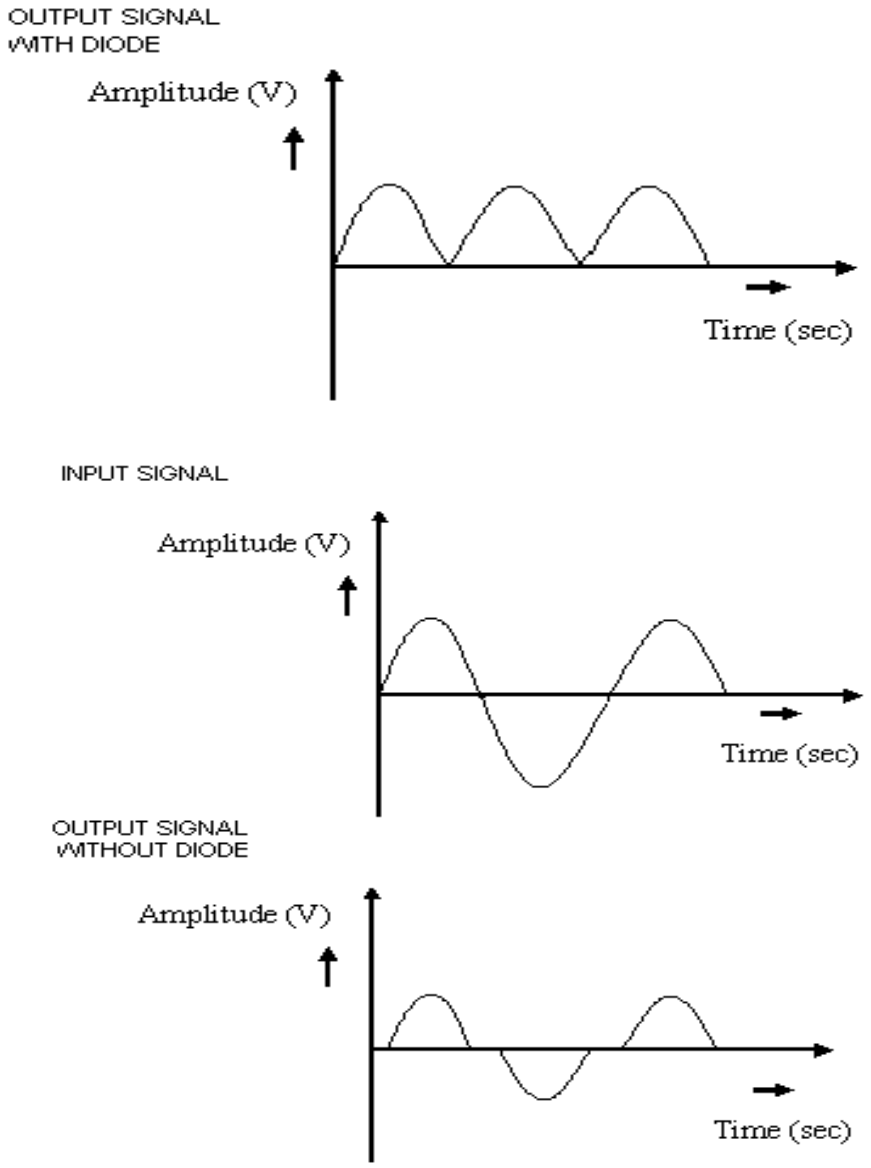
CALCULATION :

POWER, P_{IN} $= 2V_{CC}\, I_m/\pi$

OUTPUT POWER, P_o $= V_m I_m/2$

EFFICIENCY, η $= (\pi/4)(V_m/V_{CC}) \times 100$

MODEL GRAPH:



Hence the nature of the output signal gets distorted and no longer remains the same as the input. This distortion is called cross-over distortion. Due to this distortion, each transistor conducts for less than half cycle rather than the complete half cycle. To overcome this distortion, we add 2 diodes to provide a fixed bias and eliminate cross-over distortion.

Result:

10. VOLTAGE SHUNT FEEDBACK AMPLIFIER

Aim:

To measure the voltage gain of voltage shunt feedback amplifier.

Apparatus:

S.No.	Components and Equipments	Quantity
1	Bread Board	1
2	Transistor BC107	1
3	Resistors (1.5KΩ,33KΩ, 3.3KΩ, 330Ω 10KΩ)	1(each one)
4	Capacitors (100μF, 10μF)	1(each one)
5	Regulated Power Supply(0-30V)	1
6	Cathode Ray Oscilloscope (0-20MHz)	1
7	Function Generator (0-2MHz)	1
8	Digital Multimeter	1

Circuit Diagram:

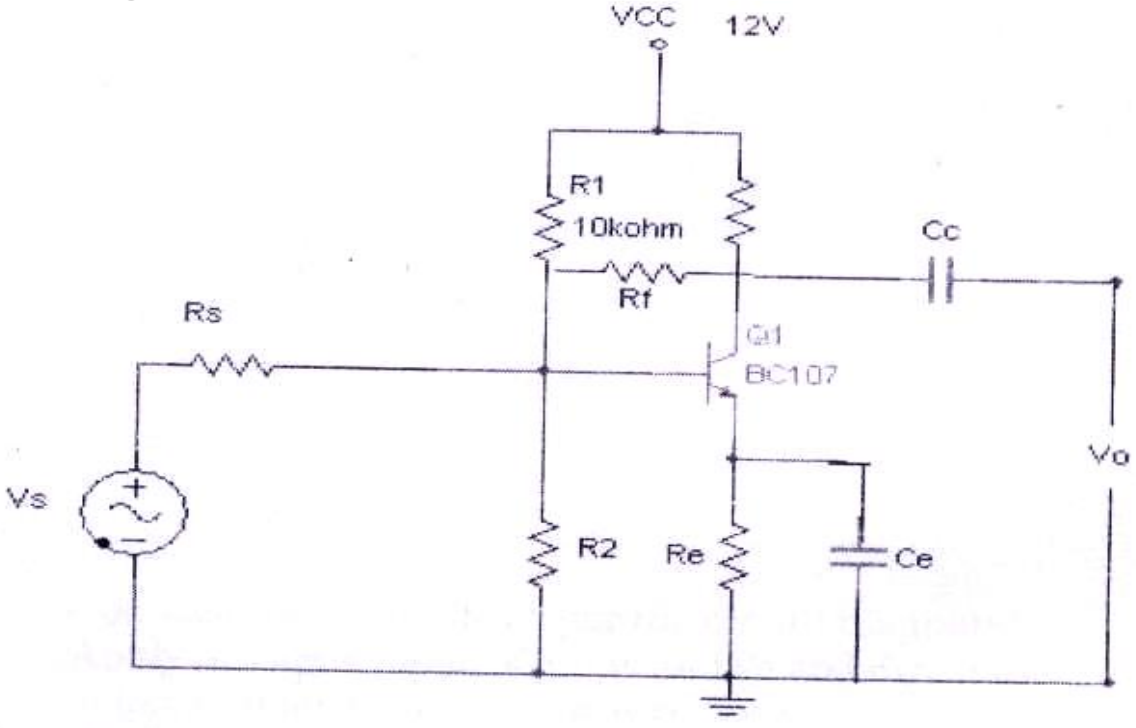


Fig 1: Voltage Shunt Feedback Amplifier

R_s = 100Ω,R_1 =33KΩ, R_2 = 1.5KΩ R_e = 300Ω R_c = 3.3KΩ R_f = 10KΩ

Theory:

When any increase in the output signal results into the input in such a way as to cause the decrease in the output signal, the amplifier is said to have negative feedback. The advantages of providing negative feedback are that the transfer gain of the amplifier with feedback can be stabilized against variations in the hybrid parameters of the transistor or the parameters of the other active devices used in the circuit. The most advantage of the negative feedback is that by proper use of this, there is significant improvement in the frequency response and in the linearity of the operation of the amplifier. This disadvantage of the negative feedback is that the voltage gain is decreased.

Model waveforms

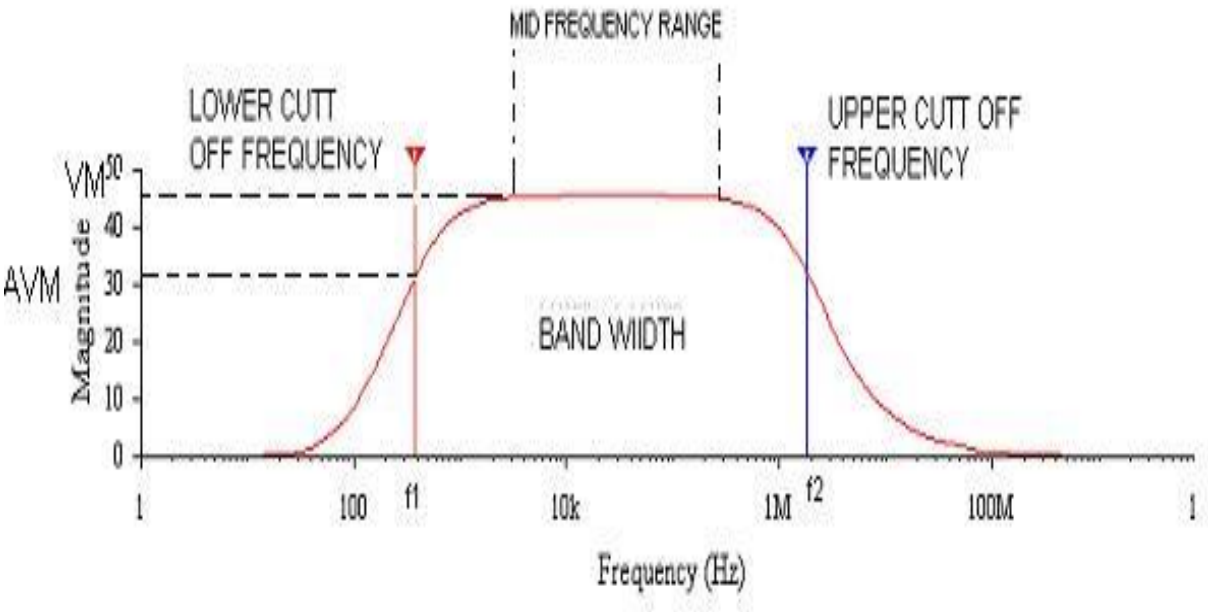


Fig 2: Frequency response of Voltage Shunt Feedback Amplifier

Procedure:

1. Connections are made as per circuit diagram.
2. Keep the input voltage constant at 20mV peak-peak and 1kHz frequency

For different values of load resistance, note down the output voltage and calculate the gain by using the expression

$$A_v = 20\log(V_0 / V_i)\ dB$$

3.Remove the emitter bypass capacitor and repeat STEP 2. and observe the effect of feedback on the gain of the amplifier.

4.For plotting the frequency the input voltage is kept constant at 20mV peak-peak and the frequency is varied from 100Hz to 1MHz.

5. Note down the value of output voltage for each frequency. All the readings are tabulated and the voltage gain in dB is calculated by using expression

$$A_v = 20\log (V_0 / V_i) \text{ dB}$$

6. A graph is drawn by taking frequency on X-axis and gain on Y-axis on semi log graph sheet
7. The Bandwidth of the amplifier is calculated from the graph using the expression Bandwidth B.W = $f_2 - f_1$.Where f_1 is lower cut off frequency of CE amplifier f_2 is upper cut off frequency of CE amplifier
8. The gain-bandwidth product of the amplifier is calculated by using the expression

Gain-Bandwidth Product = 3-dB mid band gain X Bandwidth.

Tabular Columns:

Voltage Gain: V_i = 20 mV

S.NO	Output Voltage (V_o) with feedback	Output Voltage (V_o) without feedback	Gain(dB) with feedback	Gain(dB) without feedback

Precautions:

1. While taking the observations for the frequency response , the input voltage must be maintained constant at 20mV.
2. The frequency should be slowly increased in steps.
3. The three terminals of the transistor should be carefully identified.
4. All the connections should be correct.

Result:

11. RC PHASE SHIFT OSCILLATOR.

Aim:

To design and set up an RC phase shift oscillator using BJT and to observe the sinusoidal output waveform.

Apparatus:

S.NO.	Components and Equipments	Quantity
1	Bread Board	1
2	Transistor BC107	1
3	Resistors(12KΩ,68KΩ, 3.9KΩ, 680Ω 1KΩ)	1(each one)
4	Resistors(10KΩ)	3
5	Capacitors(100μF, 0.1μF)	1&3respectively
6	Regulated Power Supply(0-30V)	1
7	Cathode Ray Oscilloscope(0-20MHz)	1
8	Digital Multimeter	1

Circuit Diagram:

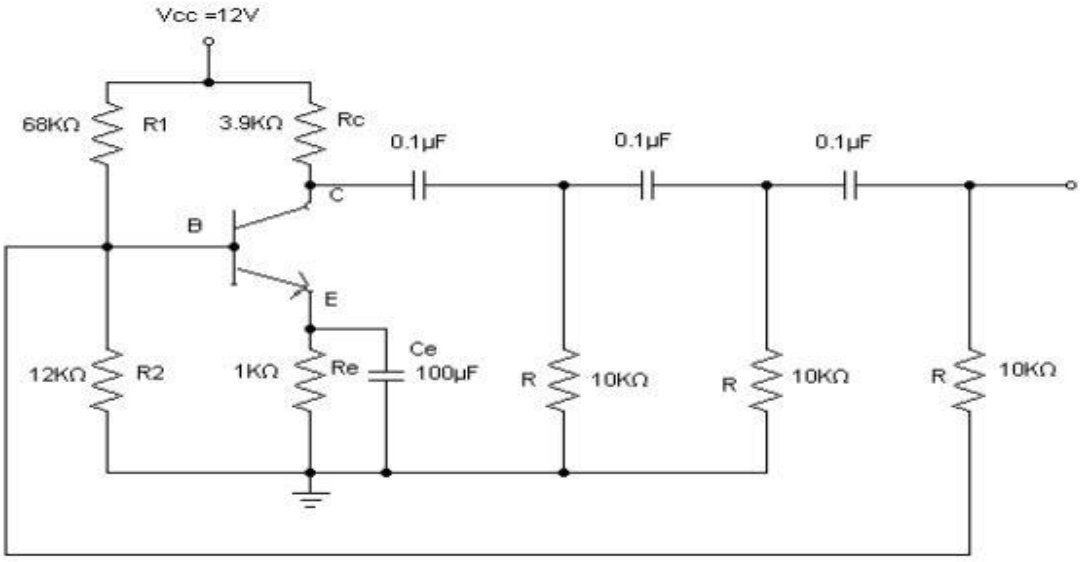


Fig 1: RC Phase shift Oscillator.

Theory:

An oscillator is an electronic circuit for generating an ac signal voltage with a dc supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements. An oscillator requires an amplifier, a frequency selective network, and a positive feedback from the output to the input. The Barkhausen criterion for sustained oscillation is Aβ = 1 where A is the gain of the

amplifier and β is the feedback factor. The unity gain means signal is in phase. (If the signal is 180° out of phase, gain will be 1.). If a common emitter amplifier is used, with a resistive collector load, there is a 180 phase shift between the voltages at the base and the collector.

In the figure shown, three sections of phase shift networks are used so that each section introduces approximately 60^0 phase shift at resonant frequency. By analysis, resonant frequency f can be expressed by the equation,

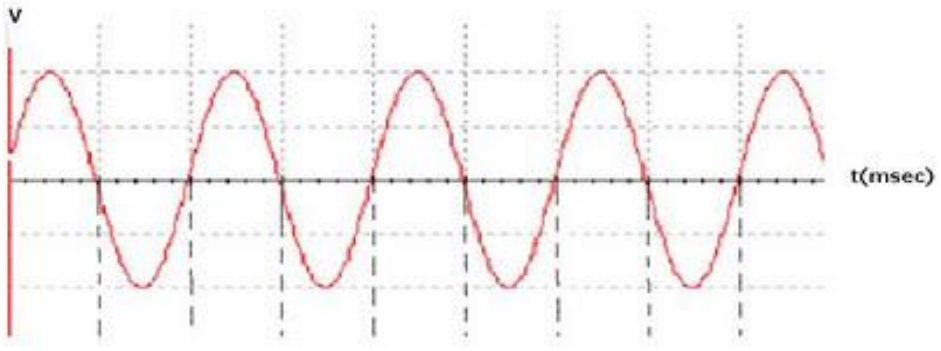
$$f = \frac{1}{2\pi RC\sqrt{6 + 4R_c/R}}$$

Procedure:

1. Connections are made as per circuit diagram.
2. Connect CRO output terminals and observe the waveform.
3. Calculate practically the frequency of oscillations by using the expression

   f = 1 / T (T= Time period of the waveform)
4. Repeat the above steps 2,3 for different values of L, and note down the practically values of oscillations of the RC-phase shift oscillator.
5. Compare the values of oscillations both theoretically and practically.

Model waveform:



Result:

12. COLPITT'S OSCILLATOR

Aim: To design and verify frequency of oscillations of Colpitt's oscillator.

Apparatus:

S.No.	Components and Equipments	Quantity
1	Bread Board	1
2	Transistor BC107	1
3	Resistors(1KΩ, 6.8KΩ 100KΩ)	1(each one)
4	Capacitors(10μF, 0.1μF,47μF)	2,2,1respectively
5	Decade Inductance box	1
6	Decade Resistance box	1
7	Regulated Power Supply(0-30V)	1
8	Cathode Ray Oscilloscope(0-20MHz)	1
9	Digital Multimeter	1

Circuit Diagram:

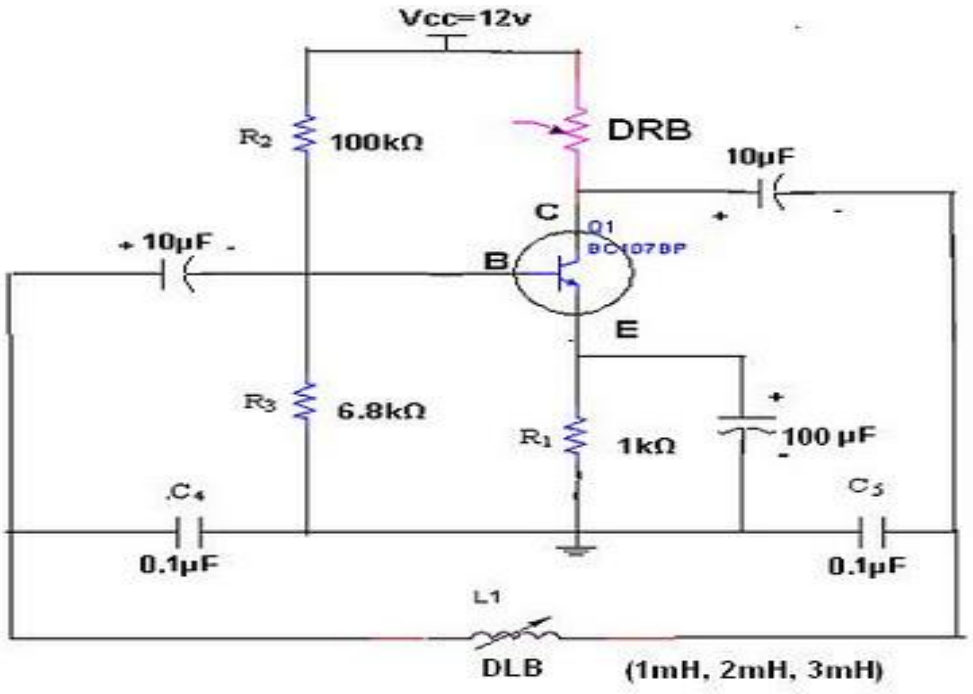


Fig 1: Colpitt's oscillator.

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Theory:

The tank circuit is made up of L_1,C_4 and C_5 .The resistance R_2 and R_3 provides the necessary biasing. The capacitance C_2 blocks the D.C component. The frequency of oscillations is determined by the values of L_1,C_4 and C_5, and is given by

$$f = \frac{1}{2\pi\sqrt{C_T L_1}} \text{ Where } C_T = \frac{C_1 C_2}{C_1 + C_2}$$

The energy supplied to the tank circuit is of correct phase. The tank circuit provides 180^0 out of phase. Also the transistor provides another 180^0 . In this way, energy feedback to the tank circuit is in phase with the generated oscillations.

Procedure:

a. Connections are made as per circuit diagram.
b. Connect CRO output terminals and observe the waveform.
c. Calculate practically the frequency of oscillations by using the expression

f = 1 / T T= Time period of the waveform)

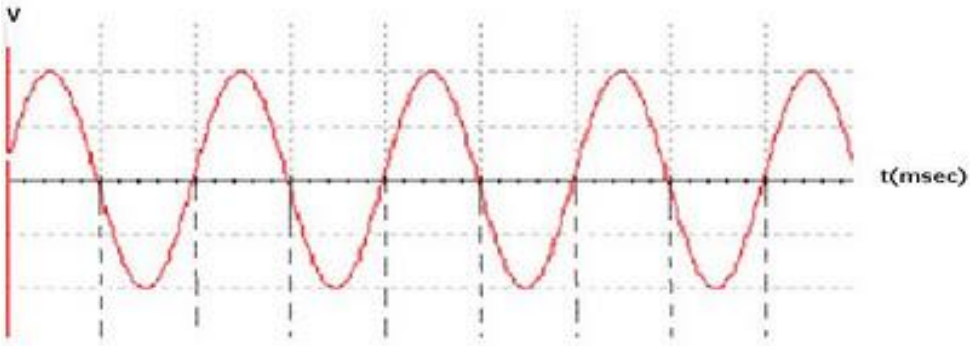
Repeat the above steps 2,3 for different values of L, an note down the practically values of oscillations of the collpitt's oscillator.

d. Compare the values of oscillations both theoretically and practically.

Observations:

Inductance (mH)	Theoretical Frequency (Hz)	Practical Frequency (Hz)

Model waveform:



Precautions:

1. All the connections should be correct.
2. Transistor terminals must be identified properly.
3. Reading should be taken without any parallax error.

Result:

13. HARTLEY/CRYSTAL OSCILLATOR

Aim:

1. To design and verify frequency of oscillations of Hartley oscillator

2. To compare the frequency of oscillations, theoretically and practically.

Apparatus:

S.No.	Components and Equipments	Quantity
1	Bread Board	1
2	Transistor BJT BC107	2
3	Resistors(1KΩ, 6.8KΩ 100KΩ)	1(each one)
4	Capacitors(10μF, 0.1μF)	1(each one)
5	Decade Inductance box	1
6	Decade Resistance box	1
7	Decade Capacitance box	1
8	Regulated Power Supply(0-30V)	1
9	Cathode Ray Oscilloscope(0-20MHz)	1
10	Digital Multimeter	1
11	Connecting Wires	

CIRCUIT DIAGRAM:

Hartley Oscillator

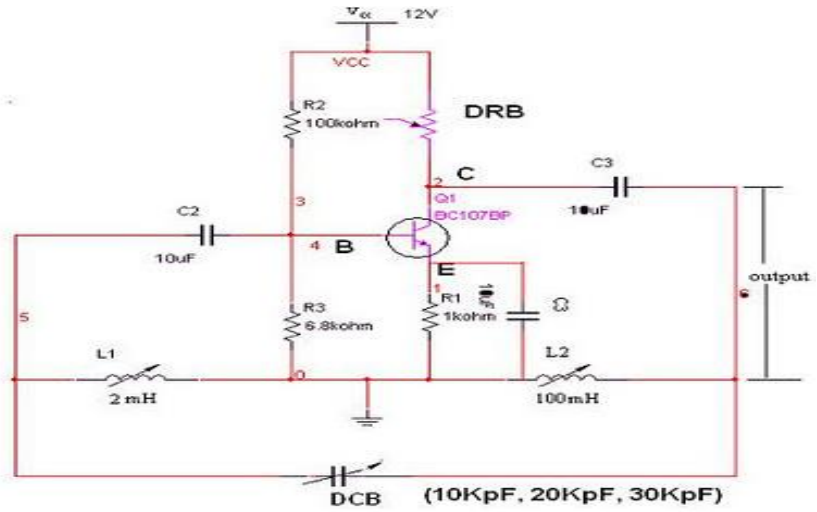


Fig 1: Hartley Oscillator

THEORY:

Hartley oscillator is very popular and is commonly used as a local oscillator in radio receivers. It has two main advantages are adaptability to wide range of frequencies and easy to tune. The tank circuit is made up of L_1, L_2, and C_1. The coil L_1 is inductively coupled to coil L_2, the combination functions as auto transformer. The resistances R_2 and R_3 provide the necessary biasing. The

capacitance C_2 blocks the d.c component. The frequency of oscillations is determined by the values of L_1, L_2 and C_1 and is given by,

$$f = \frac{1}{2\pi\sqrt{C_1(L_1+L_2)}}$$

The energy supplied to the tank circuit is of correct phase. The auto transformer provides 180˚ out of phase. Also another 180˚ is produced by the transistor. In this way, energy feedback to the tank circuit is in phase with the generated oscillations.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Connect CRO at output terminals and observe wave form.
3. Calculate practically the frequency of oscillations by using the expression.

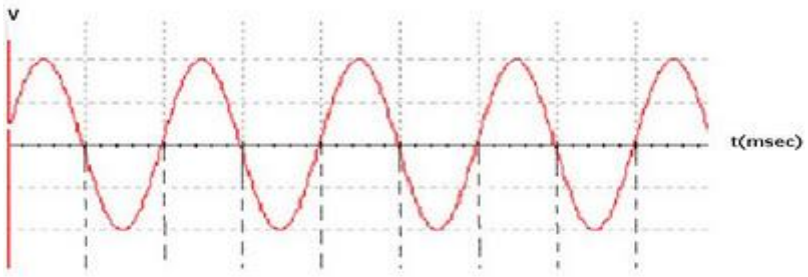
F=1/T, Where T= Time period of the waveform

4. Repeat the above steps 2, 3 for different values of L_1 and note down practical values of oscillations of hartley oscillator.
5. Compare the values of frequency of oscillations both theoretically and practically.

OBSERVATIONS:

CAPACITANCE(μF)	Theoritical frequency (KHZ)	Practical frequency (KHZ)

MODELWAVEFORM:



RESULT:

14. BJT DARLINGTON EMITTER FOLLOWER

AIM: To construct a BJT Darlington Emitter follower without bootstrapping and determination of the gain, input and output impedances

APPARATUS:

S.No.	Components and Equipments	Quantity
1	Bread Board	1
2	Transistor BC107	2
3	Resistors(1KΩ, 6.8KΩ 100KΩ)	1(each one)
4	Capacitors(10μF, 0.1μF,47μF)	2,2,1respectively
5	Decade Inductance box	1
6	Decade Resistance box	1
7	Regulated Power Supply(0-30V)	1
8	Cathode Ray Oscilloscope(0-20MHz)	1
9	Digital Multimeter	1

Theory:

The emitter follower has reasonably high input impedance and may be used wherever input impedance up to about 500 K Ohms is needed. For higher input impedance, we may use 2 transistors to form what is called a Darlington pair. When the output is taken from the Emitter terminal of the transistor, the network is referred to as an Emitter follower. The output voltage is always less than the input voltage due to the drop between the base and emitter. However, the voltage gain is usually approximately 1. in addition, the output is having the same polarity as the input voltage. Hence it is said to follow the input voltage with an in-phase relationship. This accounts for the terminology 'Emitter – follower'. For ac analysis, the collector is grounded; therefore, the circuit is a common-collector configuration. This circuit presents high impedance at the input and low impedance at the output. It is therefore frequently used for impedance matching purposes, where a load is matched to the source impedance for maximum signal transfer through the system

The Darlington connection shown is a connection of 2 transistors whose result is a current gain that is the product of the current gains of the individual transistors. Hence the Darlington pair operates as one 'Super beta' transistor offering a very high current gain. Thus, the Darlington Emitter follower is a CC

configuration that has the following characteristics:

- Voltage gain almost unity
- Current gain very high, a few thousands
- Input impedance high, hundreds of Kilo ohms
- Output impedance low, tens of ohms

Circuit Diagram without Bootstrap:

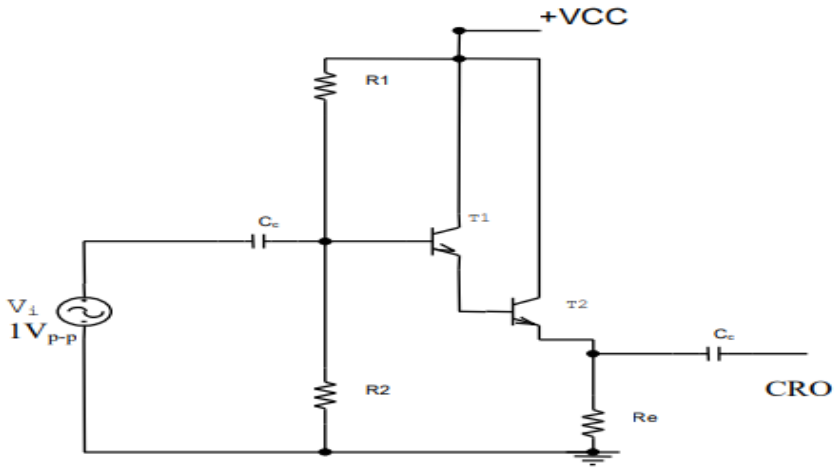


Fig 1: BJT Darlington Emitter Follower

DESIGN:

Let V_{CE} = 6V, I_{EQ}=10mA.
Then V_{CC} = 2V_{CE}=2 x 6 =12 V ,
$I_E = I_C$ = 10 mA $V_{R3} = V_{CC} - V_{CE}$= 12 – 6 = 6V
R_E= V_{R3} / I_E = 6V / (10 mA) = 0.6K =560Ω (Choose)
$V_{R2} – V_{BE1} – V_{BE2} – V_{RE}$ = 0 and
$V_{R2} = V_{BE1} + V_{BE2} + V_{RE}$ = 0.6 + 0.6 + (I_E x R_E) = 1.2 + (10x0.6) V_{R2} = 7.2 V,
$V_{CC} = V_{R1} + V_{R2}$, $V_{R1}= V_{CC} – V_{R2}$ = 12 – 7.2 = 4.8 V,
$I_{E1}= I_{B2} = I_C$ / hfe = 10 mA / 100 = 0.1mA
$I_{B1}=I_{E1}$ / hfe = 0.1mA / 100 = 1 mA,
$R_1 =V_{R1}$/ (10 (I_{B1})) = 4.8 / (10 x 1 µA) = 480 KΩ,
R_2= V_{R2} / (9 I_B) = 7.2 / (9 x 1 µA) = 800KΩ ,
Capacitor is selected(C_c) = 0.47 F and R_3=10KΩ

Procedure:

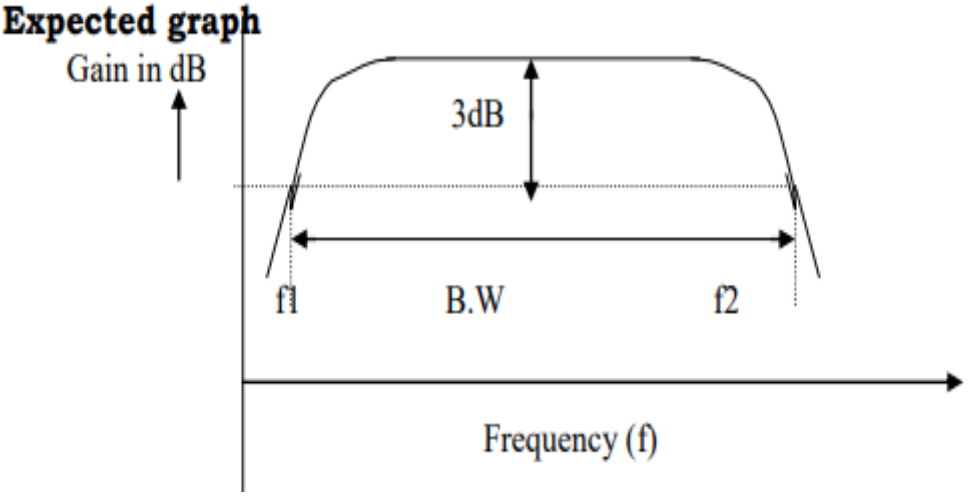
1. Connect the circuit and set VCC=12V. Measure the DC voltage (using CRO) at the (VB2), Collector (VC2), emitter (VE2) with respect to ground.
2. Connect the circuit and apply a sine wave of peak-to-peak amplitude 1V from the signal generator.

3. Vary the input sine wave frequency from 100 Hz to 1MHz in suitable Steps. Measure the output V_0 of the amplifier at each step using CRO. (The input Vi must remain constant throughout the frequency range)
4. Plot the graph of frequency v/s gain in dB.

Tabular Column $V_i = 1V_{(P-P)}$

Frequency In Hz	$V_{O\,(P-P)}$ In Volt	A_V=Vo / Vi	Gain in dB =20 $\log_{10} A_V$
10 Hz			
1MHz			

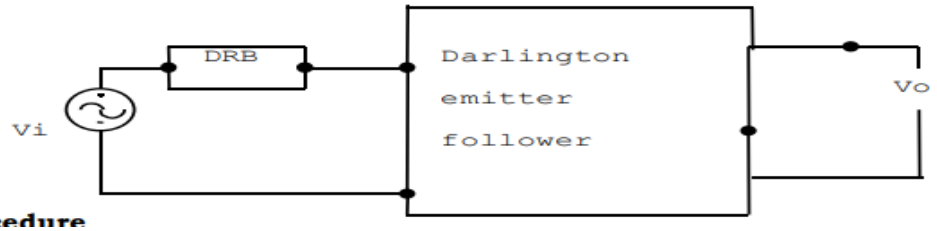
Expected graph



To measure Z_i and Z_0:

1. To measure ZI (Input Impedance) Procedure 1. Connect the circuit as shown in figure. 2. Set the DRB to minimum resistance (0Ω), I/P sine wave amplitude to 1V Peak to Peak, I/P sine wave frequency to 10 KHz. 3. Measure Vo (p-p). Let Vo=Va 4. Increase DRB till Vo=Va/2.the corresponding DRB value gives Zi.

1. To measure Z_I (Input Impedance)

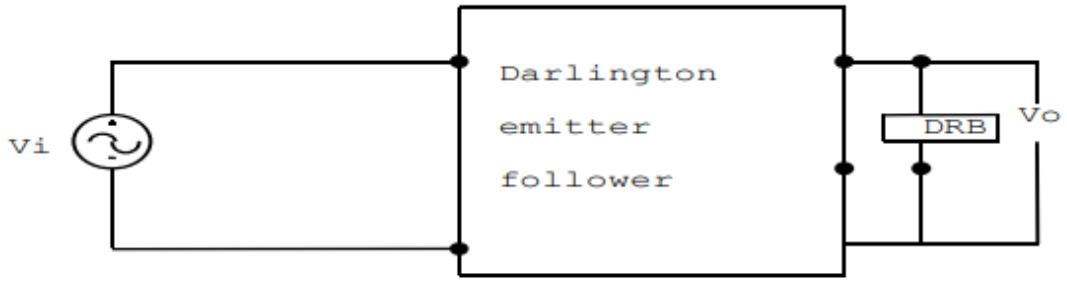


Procedure

2. To measure ZO (Output Impedance)

3. Connect the circuit as shown in figure. Set the DRB to its maximum resistance value, I/P sine wave Frequency to 10 KHz.

2. To measure Z_O (Output Impedance)



Procedure

1. Connect the circuit as shown in figure. Set the DRB to its maximum resistance value, I/P sine wave Frequency to 10 KHz.
2. Measure Vo p-p, let $V_O = V_B$
3. Decrease DRB till $V_O=V_B/2$. The corresponding DRB value gives ZO.

To find the current gain $A_I=I_O/I_i = (V_O / Z_O) / (V_i / Z_I) = (V_o/V_i) * (Z_I / Z_O)$ Current gain $A_i \approx Z_i / Z_O$, since $(V_O/V_i) = 1$

Result:

15. BJT VOLTAGE SERIES REGULATOR/ VOLTAGE SHUNT REGULATOR

AIM: To design and study the performances of BJT Voltage Series Regulator/ Voltage Shunt Regulator

APPARATUS REQUIRED:

S.NO.	NAME	RATING	NO.OF DEVICES
1	Regulated power supply	20V	1
2	Transistor	BC107	1
3	Zenor Diode	02DZ4.7	1
4	Resistors	100Ω 1KΩ	1 1
5	Digital Multimeter		1
6	Bread Board		1

CIRCUIT DIAGRAM:

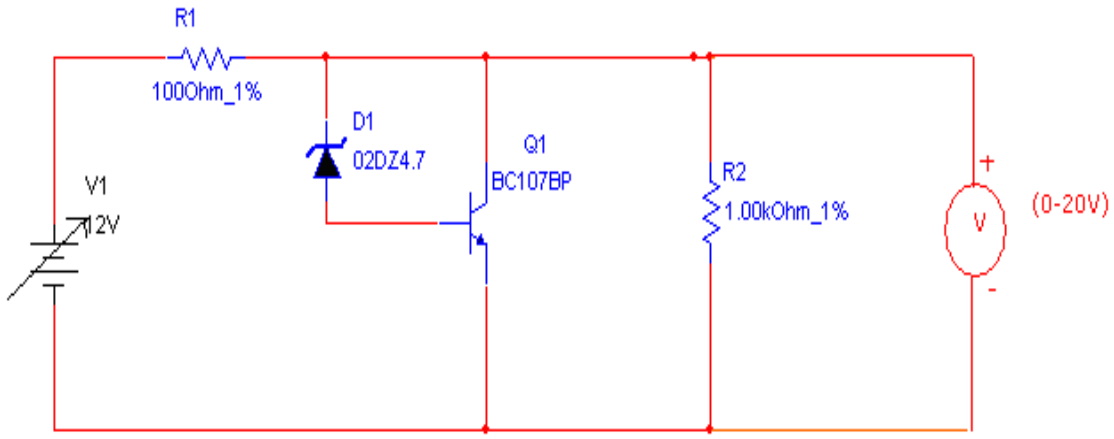


Fig: 1 BJT Voltage Series Regulator

PROCEDURE:

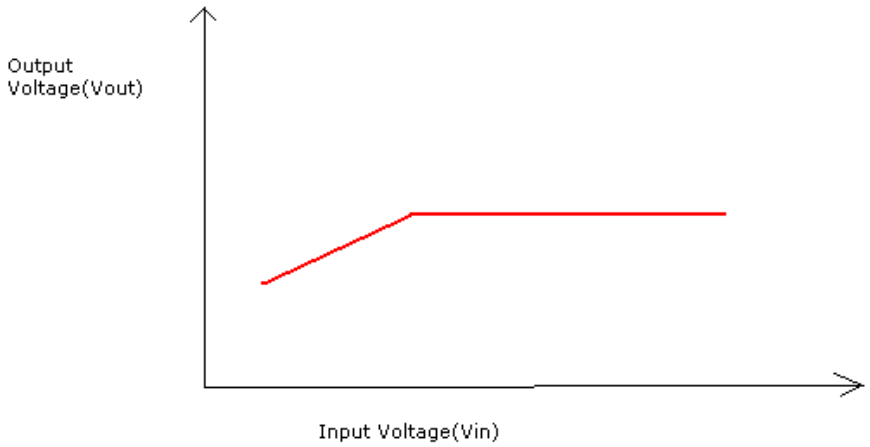
1. The circuit was connected as shown in figure.
2. The supply voltage is increased and note down the corresponding output voltage using multimeter.
3. The readings were tabulated in the tabular column.

4. The response characteristics are plotted on a graph sheet.

TABULAR COLUMN:

S.No.	Vin(V)	Vout(V)

Model Graph :



BJT Voltage Shunt Regulator

APPARATUS REQUIRED:

S.NO.	NAME	RATING	NO.OF DEVICES
1	Regulated power supply	30V	1
2	Transistor	BC107	2
3	Zenor Diode	02DZ4.7	1
4	Resistors	1KΩ 4.33KΩ 4.37KΩ 560Ω	2 1 1 1
5	Digital Multimeter		1
6	Bread Board		1

CIRCUIT DIAGRAM:

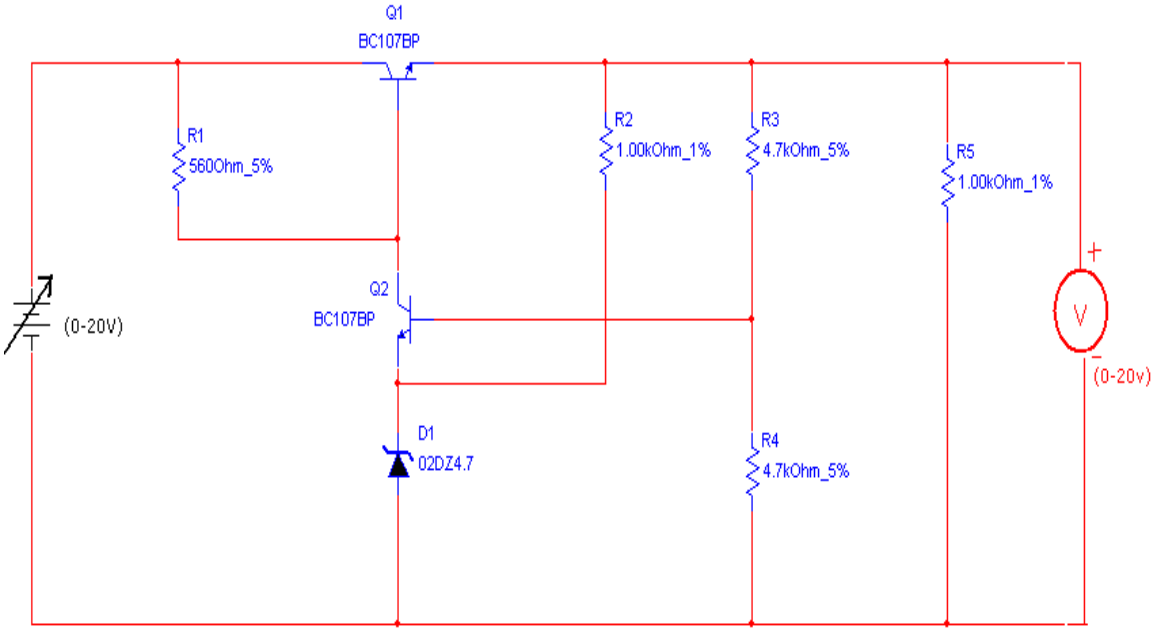


Fig: 2 BJT Voltage Shunt Regulator

THEORY:

A voltage regulator is a device or a combination of devices, designed to maintain the output voltage of a power supply as nearly constant as possible even if there are changes in the load or in input voltage. In shunt voltage regulator, transistor Q1 acts as control element, which is in shunt with load voltage. The output voltage is given as Vo = Vz + VR1 = Vz The regulation action of the circuit is explained below. Since Vz is constant, any changes in output voltage reflects a

propositional change in R1. If the output voltage decreases, voltage across R1 decreases which in turn decreases the base voltage of . As a result the base current of Q1 decreases which allows the load voltage to rise and makes it constant the same regulation action follows even if the output voltage increases.

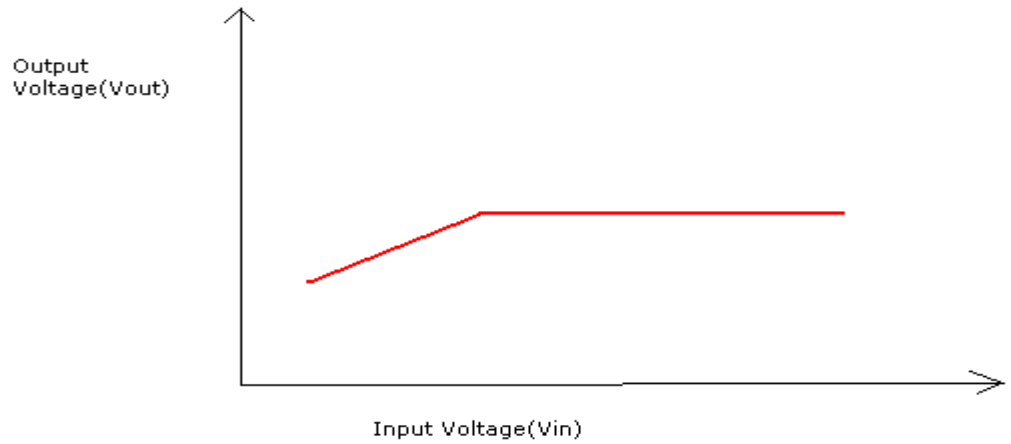
PROCEDURE:

1. The circuit is connected as shown in figure.
2. The supply voltage is to be increased in steps and note down the corresponding output voltage using multimeter.
3. The readings are tabulated in the tabular column.
4. The output response was plotted on a graph sheet.
5.

TABULAR COLUMN:

S.No.	Vin(V)	Vout(V)

Model Graph:



RESULT:

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