EC412

Hall Ticket Number:

IV/IV B.Tech (Regular) DEGREE EXAMINATION

OCTOBER, 2016 — **Electronics and Communication Engineering**

Seventh Semester — **VLSI Design**

Time: Three Hours **Maximum :** 60 Marks

Answer Question No.1 compulsorily. (1X12 = 12 Marks)

Answer ONE question from each unit. (4X12=48 Marks)

1. Answer all questions (1X12=12 Marks)

a Write any two advantages of E beam masks.
b What are the disadvantages of NMOS depletion mode pull up inverter.
c Why n-well CMOS circuits superior to p-well CMOS circuits?
d Define sheet resistance (R_s).
e Mention the purpose of design rules.
f What is the purpose of scaling?
g Design Dynamic CMOS 2 input nor gate.
h Give the stick diagram color encoding scheme for any two layers.
i Design 2 input Exor gate using transmission gates.
j What is the basic difference between PLA and PAL?
k What is the difference between the following two lines of Verilog code
#5 a = b;
a = #5 b;
l What does `timescale 1ns/ 1ps signifies in a Verilog code?

UNIT – I

2.a What are different approaches to CMOS fabrication? Describe n-well CMOS fabrication process with neat sketches 8M

2.b Compare CMOS technologies with bipolar technologies. 4M

(OR)

3.a With neat circuit diagram and waveforms discuss voltage transfer characteristics of CMOS inverter. 6M

3.b In the inverter circuit, what is meant by $Z_{p.u}$ and $Z_{p.d}$? Derive the required ratio between $Z_{p.u}$ and $Z_{p.d}$ if an nMOS inverter is to be driven through one or more pass transistors. 6M

UNIT – II

4.a Draw the stick diagram and a mask layout for an 8:1 nMOS inverter circuit. Both the input and output points should be on the poly-silicon layer. 8M

4.b An off chip capacitance load of *5* pF is to be driven from CMOS inverter. Set out suitable arrangements giving appropriate channel *L: W* ratios and dimensions. Calculate the number of inverter stages required, and the delay exhibited by the overall arrangement driving the *5* pF load. 4M

(OR)

5.a Derive expressions for rise-time and fall-time of CMOS inverter 6M

5.b How the following parameters effected when constant electric field scaling model applied. 6M
a)Gate area(A_g) b) Gate capacitance (C_g) c) Channel resistance (R_{on}) d) Maximum operating frequency (f_0) e) Switching energy per gate (E_g) f) Power speed product (P_a)

UNIT – III

6.a Construct a color-coded stick diagram to represent the design of the NAND and NOR CMOS structures and indicate pull-up/pull-down ratios in each case 6M

6.b Design two-phase clock generator using D flip-flops. 6M

(OR)

7.a	Design CMOS multiplexer based 1-bit full adder logic with buffered SUM output	8M
7.b	Discuss architectural issues in design process	4M

UNIT – IV

8.a	Draw FPGA architecture and explain each block briefly.	6M
8.b	Explain different types of gate-array-based ASICs.	6M

(OR)

9.a	Discuss typical design flow for designing VLSI IC circuits.	6M
9.b	Design an 8-bit counter by using a forever loop, named block, and disabling of named block. The counter starts at count = 7 and finishes at count = 54. The count is incremented at positive edge of clock. The clock has a time period of 10. The counter counts through the loop only once and then is disabled.	6M