14EC305

Hall Ticket Number:

II/IV B.Tech (Regular) DEGREE EXAMINATION

OCTOBER, 2016 — **Electronics and Communication Engineering**

Third Semester — **DIGITAL ELECTRONICS**

Time: Three Hours — **Maximum :** 60 Marks

Answer Question No.1 compulsorily. (1X12 = 12 Marks)

Answer ONE question from each unit. (4X12=48 Marks)

1. Answer all questions (1X12=12 Marks)

a Convert $(1011010)_2$ into gray code.

b Represent $(-95)_{10}$ using Signed 2's Complement form.

c Prove $\overline{x+y} = \bar{x}\bar{y}$.

d Specify any two degenerate forms of two level implementations.

e Simplify $F(b,c,a,d) = \sum m(2,3,4,7,11,12,15)$.

f Implement a Half Adder using Basic Gates.

g Design a 8:1 MUX using 4:1 MUX.

h Write the excitation table for JK flip-flop.

i Differentiate Combinational and Sequential logic implementation of the circuits.

j In order to save the power consumption the logic family best suited for design is _____

k Draw a two bit up counter using JK flip-flops.

l Which PLD is used in electronic toys.

UNIT – I

2.a Find the subtraction of $(12345)_{10}$-$(479)_{10}$ using 10's and 9's complement methods. 6M

2.b What are the logic gates? Explain its functionality using Truth table, Boolean expression, its circuit symbol. 6M

(OR)

3.a What are binary codes? Mention the example for different binary codes. Generate the 4 bit reflected code. 6M

3.b Minimize the given expression and represent it in both Standard SOP and Standard POS forms using Boolean theorems. 6M

$$F(a,b,c) = \sum m(2,3,4,6,7)$$

UNIT – II

4.a Minimize the given Boolean Function using K- Maps.

$$F(a,b,c,d,e) = \sum m(0,1,5,6,9,13,14,17,21,22,25,29) + d(2,11,26,30)$$ 6M

4.b Simply the following Boolean function using Quine – McCluskey method.

$$Y(A,B,C,D) = \sum m(1,2,3,5,9,12,14,15) + d(4,8,11)$$ 6M

(OR)

5.a Design a Full Adder and also Implement it using Half Adders. 6M

5.b Implement $F = (A+B')(CD+E)$ using Multi level NAND gates. 6M

UNIT – III

6.a Design a 4 bit Magnitude comparator. 6M

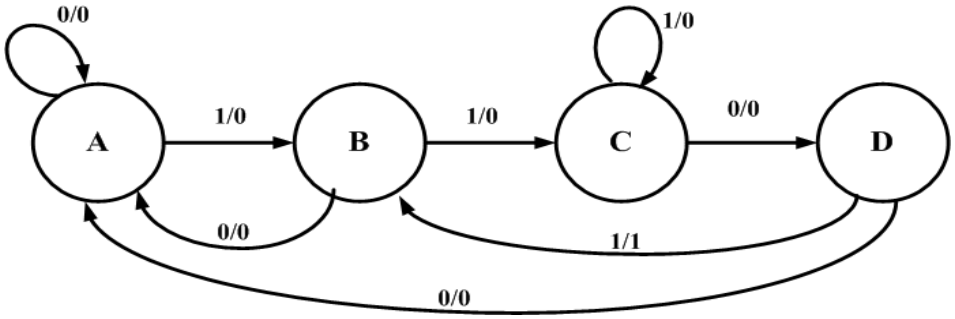
6.b Implement the following Boolean expression using 16:1 Multiplexer.

$$Y = \bar{A}B\bar{C} + A\bar{B}\bar{C}D + \bar{A}\bar{B} + \bar{A}CD$$ 6M

(OR)

7.a Convert the JK Flip – flop to SR, T & D Flip – flops. 6M

7.b Design a Sequential circuit using D flip – flops for the given state diagram 6M



UNIT – IV

8.a Design an asynchronous Decimal BCD counter using D flip – flops. 6M

8.b A 3 – input and 4 – output combinational circuit has the following output functions. Implement the circuit using a suitable PAL. 6M

$$A(x, y, z) = \sum m(1, 2, 4, 6)$$
$$B(x, y, z) = \sum m(0, 1, 3, 6, 7)$$
$$C(x, y, z) = \sum m(1, 2, 4, 6, 7)$$
$$D(x, y, z) = \sum m(1, 2, 3, 5, 7)$$

(OR)

9.a Design an Universal Shift register using D flip – flops. 6M

9.b Construct the NAND gate using Schottky TTL logic and explain its operation and working with neat sketch. 6M