PSPICE LAB MANUAL

LAB CODE:EC 262

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BAPATLA ENGINEERING COLLEGE
BAPATLA

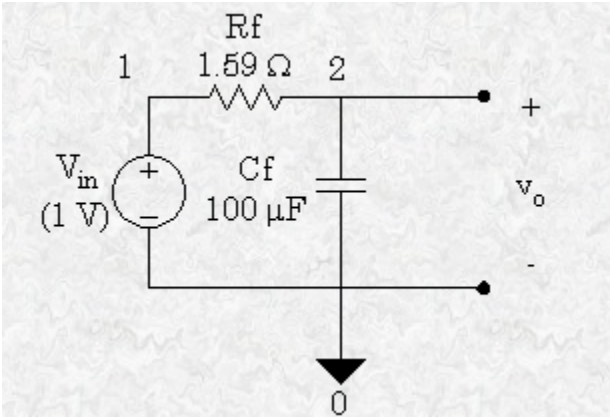
LIST OF EXPERIMENTS

1. Verification of Low pass and High pass Filter
2. Verification of Half–Wave and Full-Wave Rectifier
3. Frequency Response of CE Amplifier
4. Frequency Response of CS Amplifier
5. Frequency Response of CC Amplifier
6. Design of Wein-Bridge Oscillator
7. Design and Verification of Class-A Power Amplifier
8. Design and Verification of Pre-emphasis and De-emphasis circuits
9. Verification of Clippers
10. Verification of Clampers
11. Design and Verification of RC coupled amplifier
12. Design and Verification of Voltage Regulator
13. Design and Verification of Attenuators
14. Design and Verification of Differential amplifier
15. Design and Verification of Logic Gates

PROGRAM: 1

AIM: To verify the characteristics of Low pass and High pass filter

CIRCUIT



Here's a simple circuit for you to dive into running SPICE simulations and plotting results.

What is the purpose of this circuit? Basically it has two roles: to **pass** the desired low frequency signals and **stop** the unwanted high frequency signals.

CUTOFF FREQUENCY

As stated above, the circuit has two roles: to pass the desired low frequency signals and stop the unwanted high frequency signals. But at what frequency does the filter change its behavior from passing the low ones to stopping the high ones. This is called the cut-off frequency.

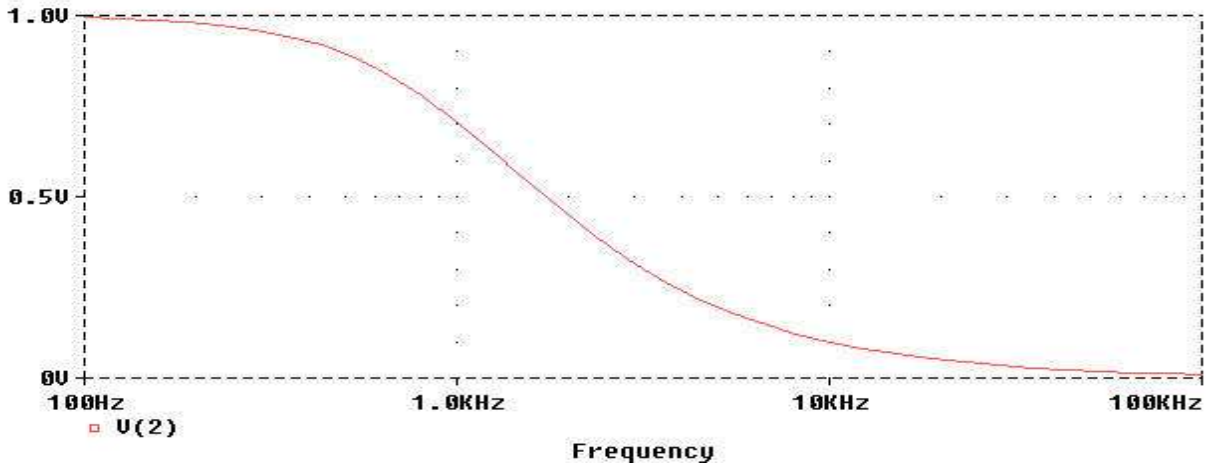
$$fc = \frac{1}{2\pi \times R1 \times C1}$$

For R1=1k and C1=0.032uF you get fc = 5kHz. Run a simulation. Plot the AC (frequency) sweep results for the output magnitude VM(2) and phase VP(2). What does the magnitude look like before and after 5kHz?

SPICE FILE

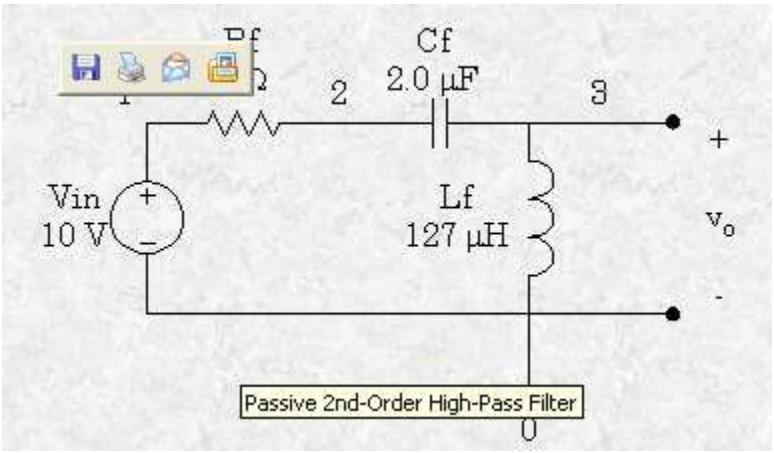
```
VIN 1 0 AC 1V

RF 1 2 1.59

CF 2 0 100UF

.AC DEC 20 100HZ 100KHZ

.PROBE

.END
```

After running this in PSpice, we start PROBE, choose "Add" from the "Trace" menu and plot the output voltage. PROBE provides the following graph.



HIGH PASS FILTER

CIRCUIT



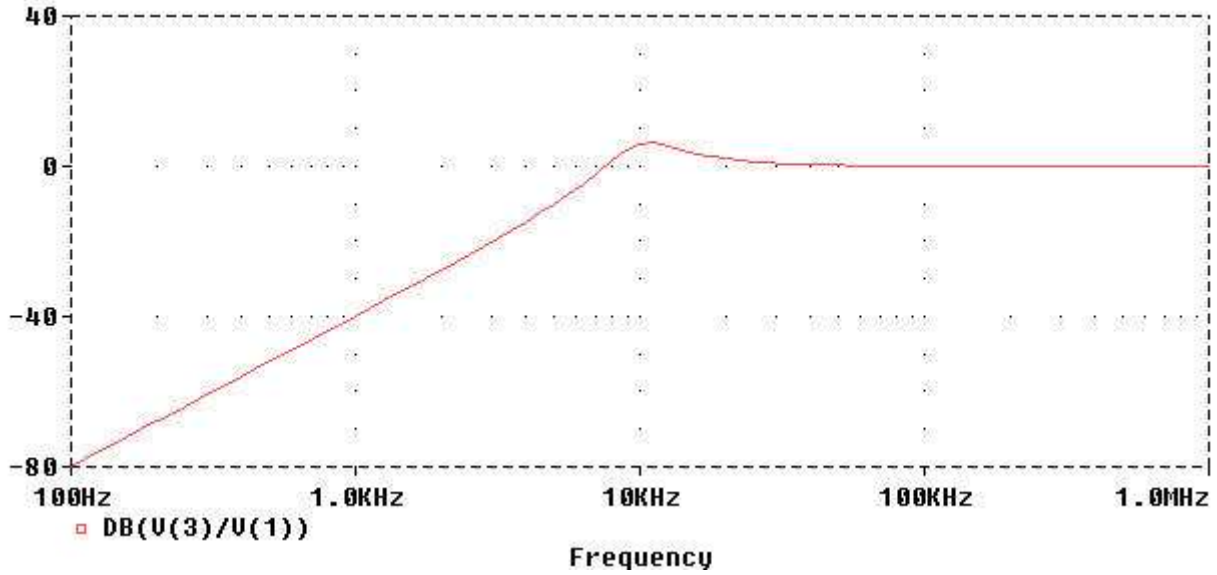
Here's a simple circuit for you to dive into running SPICE simulations and plotting results.

What is the purpose of this circuit? Basically it has two roles: to **pass** the desired high frequency signals and **stop** the unwanted low frequency signals.

SPICE FILE

```
Vin 1 0 AC 10V
Rf 1 2 4.0
CF 2 3 2.0uF
Lf 3 0 127uH
.AC DEC 20 100Hz 1MEG
.PROBE
.END
```

This time we did not use 1V for the input voltage. Therefore, we will need to have PROBE actually divide the input into the output to get the gain. We show this gain in decibels.



Notice that the gain below the resonant frequency of 10 kHz slopes upward at 40 dB/decade. When we plot the phase shift of this filter, we only need to specify the phase angle of the output voltage since the input voltage was specified at 0 degrees.

PROGRAM:2

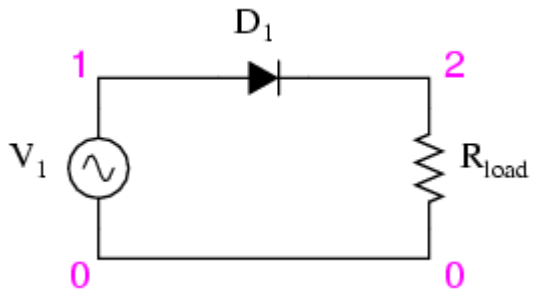
AIM: To verify the characteristics of Low pass and High pass filter

RECTIFIER

Before the development of silicon semiconductor rectifiers, vacuum tube diodes and copper(I) oxide or selenium rectifier stacks were used. High power rectifiers, such as are used in high-voltage direct current power transmission, now uniformly employ silicon semiconductor devices of various types. These are thyristors or other controlled switching solid-state switches which effectively function as diodes to pass current in only one direction.

HALF WAVE RECTIFIER

CIRCUIT



In half wave rectification, either the positive or negative half of the AC wave is passed, while the other half is blocked. Because only one half of the input waveform reaches the output, it is very inefficient if used for power transfer. Half-wave rectification can be achieved with a single diode in a one-phase supply, or with three diodes in a three-phase supply. Half wave rectifiers yield a unidirectional but pulsating direct current.

SPICE FILE

V1 1 0 SIN(0 10V 100HZ)

R 1 2 1K

DA 0 2 D1

.MODEL D1 D

.TRAN 0.01MS 20MS

.PROBE

.END

MODEL WAVE FORM

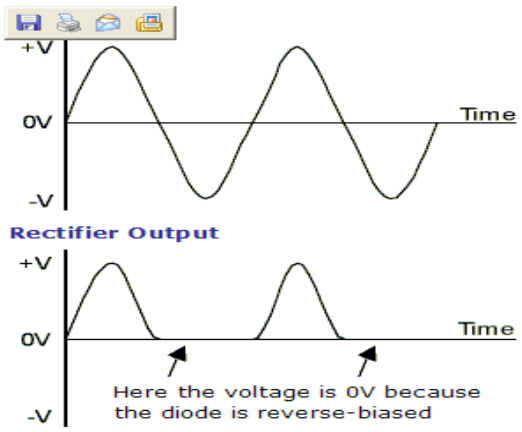
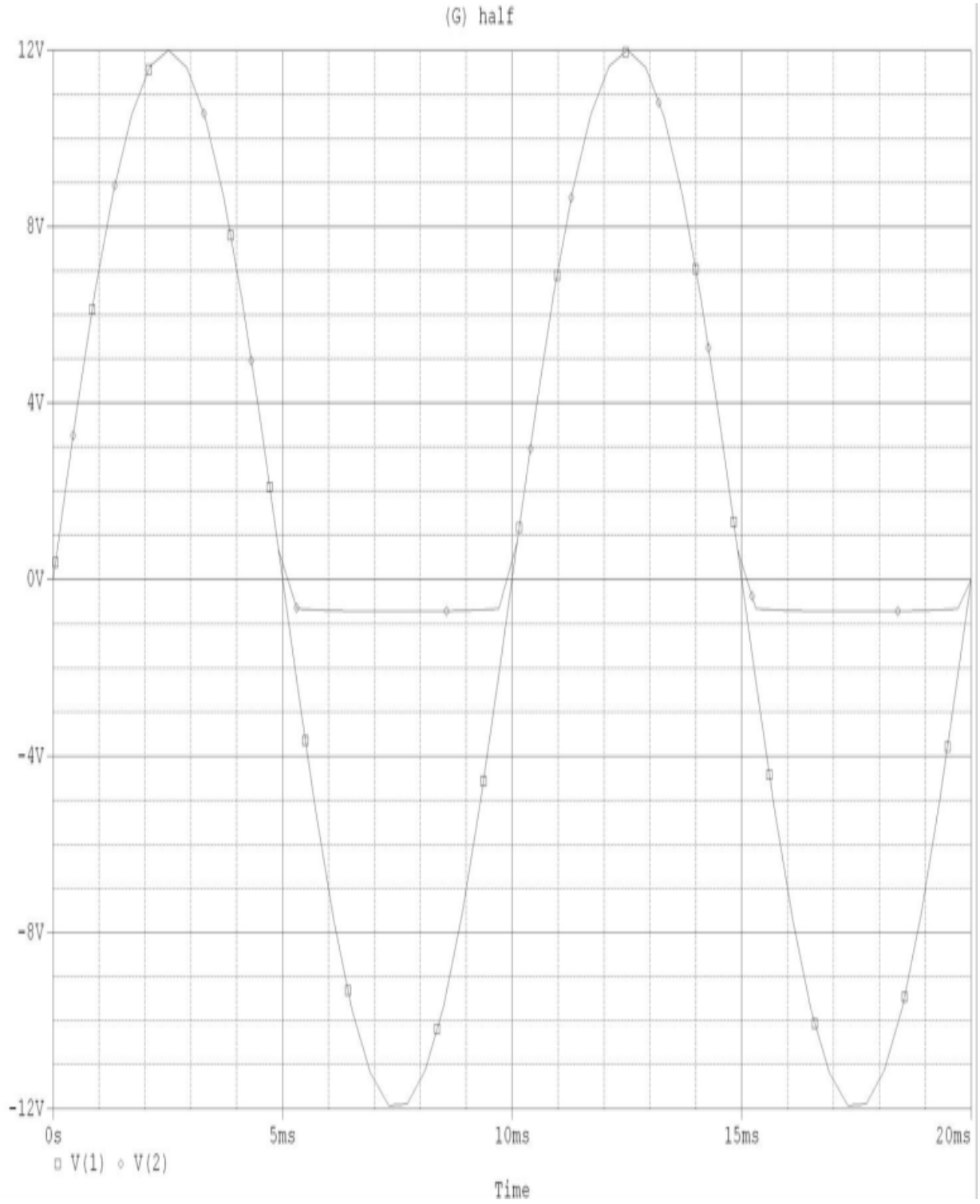


Figure : Half-wave rectification

RESULT:



FULL WAVE RECTIFIER

A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output. Full-wave rectification converts both polarities of the input waveform to DC (direct current), and is more efficient.

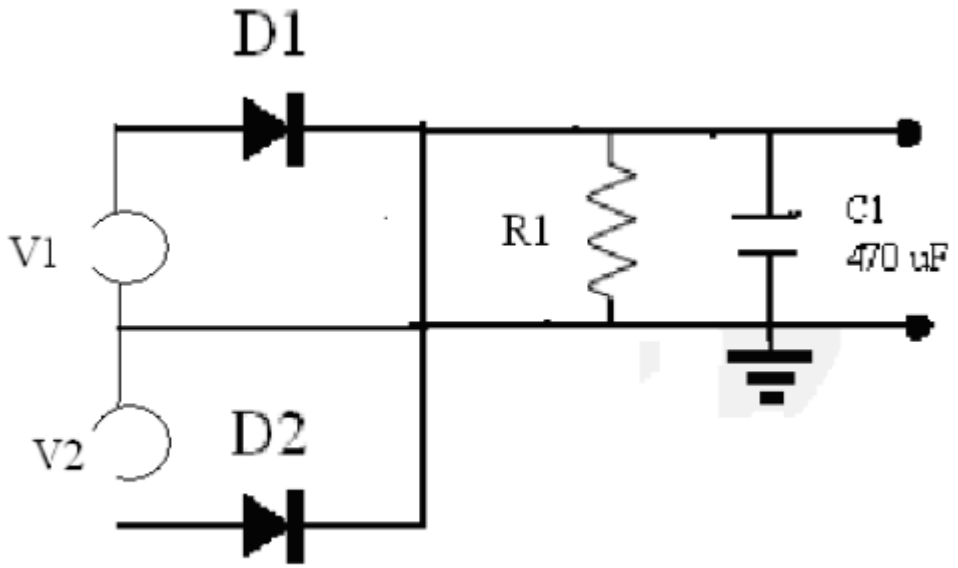


Figure : Full Wave Rectifier

SPICE FILE

V1 1 0 SIN(0 10V 100HZ)

R 2 3 1K

C 2 3 1N

D1 1 2 MOD1

D2 0 2 MOD1

.MODEL MOD1 D

.TRAN 0.01MS 20MS

.PROBE

.END

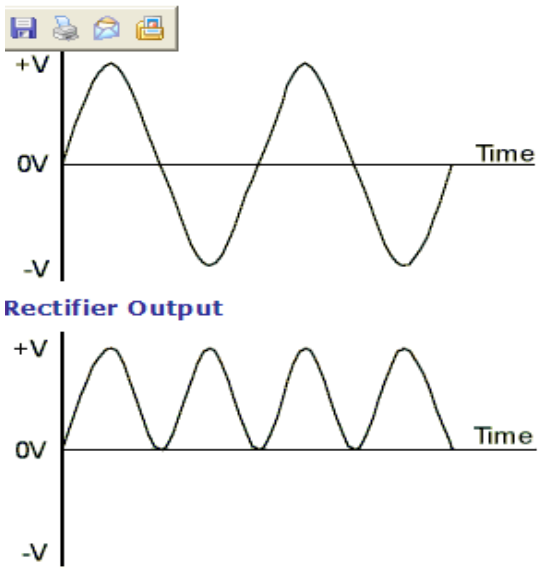
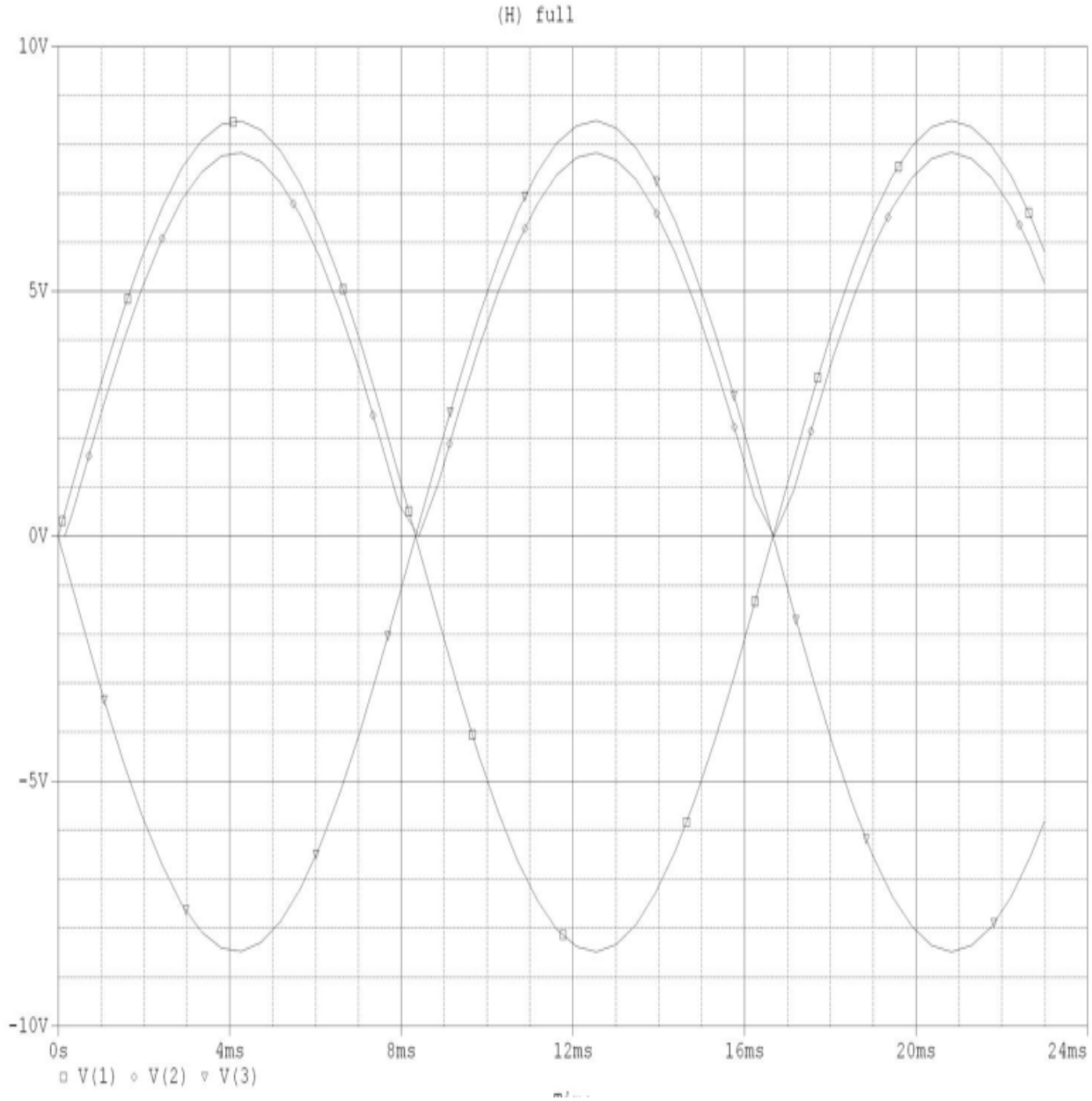


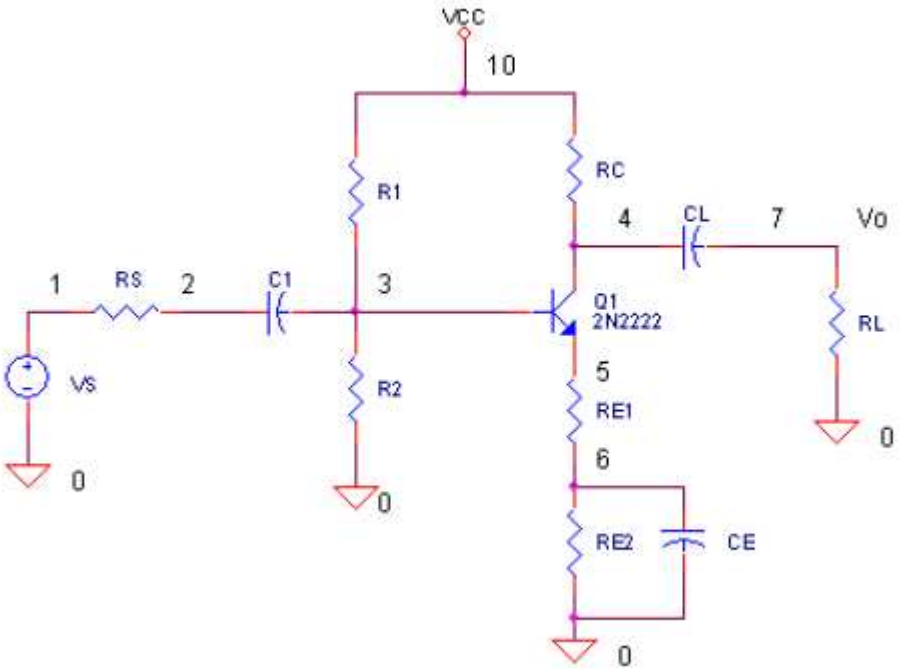
Figure : Full-wave rectification

RESULT:


(H) full
10V
5V
0V
-5V
-10V
0s
4ms
8ms
12ms
16ms
20ms
24ms
V(1) V(2) V(3)

PROGRAM:3

AIM: To verify the characteristics of CE Amplifier

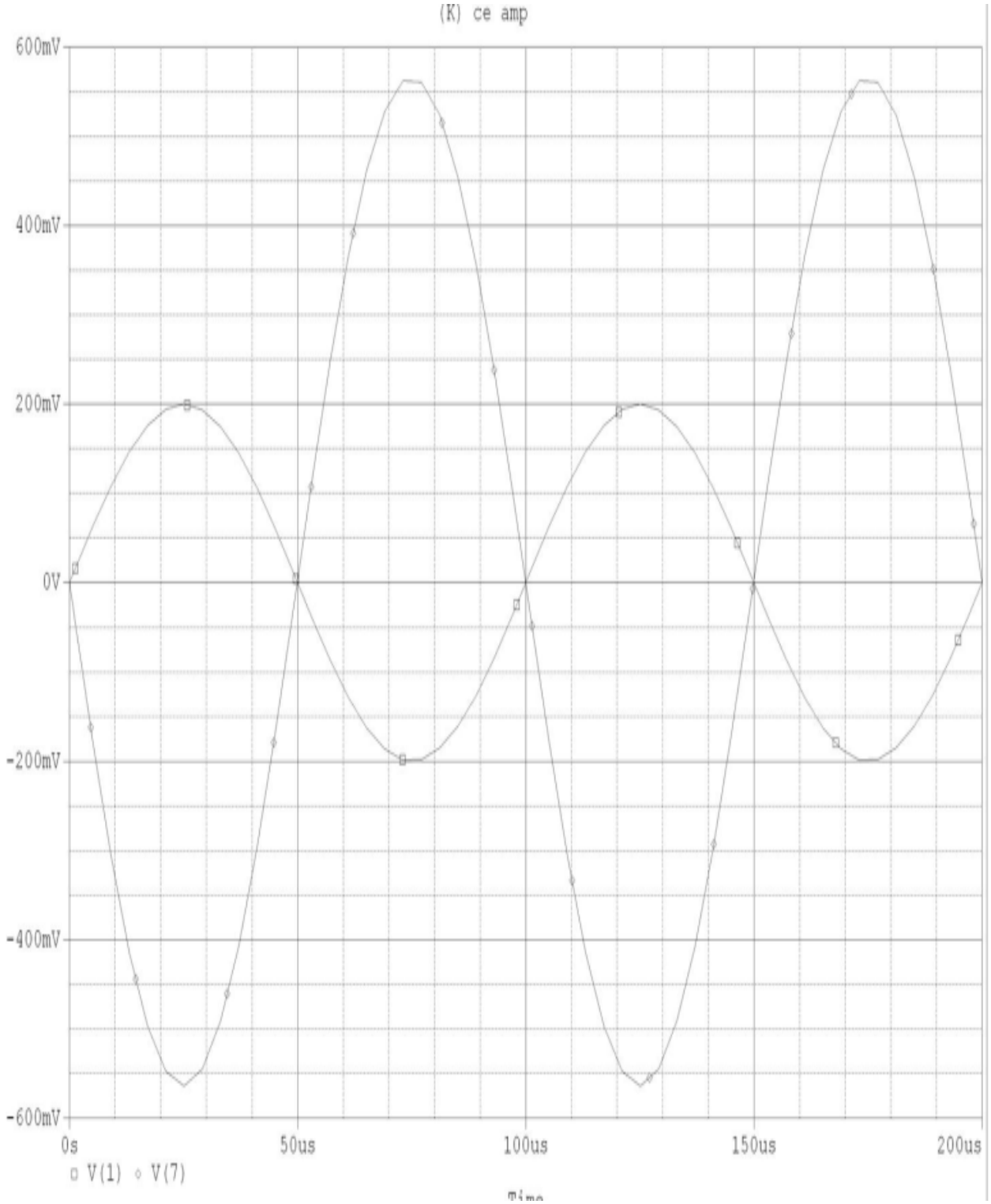


The COMMON-EMITTER CONFIGURATION (CE) is the most frequently used configuration in practical amplifier circuits, since it provides good voltage, current, and power gain. The input to the CE is applied to the base-emitter circuit and the output is taken from the collector-emitter circuit, making the emitter the element "common" to both input and output. The CE is set apart from the other configurations, because it is the only configuration that provides a phase reversal between input and output signals.

SPICE FILE

```
VIN 1 4 SIN(0 1.5V  2KHZ)

VB 4 0 2.3V

RL 3 0 15K

V1 2 0 15V

Q1 2 1 3 MOD1

.MODEL MOD1 NPN

.TRAN 0.02MS 0.78MS

.PROBE

.END
```

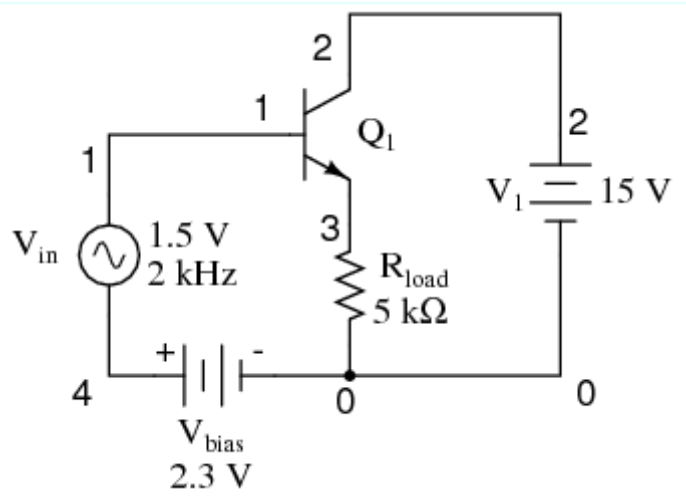
RESULT:


(K) ce amp
600mV
400mV
200mV
0V
-200mV
-400mV
-600mV
0s
50us
100us
150us
200us
V(1)
V(7)
Time

PROGRAM:4

PROGRAM:4

AIM: To verify the characteristics of **CC** Amplifier



Common collector amplifier has collector common to both input and output.

It is called the *common-collector* configuration because (ignoring the power supply battery) both the signal source and the load share the collector lead as a common connection point

Common collector: Input is applied to base and collector. Output is from emitter-collector circuit.It should be apparent that the load resistor in the common-collector amplifier circuit receives both the base and collector currents, being placed in series with the emitter. Since the emitter lead of a transistor is the one handling the most current (the sum of base and collector currents, since base and collector currents always mesh together to form the emitter current), it would be reasonable to presume that this amplifier will have a very large current gain. This presumption is indeed correct: the current gain for a common-collector amplifier is quite large, larger than any other transistor amplifier configuration. However, this is not necessarily what sets it apart from other amplifier designs.

SPICE FILE

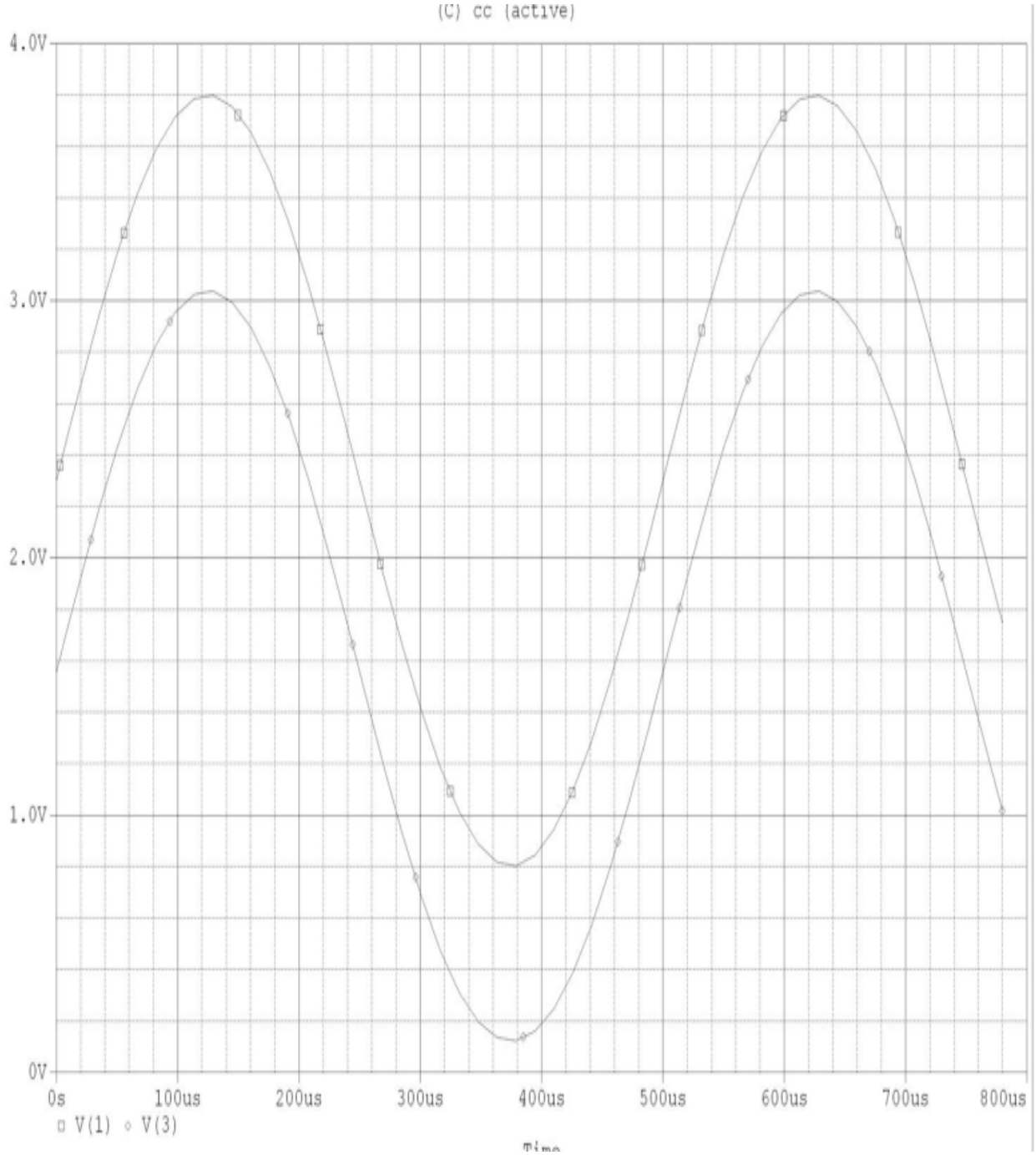
VIN 1 4 SIN(0 1.5 2000 0 0)

VBIAS 4 0 DC 2.3

Q1 2 1 3 MOD1

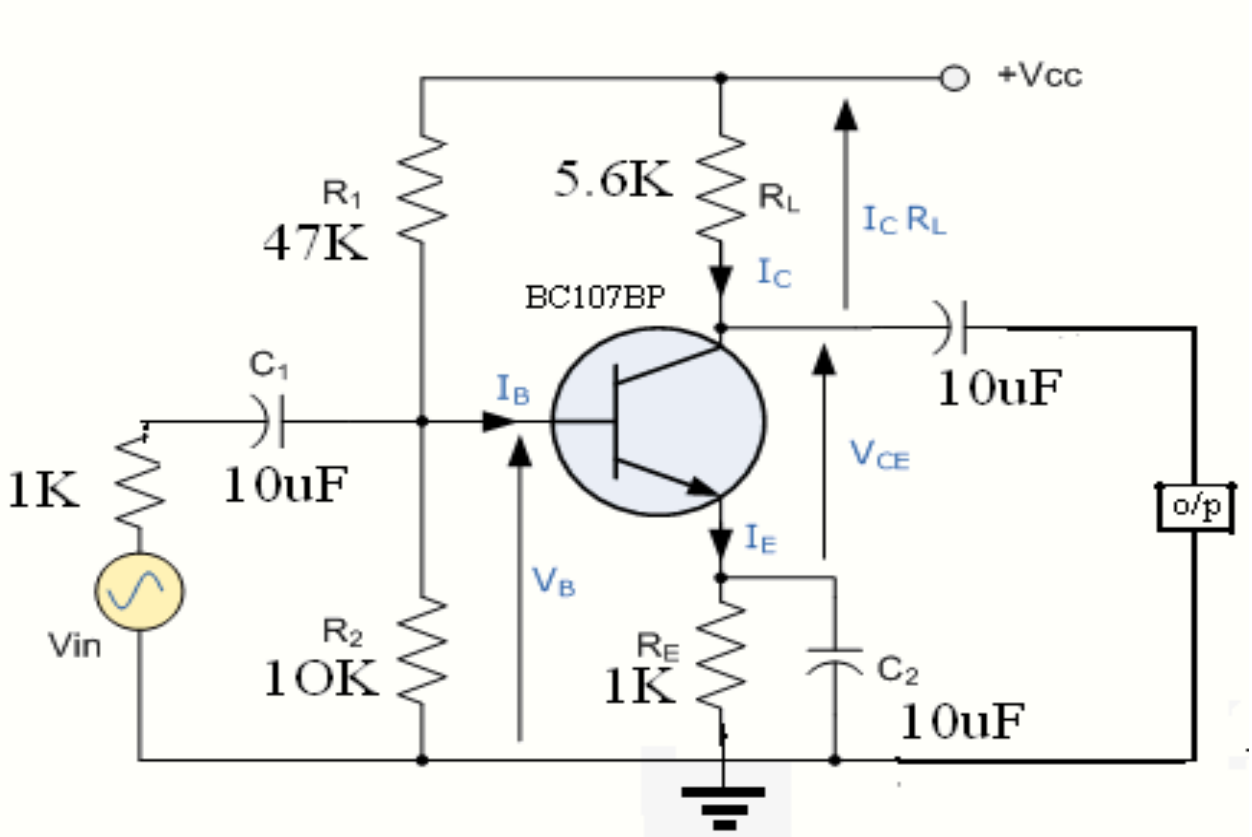
```
V1 2 0 DC 15
RLOAD 3 0 5K
.MODEL MOD1 NPN
.TRAN .02M .78M
.PLOT TRAN V(1,0) V(3,0)
.END
```

RESULT:


(C) cc (active)
4.0V
3.0V
2.0V
1.0V
0V
0s
100us
200us
300us
400us
500us
600us
700us
800us
V(1)
V(3)
time

PROGRAM:5

AIM: To verify the characteristics of **CS** Amplifier

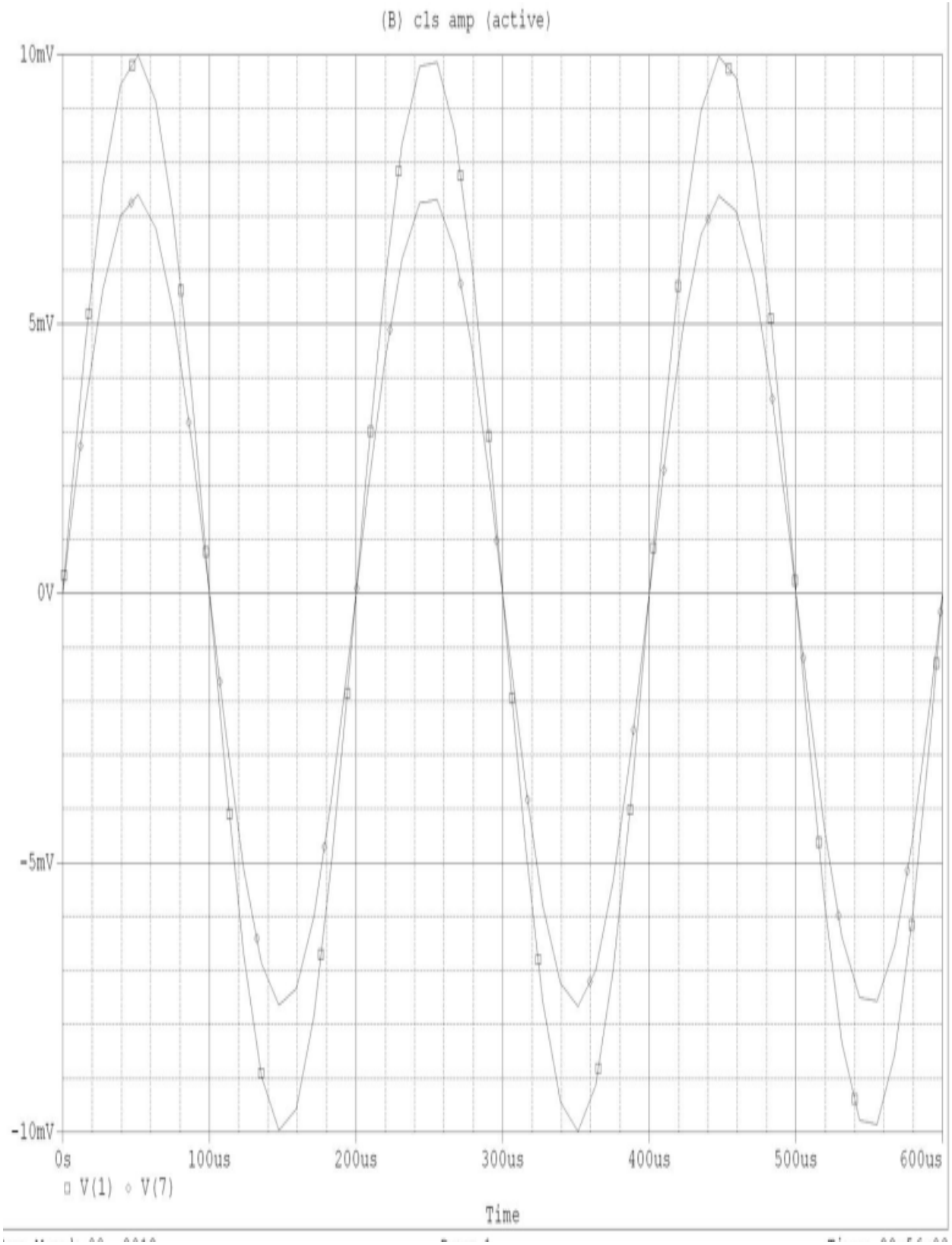


So far we have looked at the bipolar type transistor amplifier and especially the common emitter amplifier, but small signal amplifiers can also be made using **Field Effect Transistors** or **FET's** for short. These devices have the advantage over bipolar transistors of having an extremely high input impedance along with a low noise output making them ideal for use in amplifier circuits that have very small input signals. The design of an amplifier circuit based around a junction field effect transistor or "JFET", (n-channel FET) or even a metal oxide silicon FET or "MOSFET" is exactly the same principle as that for the bipolar transistor circuit used for a Class A amplifier circuit we looked at in the previous experiment. Firstly, a suitable quiescent point or "Q-point" needs to be found for the correct biasing of the JFET amplifier circuit with single amplifier configurations of Common-source (CS), Common-drain (CD) or Source-follower (SF) and the Common-gate (CG) available for most FET devices. These three JFET amplifier configurations correspond to the common-emitter, emitter-follower and the common-base configurations using bipolar transistors..

SPICE FILE

```
VS 1 0 SIN(0 10MV 5KHZ)
R 1 7 15K
CG 7 2 4.7UF
R1 2 0 100K
R2 2 5 1MEG
RS 4 0 1.5K
RD 3 5 4.7K
VDD 5 0 15V
CD 3 6 15UF
CS 4 0 50UF
RL 6 0 20K
JN 3 2 4 BFW10
.MODEL BFW10 NJF
.TRAN 0.1MS 0.6MS
.PROBE
.END
```

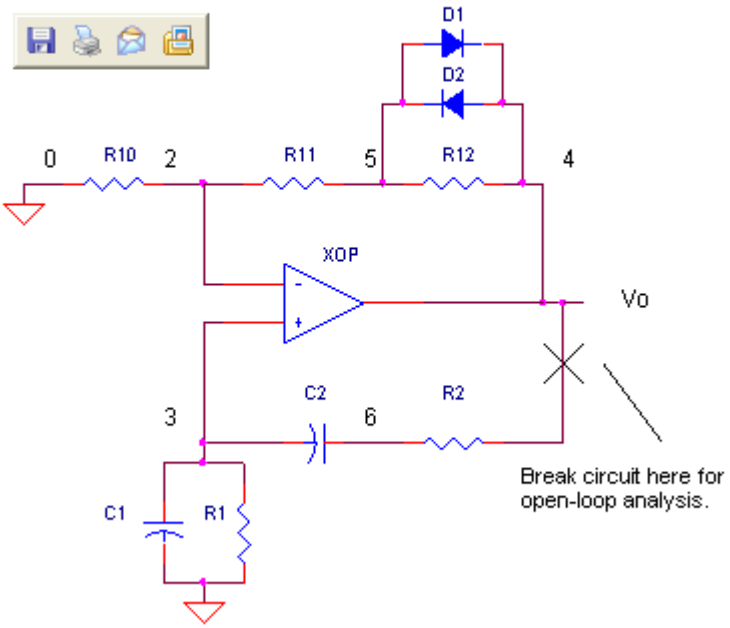
RESULT


(B) cls amp (active)
10mV
5mV
0V
-5mV
-10mV
0s
100us
200us
300us
400us
500us
600us
V(1)
V(7)
Time

PROGRAM:6

AIM: To verify the characteristics of Wein Bridge Oscillator

CIRCUIT



The opamp Wien-bridge oscillator provides a nice view into classic oscillator design using feedback analysis. Feedback analysis reveals if your circuit is stable (well behaved) or unstable (may oscillate). When designing amplifiers (especially high-speed ones), the trick is to avoid the conditions that make the circuit oscillate. When designing oscillators, you strive to achieve those conditions in a predictable way.

FEEDBACK ANALYSIS

Feedback analysis simply means opening the circuit and injecting an AC signal VTEST at one end of the circuit. Then, by looking at the magnitude (gain) and phase (time-shift) of signal as it travels around the opened loop, you can tell whether you've got an amplifier or an oscillator on your hands.

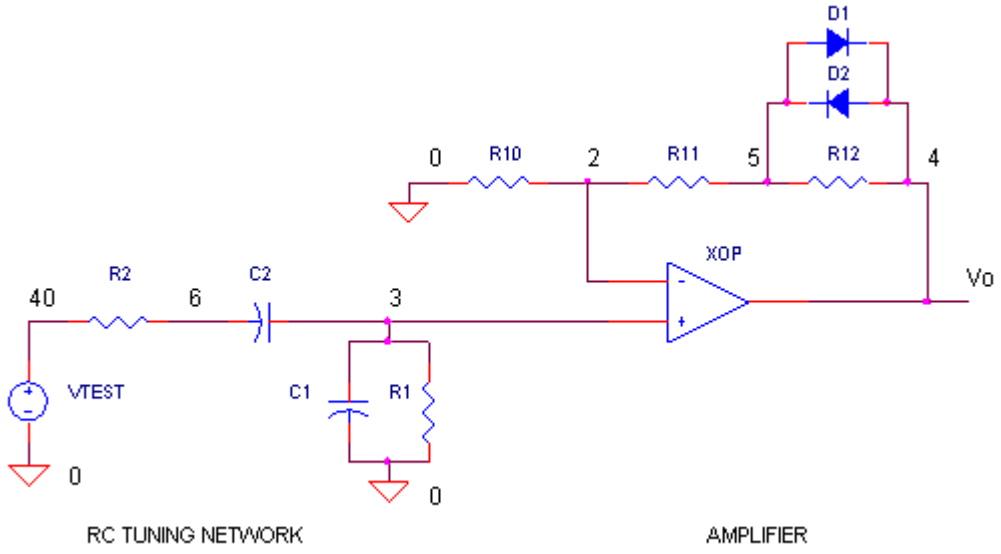
When wearing your oscillator design hat, the idea is to pick components that will make the open-loop analysis meet the **conditions for oscillation** at your chosen frequency: The conditions are as follows:

If the AC gain around the opened loop is **1 V/V** and the total phase shift is **-360 or 0 deg**, the circuit will oscillate at that frequency.

OPENING THE LOOP

Open the loop of the Wien Bridge Oscillator at the op amp's output. This is a good point because of the relatively low impedance of the output terminal. Likewise, VTEST also has a low output impedance. Therefore, opening the loop here does not significantly alter the circuit's behavior.

OPWIEN_OL.CIR (Open-Loop Circuit)



OPWIEN_OL.CIR (Open-Loop Circuit)

RC TUNING NETWORK

Two basic sections form the Wien-bridge oscillator: an RC tuning network and an amplifier. Both are necessary to achieve the conditions for oscillations. The RC network is characterized by a center frequency

$$fo = \frac{1}{2\pi \times R \times C}$$

where R=R1=R2 and C=C1=C2. At the center frequency, two interesting things occur at V(3). First, the phase shift goes through 0 degrees. And second, the magnitude reaches a peak of 1/3 V/V.

CIRCUIT ANALYSIS Run a SPICE simulation of the open-loop circuit **OPWEIN_OL.CIR**. Add trace VM(3) to see what the Magnitude looks like at the center frequency. For R1=R2=10k and C1=C2=16nF, the center frequency should be near 1 kHz. What does the phase look like? Add another plot window and then add trace VP(3) to see the Phase shift. The RC network does a nice job of meeting one of the conditions for oscillation: the phase is 0 degrees at the design frequency.

NON-INVERTING AMPLIFIER

The RC network falls short of the oscillation conditions in that the gain is only 1/3 V/V. How is the gain of 1V/V around the loop to be achieved? As you might have guessed, the non-inverting amplifier provides the needed gain. How much? A gain of 3 V/V makes the total gain **1/3 x 3 = 1 V/V**. Setting the correct op amp gain is critical. Not enough - oscillations will cease. Too much – oscillation amplitude will grow until the output saturates.

What's needed is a mechanism to guarantee oscillations will start (GAIN > 3), yet, limit the gain (GAIN=3) at steady state. Enter our heros - D1, D2 and R12. The circuit adjusts its gain depending on the signal level. For small signals, the diodes do not conduct and the gain is set by

$$GAIN = \left(1 + \frac{R11 + R12}{R10}\right) > 3$$

For larger signals, the voltage across R12 is big enough to make D1 and D2 conduct. The shunt resistance of the conducting diodes effectively reduces the R12 resistance, consequently, reducing the overall gain to GAIN=3.

CIRCUIT ANALYSIS Run a simulation of **OPWIEN_OL.CIR**. View the AC output of the op amp VM(4). For R10=10k, R11=18k and R12=5k, the op amp gain is (1 + (18+5)/10) = 3.3 V/V. This should make the overall open-loop gain equal to 1/3 x 3.3 = 1.1 V/V. Does the peak at VM(4) reach this expected gain?

OSCILLATOR OPERATION

It's time to close the loop and try out the Wien-Bridge Oscillator. Run a simulation of closed-loop circuit **OPWIEN.CIR** and plot the Transient Analysis at V(4). How much time does it take for the amplitude to stabilize?

HANDS-ON DESIGN Design the circuit with a different oscillation frequency. Calculate the values for R and C. (Example: For fo = 10kHz, choose R1=R2=10k and calculate C1=C2=1/(2π x R1 x fo) = 1.6nF.) Test drive your oscillator. If there's too little or too many sinewaves on the plot, adjust the total time of the Transient Analysis to another value like 5 ms by modifying the .TRAN statement to look like

```
.TRAN    0.05MS    5MS
```

If there's no input signal to an oscillator, what starts the oscillations? Current source IS injects a pulse into the RC network to jump start the oscillations. In a real circuit, the large transient at power up will kick the circuit into action.

CIRCUIT INSIGHT What happens if there's not enough gain around the loop? Reduce R12 to 1k making the total loop gain less than 1. Run a simulation. The circuit rings briefly, but there's not enough gain to sustain oscillations.

SPICE FILES

```
OPWIEN_OL.CIR - OPAMP WIEN-BRIDGE OSC, OPEN-LOOP ANALYSIS
*
VTEST     40          0          AC          1
*
* RC TUNING
R2        40          6          10K
C2        6           3          16NF
R1        3           0          10K
C1        3           0          16NF
* NON-INVERTING OPAMP
R10       0           2          10K
R11       2           5          18K
XOP       3 2         4          OPAMP1
* AMPLITUDE STABILIZATION
R12       5           4          5K
*D1       5           4          D1N914
*D2       4           5          D1N914
*
.model    D1N914    D(Is=0.1p Rs=16 CJO=2p Tt=12n Bv=100 Ibv=0.1p)
*
* OPAMP MACRO MODEL, SINGLE-POLE
* connections:      non-inverting input
*                   |   inverting input
*                   |   |   output
*                   |   |   |
.SUBCKT OPAMP1     1   2   6
* INPUT IMPEDANCE
RIN       1           2          10MEG
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN     3 0         1 2        100K
RP1       3           4          1K
```

```
CP1         4           0           1.5915UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER 5 0         4 0         1
ROUT        5           6           10
.ENDS
*
*
* ANALYSIS
.AC         DEC 10    10 10MEG
* VIEW RESULTS
.PRINT      AC          VM(3) VP(3)
.PLOT       AC          VM(3) VP(3)
.PROBE
.END
```

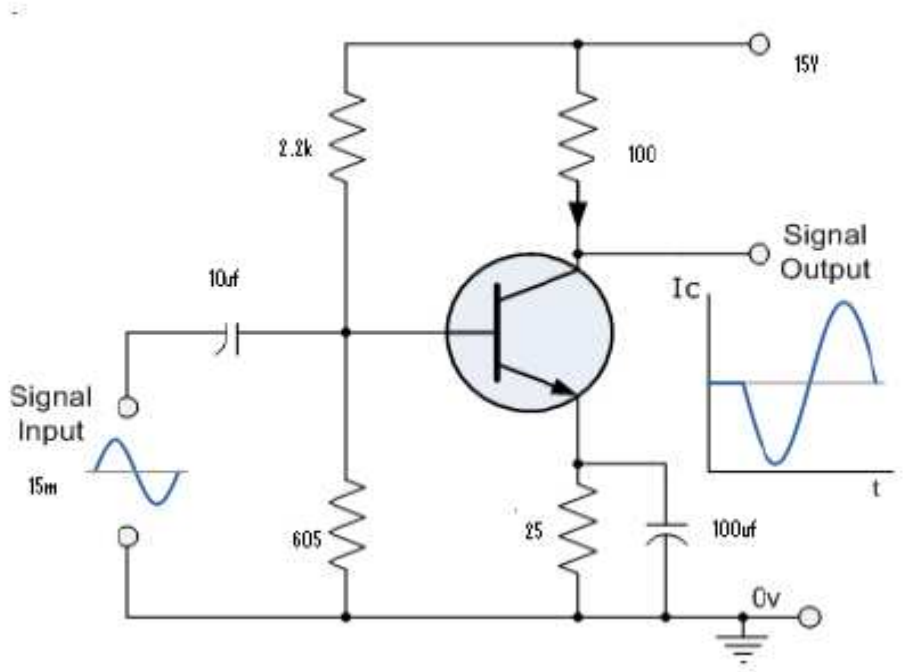
```
OPWIEN.CIR - OPAMP WIEN-BRIDGE OSCILLATOR
*
* CURRENT PULSE TO START OSCILLATIONS
IS          0           3           PWL(0US 0MA   10US 0.1MA   40US 0.1MA   50US 0MA   10MS 0MA)
*
* RC TUNING
R2          4           6           10K
C2          6           3           16NF
R1          3           0           10K
C1          3           0           16NF
* NON-INVERTING OPAMP
R10         0           2           10K
R11         2           5           18K
XOP         3 2         4           OPAMP1
* AMPLITUDE STABILIZATION
R12         5           4           5K
D1          5           4           D1N914
D2          4           5           D1N914
*
.model      D1N914    D(Is=0.1p Rs=16 CJO=2p Tt=12n Bv=100 Ibv=0.1p)
*
* SINGLE-POLE OPERATIONAL AMPLIFIER MACRO-MODEL
* connections:      non-inverting input
*               |   inverting input
*               |   |   output
*               |   |   |
.SUBCKT OPAMP1     1   2   6
* INPUT IMPEDANCE
RIN         1           2           10MEG
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN       3 0         1 2         100K
RP1         3           4           1K
CP1         4           0           1.5915UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER 5 0         4 0         1
```

```
ROUT    5       6       10
.ENDS
*
* ANALYSIS
.TRAN   0.05MS 10MS
*
* VIEW RESULTS
.PRINT  TRAN    V(4)
.PLOT   TRAN    V(4)
.PROBE
.END
```

PROGRAM:7

AIM: To verify the characteristics of CLASS A Power Amplifier

CIRCUIT



An **electronic amplifier** is used for increasing the power of a signal. It does this by taking energy from a power supply and controlling the output to match the input signal shape but with a larger amplitude. In this sense, an amplifier may be considered as modulating the output of the power supply.

SPICE FILE

VS 1 0 SIN(0 5MV 10KHZ)

VCC 5 0 15V

CB 1 2 10UF

CC 3 6 10UF

CE 4 0 100UF

R1 5 2 2.7K

R2 2 0 605

RC 5 3 100

RE 4 0 25

RL 6 0 47

Q1 3 2 4 SL100

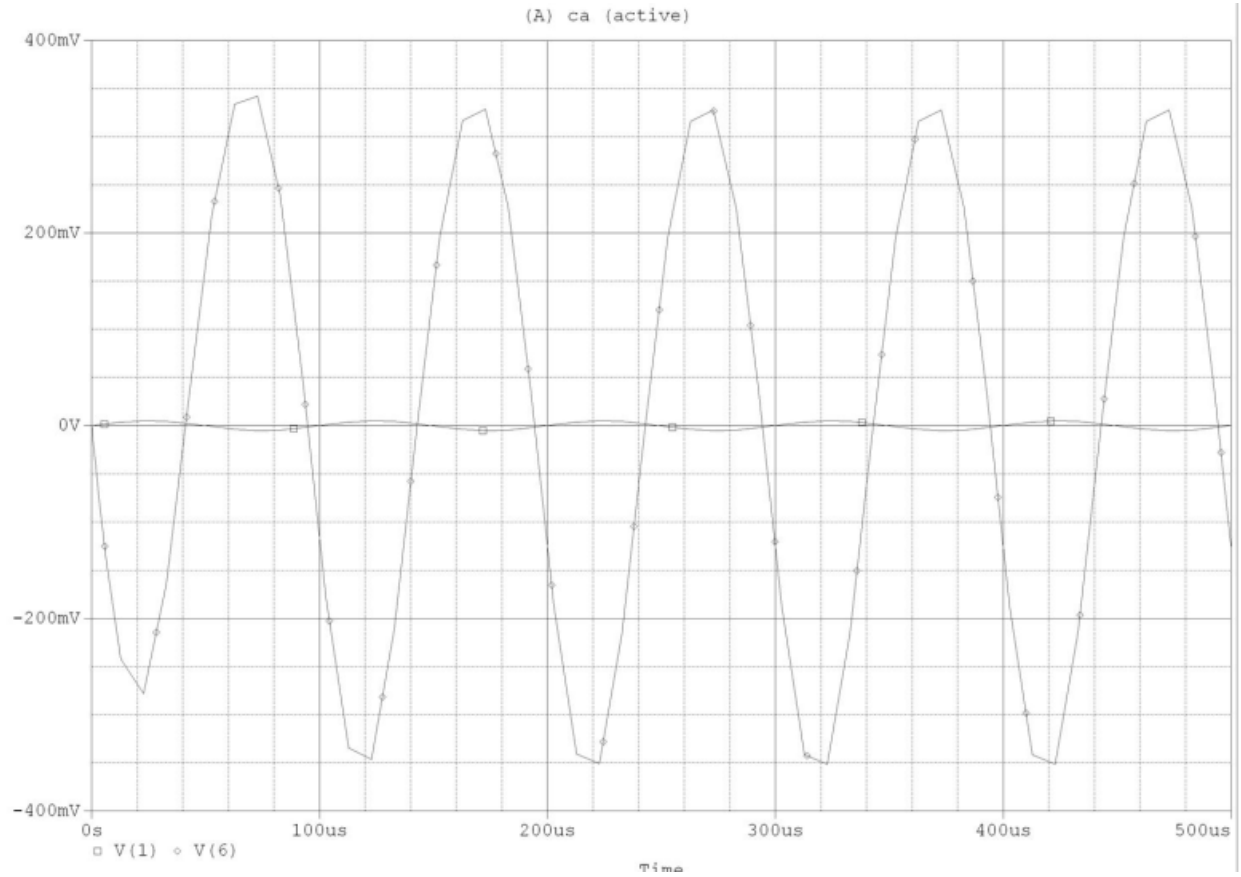
.MODEL SL100 NPN

.TRAN 0.1MS 0.5MS

.PROBE

.END

RESULT



PROGRAM:8

AIM: To verify the characteristics of pre emphasis and De-emphasis circuits

Pre-emphasis

The circuits are the transmitting side of the frequency modulator. It is used to increase the gain of the higher frequency component as the input signal frequency increased, the impendence of the

collector voltage increase. If the signal frequency is lesser then the impendence decrease which increase the collector current and hence decrease the voltage.

4.4.2 De-emphasis

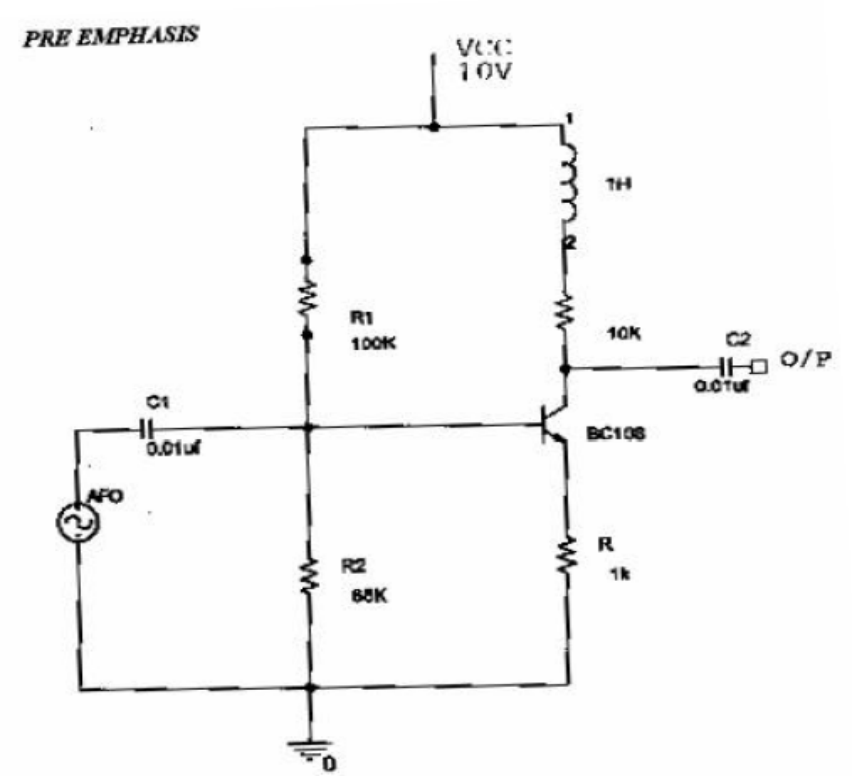
The circuit is placed at the receiving side. It acts as allow pass filter. The boosting gain for higher frequency signal in the transmitting side is done by the pre-emphasis circuit is filtered to the

same value by the low pass filter. The cut off frequency is given by the formula

fc = 1/(2p RC) (4-1)

Where R = 2 p fc L

CIRCUIT



CIRCUIT

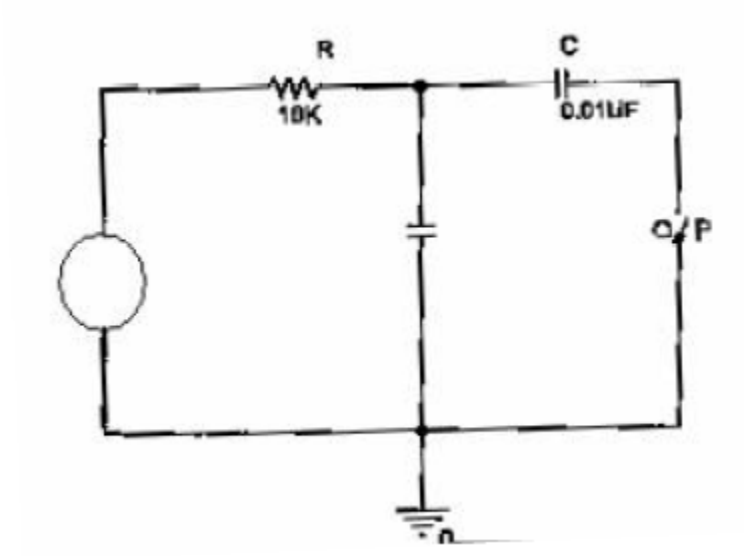
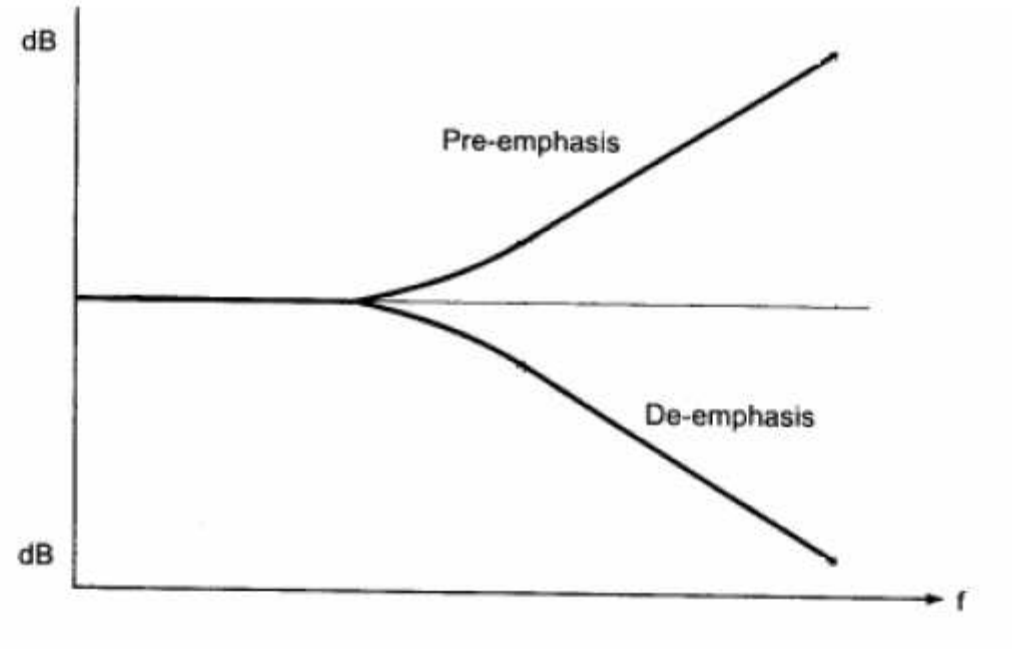


Figure:De emphasis

Model graph



DESIGN FORMULA

f_c = 1/(2 p RC) (assume =R = 10 KO, C = 0.01µf)

R = 2 pf_cL; L=1/(2pf_c)

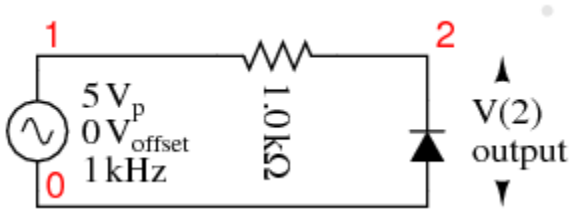
TEST PROCEDURE

1. The circuit connection are made as shown in the circuit diagram for the pre-emphasis and deemphasis
circuits
2. A power supply of 10V is given to the circuit
3. For a constant value of input voltage the values of the frequency is varied and the output is noted on the CRO
4. A graph is plotted between gain and frequency
5. The cut frequencies are practical values of the values of cut off frequency \are found, compared and verified.

PROGRAM:9

AIM: To verify the characteristics of CLIPPERS

CIRCUIT



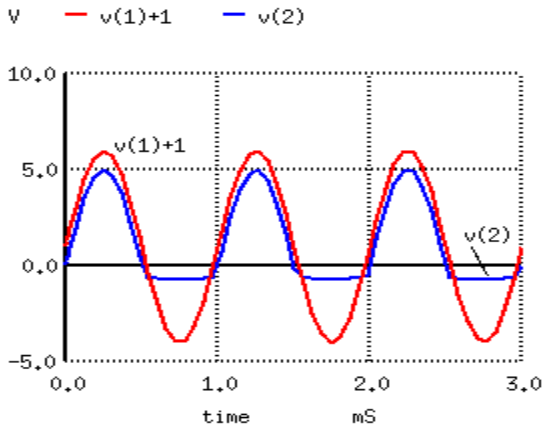
A circuit which removes the peak of a waveform is known as a *clipper*. A negative clipper is shown in Figure above.

During the positive half cycle of the 5 V peak input, the diode is reversed biased. The diode does not conduct. It is as if the diode were not there. The positive half cycle is unchanged at the output V(2) in Figure below. Since the output positive peaks actually overlays the input sinewave V(1), the input has been shifted upward in the plot for clarity.

SPICE FILE

```
D1 0 2 DIODE
R1 2 1 1.0K
V1 1 0 SIN(0 5 1K)
.MODEL DIODE D
.TRAN .05M 3M
.END
```

RESULT:

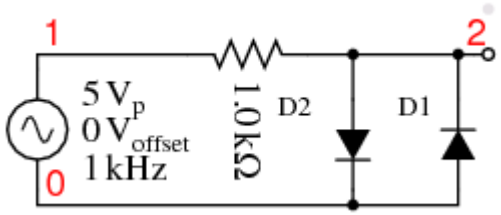


V(1)+1 is actually V(1), a 10 Vptp sine wave, offset by 1 V for display clarity. V(2) output is clipped at -0.7 V, by diode D1.

During the negative half cycle of sine wave input of Figure above, the diode is forward biased, that is, conducting. The negative half cycle of the sine wave is shorted out. The negative half cycle of V(2) would be clipped at 0 V for an ideal diode. The waveform is clipped at -0.7 V due to the forward voltage drop of the silicon diode. The spice model defaults to 0.7 V unless parameters in the model statement specify otherwise. Germanium or Schottky diodes clip at lower voltages.

Closer examination of the negative clipped peak reveals that it follows the input for a slight period of time while the sine wave is moving toward -0.7 V. The clipping action is only effective after the input sine wave exceeds -0.7 V. The diode is not conducting for the complete half cycle, though, during most of it.

CIRCUIT



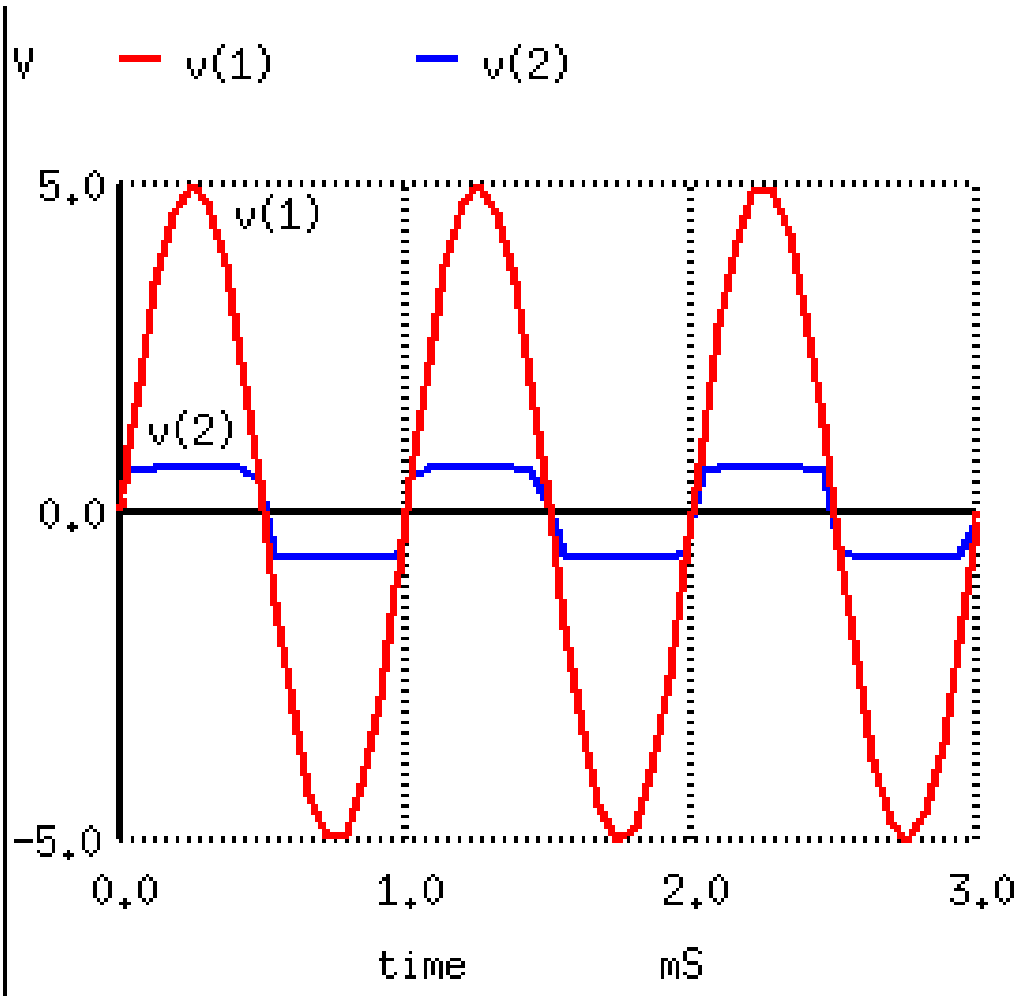
SPICE FILE

D1 0 2 DIODE
D2 2 0 DIODE
R1 2 1 1.0K
V1 1 0 SIN(0 5 1K)

```
.MODEL DIODE D
.TRAN 0.05M 3M
.END
```

Symmetrical clipper: Anti-parallel diodes clip both positive and negative peak, leaving a ± 0.7 V output.

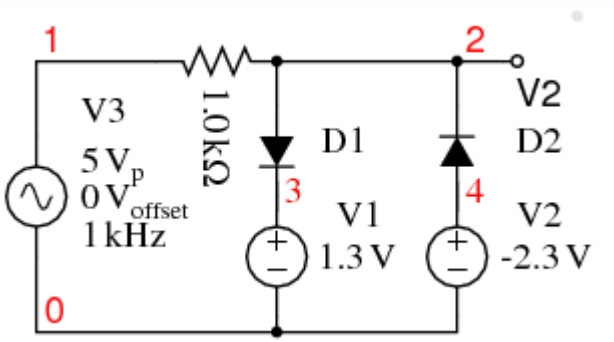
Diode D1 clips the negative peak at -0.7 V as before. The additional diode D2 conducts for positive half cycles of the sine wave as it exceeds 0.7 V, the forward diode drop. The remainder of the voltage drops across the series resistor. Thus, both peaks of the input sinewave are clipped in Figure below.



Diode D1 clips at -0.7 V as it conducts during negative peaks. D2 conducts for positive peaks, clipping at 0.7V.

The most general form of the diode clipper is shown in Figure below. For an ideal diode, the clipping occurs at the level of the clipping voltage, V1 and V2. However, the voltage sources have been adjusted to account for the 0.7 V forward drop of the real silicon diodes. D1 clips at 1.3V +0.7V=2.0V when the diode begins to conduct. D2 clips at -2.3V -0.7V=-3.0V when D2 conducts.

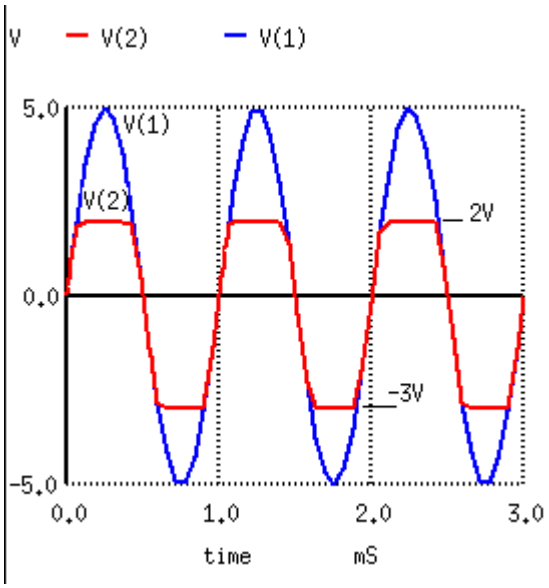
CIRCUIT



SPICE FILE

```
V1 3 0 1.3
V2 4 0 -2.3
D1 2 3 DIODE
D2 4 2 DIODE
R1 2 1 1.0K
V3 1 0 SIN(0 5 1K)
.MODEL DIODE D
.TRAN 0.05M 3M
.END
```

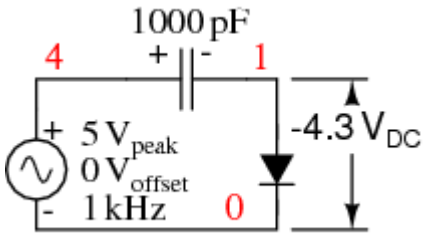
RESULT:


V
V(2)
V(1)
5.0
0.0
-5.0
V(1)
V(2)
2V
-3V
0.0
1.0
2.0
3.0
time
mS

PROGRAM:10

AIM: To verify the characteristics of CLAMPERS

CIRCUIT



The circuits in Figure above are known as *clampers* or *DC restorers*. These circuits clamp a peak of a waveform to a specific DC level compared with a capacitively coupled signal which swings about its average DC level (usually 0V). If the diode is removed from the clamper, it defaults to a simple coupling capacitor– no clamping.

What is the clamp voltage? And, which peak gets clamped? In Figure above the clamp voltage is 0 V ignoring diode drop, (more exactly 0.7 V with Si diode drop). In Figure above, the positive peak of V(1) is clamped to the 0 V (0.7 V) clamp level. Why is this? On the first positive half cycle, the diode conducts charging the capacitor left end to +5 V (4.3 V). This is -5 V (-4.3 V) on the right end at V(1,4). Note the polarity marked on the capacitor in Figure above. The right end of the capacitor is -5 V DC (-4.3 V) with respect to ground. It also has an AC 5 V peak sinewave coupled across it from source V(4) to node 1. The sum of the two is a 5 V peak sine riding on a -5 V DC (-4.3 V) level. The diode only conducts on successive positive excursions of source V(4) if the peak V(4) exceeds the charge on the capacitor. This only happens if the charge on the capacitor drained off due to a load, not shown. The charge on the capacitor is equal to the positive peak of V(4) (less 0.7 diode drop). The AC riding on the negative end, right end, is shifted down. The positive peak of the waveform is clamped to 0 V (0.7 V) because the diode conducts on the positive peak.

SPICE FILE

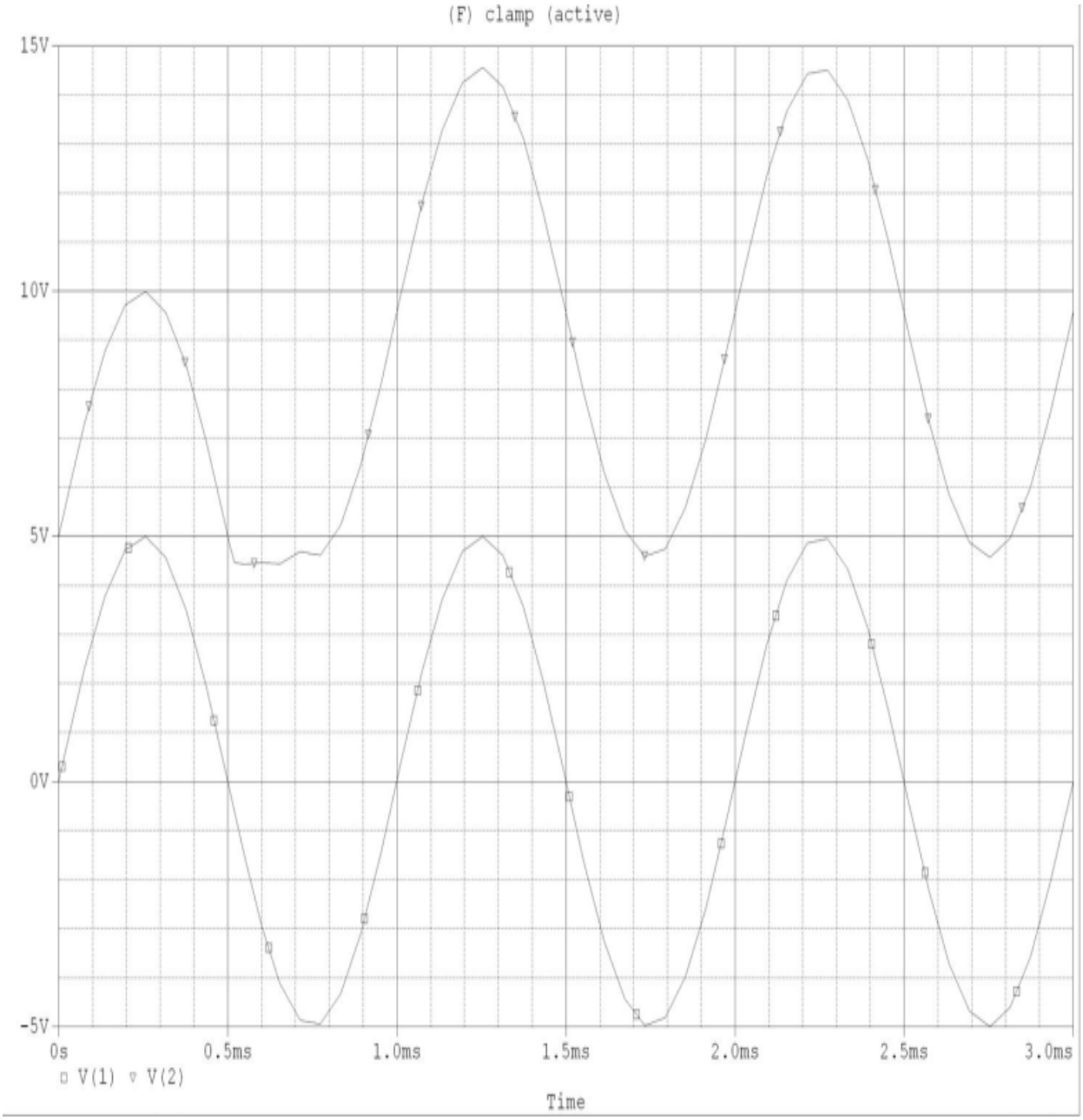
V1 1 0 SIN(0 5 1K)

C 2 1 1000P

D1 3 2 DIODE

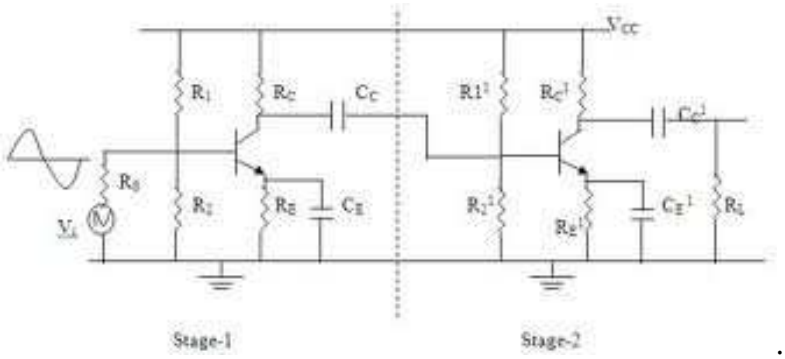
```
V 3 0 5V
.MODEL DIODE D
.TRAN 0.05MS 3MS
.PROBE
.END
```

RESULT:



PROGRAM:11

AIM: To verify the characteristics of RC Coupled Amplifier

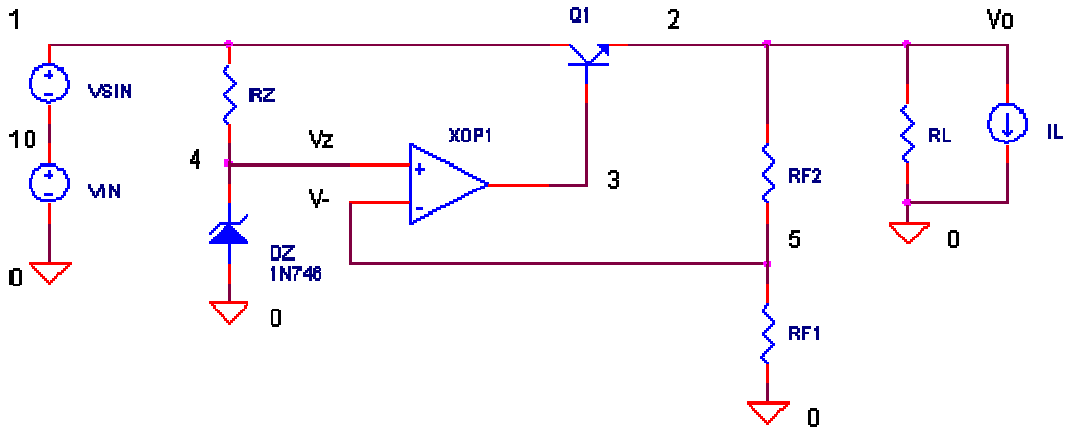


When a.c. signal is applied to the base of the first transistor, it is amplified and developed across the out of the 1st stage. This amplified voltage is applied to the base of next stage through the coupling capacitor C_c where it is further amplified and reappears across the out put of the second stage. Thus the successive stages amplify the signal and the overall gain is raised to the desired level. Much higher gains can be obtained by connecting a number of amplifier stages in succession (one after the other). Resistance-capacitance (RC) coupling is most widely used to connect the output of first stage to the input (base) of the second stage and so on. It is the most popular type of coupling because it is cheap and provides a constant amplification over a wide range of frequencies. The above shows the circuit arrangement of a two stage RC coupled CE mode transistor amplifier where resistor R is used as a load and the capacitor C is used as a coupling element between the two stages of the amplifier.

PROGRAM:12

AIM: Op Amp Regulator with Series-Pass Transistor

CIRCUIT



OPREG.CIR

What is the function of a voltage regulator circuit? It's basically this - maintain a precise voltage regardless of the current drawn by the load. Three basic components are needed to achieve good voltage regulation.

1. A precision reference (zener diode) to set the output voltage.

2. A muscle component (transistor) to deliver the required current.

3. An automatic controller (opamp) to adjust the transistor drive. The "prime directive" of the op amp is to adjust the base drive of Q1 delivering the required load current while keeping the output voltage at a fixed value.

OUTPUT VOLTAGE

Resistors RF1 and RF2 feed a fraction of the regulator output Vo to the op amp's negative input V-. The op amp then adjusts the drive to Q1 such that V- is equal to the zener voltage Vz. When this occurs, the output voltage is related to the zener voltage through the RF1, RF2 divider by

$$Vo = Vz \times (1 + \frac{RF2}{RF1})$$

With the zener voltage at about 3V and RF2=10k, RF1=5K, the output voltage should be 3 x (1+10/5) = 9V. Run a simulation. What is the output voltage at V(2)?

HANDS-ON DESIGN Suppose you're asked to design a 12V regulator. What value of RF2 would you need with Vz = 3V? Choose a new RF2 and test drive your circuit.

LOAD REGULATION

How well does the regulator perform? One test is to apply a change in the load current and see how well the regulator maintains its output voltage.

Current source IL generates a 1A pulse starting at 10ms and ending at 20ms. Place IL in the circuit by removing the "*" at the beginning of the IL statement. Run a simulation and plot the load current by adding trace I(IL) to the plot window.

The output should not change much except for the appearance of 2 small spikes. These spikes show that the regulator takes some finite time to respond when the load current changes.

CIRCUIT INSIGHT Want to see the automatic controller (op amp) in action? Plot the Q1 base voltage V(3) to see the op amp increase the transistor on-voltage when the during the 1A pulse. You can also see the op amp achieve its prime directive of maintaining V- = Vz by plotting V(4) and V(5).

LINE REGULATION

How well does the regulator hold the output voltage as the input voltage changes? The input voltage is a combination of VIN (DC source at 15V) and VS (AC sinewave currently set to 0V peak). To test the regulators line regulation, set VS to 1V peak by editing the VS statement to look like

```
VS    1     10    SIN(0  1  1KHZ)
```

Run a simulation and check how much variation appears at V(2). What causes these variations? One factor is the change in zener voltage V(4) due to a change at V(1). As V(1) varies, the current through RZ and consequently the zener diode voltage also varies.

SIMULATION NOTE

There are two semiconductors modeled here, zener diode D1N746 and transistor Q1. The diode parameters,(Is=5u Rs=14 Bv=2.81 Ibv=5u), came from the manufacturer's web site. Actually there are more parameters than these four listed. The unlisted ones get set to their default parameters. For the simple transistor Q1 used, all of the default parameters are used except the current gain BF = 100.

CIRCUIT INSIGHT You can view Q1's base current by adding IB(Q1) to the plot window. How much base current is required during the 1A draw of the load? The op amp supplies this current to the transistor. However, many op amps can only deliver about 10mA! If Q1 is asking for more, you may need to get an op amp with more current output muscle or a transistor with greater current gain BF. Set BF to a higher value like 200 and check IB(Q1) during the 1A load pulse.

SPICE FILE

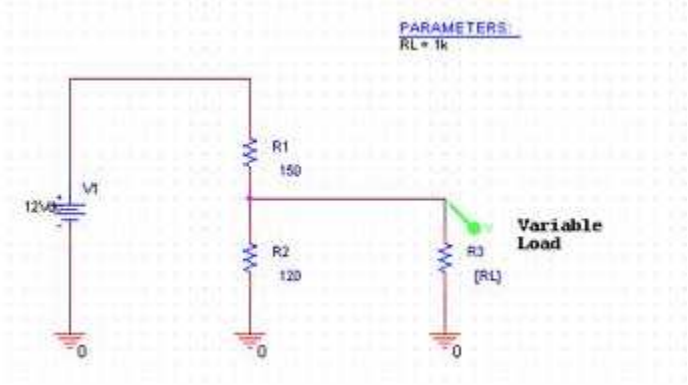
```
OPREG.CIR - OPAMP VOLTAGE REGULATOR W/ SERIES-PASS TRANSISTOR
*
* INPUT VOLTAGE (VSIN FOR TEST ONLY)
VIN     10      0       DC      15
VSIN    1       10      SIN(0 0 1KHZ)
* SERIES TRANSISTOR
Q1      1 3     2       QNOM
* REFERENCE VOLTAGE
RZ      1       4       5K
DZ      0       4       D1N746
* OPAMP CONTROLLER
XOP1    4 5     3       OPAMP1
RF2     2       5       10K
RF1     5       0       5K
* LOAD
RL      2       0       100
*IL     2       0       PWL(0 0  10MS 0   10.1MS 1   20MS 1   20.1MS 0   30MS
0)
*
.model  QNOM    NPN(BF=100)
.model  D1N746  D(Is=5u Rs=14 Bv=2.81 Ibv=5u)
*
* * OPAMP MACRO MODEL, SINGLE-POLE
* connections:      non-inverting input
*                   |   inverting input
*                   |   |   output
*                   |   |   |
.SUBCKT OPAMP1      1   2   6
* INPUT IMPEDANCE
RIN     1       2       10MEG
* GAIN BANDWIDTH PRODUCT = 10MHZ
* DC GAIN (100K) AND POLE 1 (100HZ)
EGAIN   3 0     1 2     100K
RP1     3       4       1K
CP1     4       0       1.5915UF
```

```
* OUTPUT BUFFER AND RESISTANCE
EBUFFER 5 0     4 0     1
ROUT    5       6       10
.ENDS
*
* ANALYSIS
.TRAN   0.05MS 30MS
* VIEW RESULTS
.PRINT TRAN    V(2)
.PLOT   TRAN    V(2)
.PROBE
.END
```

PROGRAM:13

AIM: To verify the characteristics of ATTENUATOR

CIRCUIT

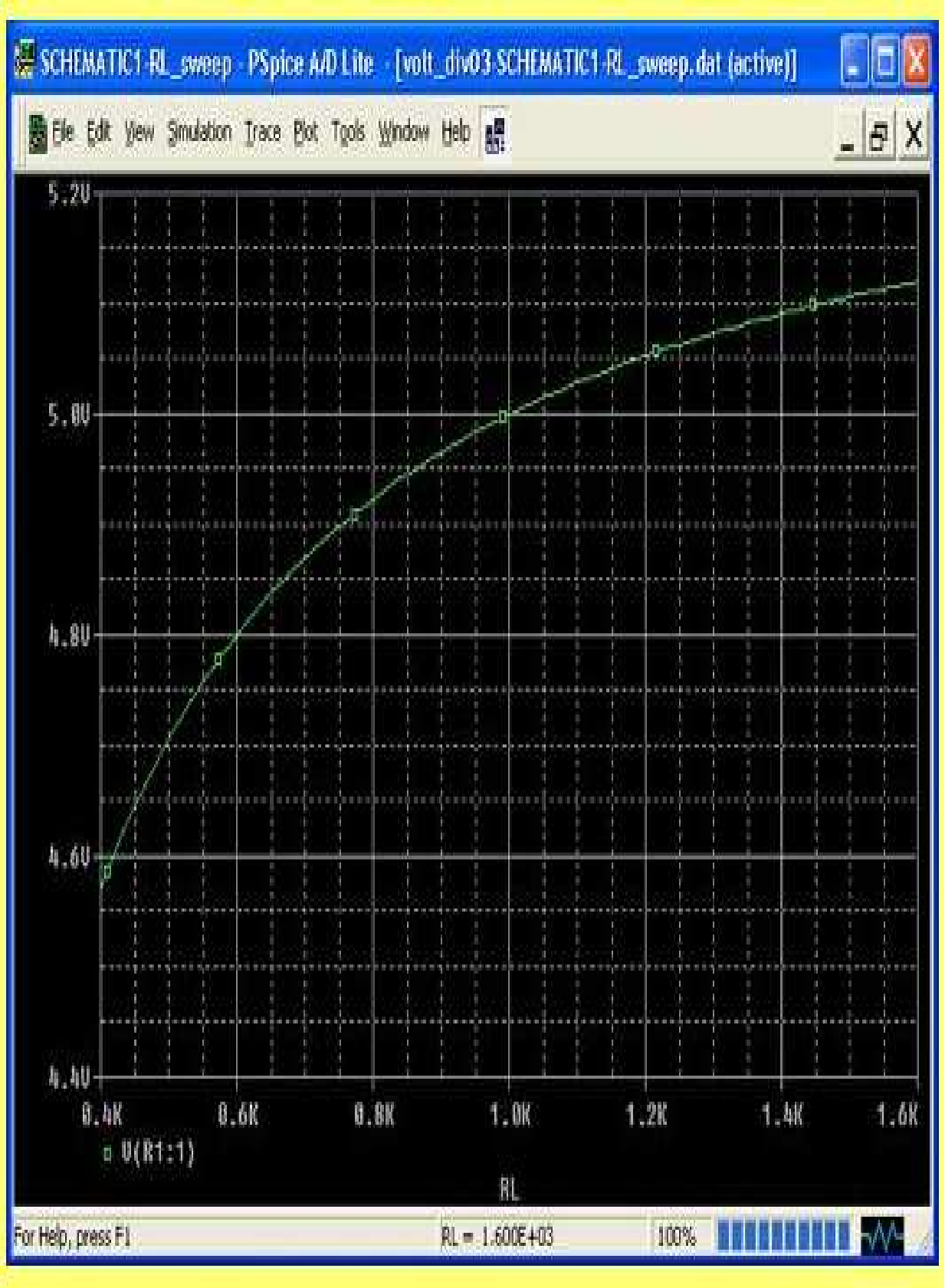


An **attenuator** is an electronic device that reduces the amplitude or power of a signal without appreciably distorting its waveform.

An attenuator is effectively the opposite of an amplifier, though the two work by different methods. While an amplifier provides gain, an attenuator provides loss, or gain less than 1.

Attenuators are usually passive devices made from simple voltage divider networks. Switching between different resistances forms adjustable stepped attenuators and continuously adjustable ones using potentiometers. For higher frequencies precisely matched low VSWR resistance networks are used.

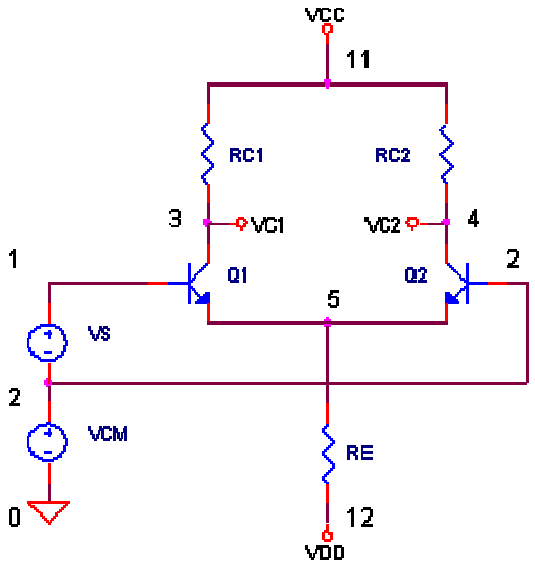
Fixed attenuators in circuits are used to lower voltage, dissipate power, and to improve impedance matching. In measuring signals, attenuator pads or adaptors are used to lower the amplitude of the signal a known amount to enable measurements, or to protect the measuring device from signal levels that might damage it. Attenuators are also used to 'match' impedances by lowering apparent SWR.


SCHEMATIC1-RL_sweep - PSpice A/D Lite - [volt_div03 SCHEMATIC1-RL_sweep.dat (active)]
File Edit View Simulation Trace Plot Tools Window Help
5.2V
5.0V
4.8V
4.6V
4.4V
0.4K
0.6K
0.8K
1.0K
1.2K
1.4K
1.6K
V(R1:1)
RL
For Help, press F1
RL = 1.600E+03
100%

PROGRAM:14

AIM: To verify the characteristics of Differential Amplifier

CIRCUIT



BJT_DIFFAMP1.CIR

Look under the hood of most op amps, comparators or audio amplifiers, and you'll discover this powerful front-end circuit - the differential amplifier. A simple circuit able to amplify small signals applied between its two inputs, yet reject noise signals common to both inputs. This circuit has a unique topology: two inputs and two outputs. Although you can tap the signal from one output only, taking the difference between both outputs delivers twice the gain! And it improves Common-Mode Rejection (CMR), an essential function when the common-mode signal is a noise source or DC bias from a previous stage.

GAIN AND REJECTION

How does this amplifier amplify differential signals and reject common ones? The bias condition assumes equal voltages at VB1 and VB2, forcing the bias current IE (set by RE) to split equally between the transistors resulting in IC1 = IC2. With RC1 = RC2, equal voltages develop at VC1 and VC2.

DIFFERENTIAL GAIN

Now suppose a differential signal is applied to the inputs. This will incrementally increase and decrease the base voltages to

$$VB1 + \Delta V \text{ and } VB2 - \Delta V$$

Because Q1 conducts a little more and Q2 a little less, IE now splits unevenly creating

$$IC1 > IC2$$

This, in turn, forces the voltage at VC1 to decrease and VC2 to increase. The result: a voltage change at each output due to a differential input.

COMMON-MODE REJECTION

Now suppose a common-mode input signal is applied. We incrementally increase both inputs to

$$VB1 + \Delta V \text{ and } VB2 + \Delta V$$

Because the conduction level of neither transistors has changed (both bases and emitters moved by the same amount), the collector currents did not change.

$$IC1 = IC2 \approx IE / 2.$$

Subsequently, the voltages at VC1 and VC2 remain the same! Therefore, the circuit has rejected a signal common to both inputs.

Well, the last statement is *almost* true. Actually, a change in emitter voltage had a small ill effect. It changed the bias current IE set by RE. And this directly impacted $IC1 = IC2 \approx IE / 2$, slightly shifting the levels at VC1, VC2. As you can see the rejection is not perfect. However, it can still be effective at removing a large part of noise or a DC bias common to both inputs.

DIFFERENTIAL GAIN

How do we calculate the differential voltage gain? You can think of Q1 and Q2 as current sources controlled by their base voltages. RC1 and RC2 then convert the currents back into voltages. First, the small signal collector current

$$i_C = gm \cdot v_B$$

where the transconductance gm (A / V) is set by the DC collector current
$gm = Ic / V_T = Ic / 25\ mV$ at room temperature. Then, R_C transforms i_C back to a voltage

$$v_C = R_C \cdot gm \cdot v_B$$

Getting the input VS into the picture, notice it divides equally across each base-emitter junction, but with opposite polarities. Putting it all together you get a **single-ended output** for each transistor

$$v_{C1} = R_{C1} \cdot gm \cdot +VS / 2$$

$$v_{C2} = R_{C2} \cdot gm \cdot -VS / 2$$

Subtracting the two outputs gets you a **differential output** of

$$v_{C1} - v_{C2} = R_C \cdot gm \cdot VS$$

What about the bias current? RE sets the bias at Ie = (-0.6V - VDD) / RE = (-0.6 V - (-15 V)) / 7.2 k = 2 mA which divides equally between Q1 and Q2 giving

$$Ic1 = Ic2 \approx Ie / 2 \approx 1\ mA$$

Finally, we easily calculate $gm = 1\ mA / 25\ mV = 0.04\ A/V$. The single-ended gain becomes

$$v_{C1} / VS = R_{C1} \cdot gm \cdot 1/2$$
$$= 1\ k \cdot 0.04 \cdot 1/2$$
$$= 20\ V/V$$

CIRCUIT INSIGHT Run a simulation of BJT_DIFFAMP1.CIR. For VS = 10 mV peak, do you see about 200 mV peak at V(3)? Check out the signal at V(4). Is it equal and opposite to V(3)? To double the gain, remove traces V(3) and V(4) and plot the difference between the two outputs:
V(3)-V(4) or V(3,4).

HANDS-ON DESIGN How can you adjust the gain? Notice, that RE sets Ic, which determines gm, which directly sets the gain. So to decrease the gain by a factor of 2 or 3, for example, just increase RE by a factor of 2 or 3. Looking at the output equation, how else can you adjust gain? Try adjusting the values of RC1 and RC2 to vary the gain.

COMMON MODE REJECTION

CIRCUIT INSIGHT To see the CMR in action, zero the signal source by setting VS to 0MVPEAK. Then turn up VCM to something like 100MVPEAK. Run a new simulation. What happens at both
V(3) and V(4)? Notice the output voltages are very small! And to boot, they move in the same direction. This can work in our favor if we're able to take the difference between outputs, V(3,4).

This *differential output* further improves the CMR! Now, try mismatching the RCs by a percent or two and watch what happens at V(3,4).

In practice, how do you take the difference? Simply follow a differential amplifier with another differential amplifier. Or, like in op amp circuits, subtract the collector currents directly using additional transistors to mirror current from one collector to another. (A future design topic to be sure.)

HOW MUCH DISTORTION?

HANDS-ON DESIGN How big can VS be before the output becomes distorted. Restore VS back to 10MVPEAK and set VCM to 0MVPEAK. Rerun the diff amp simulation and plot V(3,4). Okay, it looks pretty normal. Now, turn VS up to something like 20, 50 or 100 mV. What's happening to the natural beauty of the output sinewave?

Want a better view of the input / output transfer curve? You're not limited to plotting time on the X-axis. In fact, you can change it to a different variable. (Most simulators let do this by clicking on the X-Axis or via a pull-down menu item.) Try plotting V(3,4) on the Y-Axis and V(1) on the X-Axis. How much of this input / output curve is actually a straight line?

THD

If you're interested, SPICE can calculate the Total Harmonic Distortion (THD). For example, including the statement

```
.FOUR 10KHZ V(3,4)
```

asks SPICE to calculate the percentage of higher harmonics to the 10 kHz fundamental sinewave in the waveform at V(3,4). If its all 10 kHz fundamental and no harmonics, you've got pure sinewave dancing at the output. However, as is typical in most amplifiers, the larger signal, the more distorted it gets.

Run a few simulations while increasing VS beyond 10 mV. Checkout the THD results appearing in the in the output text file**, BJT_DIFFAMP1.OUT**.

VOLTAGE-CONTROL AMPLIFIER

The differential amplifier makes a handy Voltage-Controlled Amplifier (VCA). All you need to do is vary the emitter bias current (which of course varies the transistor's transconductance.) How? One way is to replace the -15 VDC supply with a voltage source that varies. For example, use a PWL statement to linearly ramp VDD slowly (say over 1000us) from -5 V to -15 V. Does the output at V(3,4) increase over time? Remember to increase the total time for the transient analysis as needed.

LEVEL SHIFTING

The current-source nature of the transistor's output provides a big benefit. You can shift the output to different voltage levels. If the next stage needs a voltage biased around 25 V, for example, simply change VCC to a higher voltage. Although the output DC bias voltage will be higher, the gain should remain basically the same.

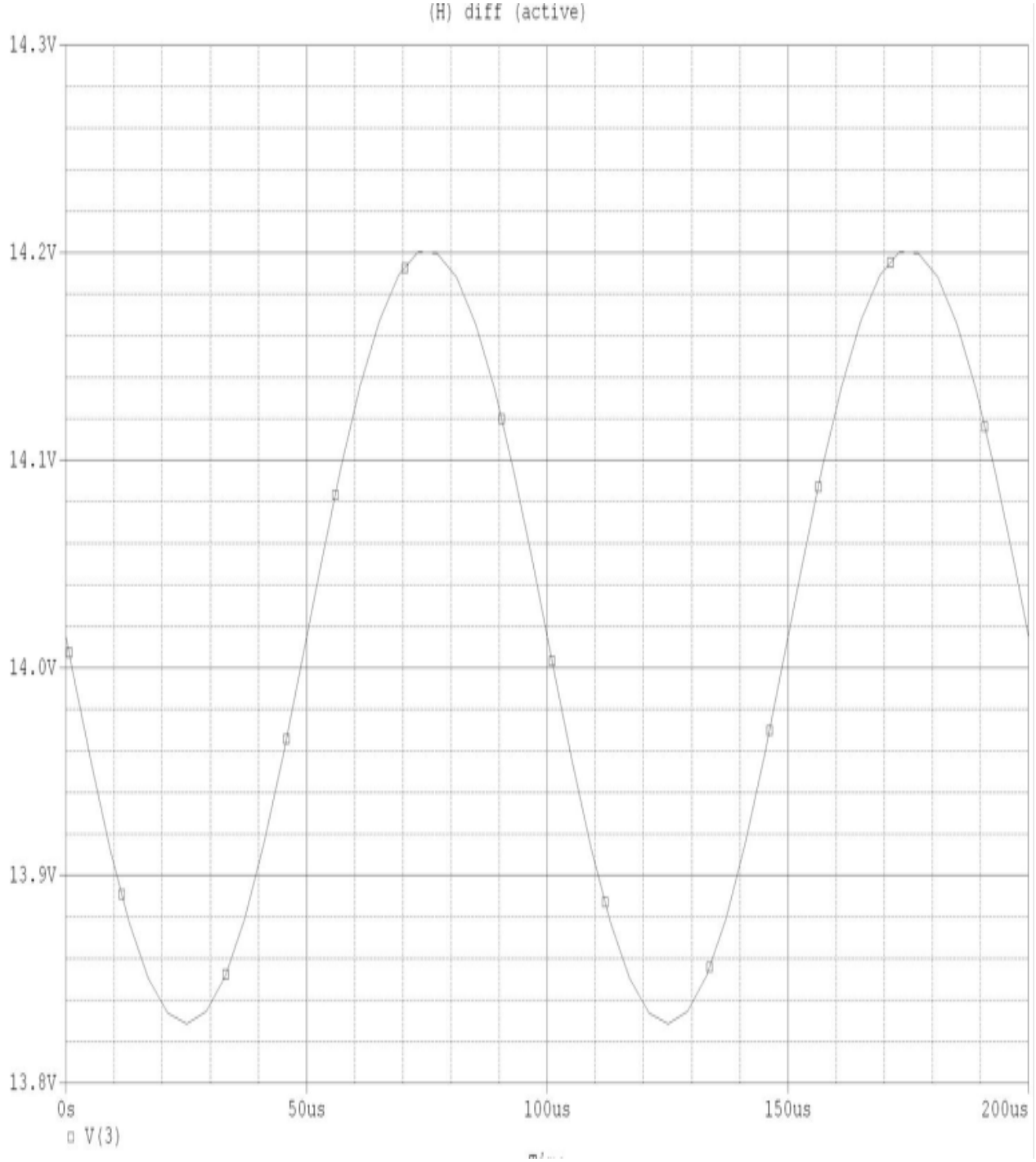
You can also shift the output to a negative rail! Just flip the entire circuit upside down and swap the NPN transistors for PNPs. Many op amps and audio amps shift the output to the negative rail, delivering the signal to the next stage, the Miller Integrator.

SPICE FILE

```
BJT_DIFFAMP1.CIR - BJT DIFFERENTIAL AMPLIFIER
*
* SIGNAL SOURCE
VS      1       2       AC      1       SIN(0   10MVPEAK        10KHZ)
VCM     2       0       SIN(0   0MVPEAK 5KHZ)
*
* POWER SUPPLIES
VCC     11      0       DC      +15V
VDD     12      0       DC      -15V
*
Q1      3 1     5       Q2N2222
Q2      4 2     5       Q2N2222
RC1     11      3       1000
RC2     11      4       1000
RE      5       12      7.2K
*
*
.model Q2N2222  NPN(Is=3.108f Xti=3 Eg=1.11 Vaf=131.5 Bf=217.5 Ne=1.541
+               Ise=190.7f Ikf=1.296 Xtb=1.5 Br=6.18 Nc=2 Isc=0 Ikr=0 Rc=1
+               Cjc=14.57p Vjc=.75 Mjc=.3333 Fc=.5 Cje=26.08p Vje=.75
+               Mje=.3333 Tr=51.35n Tf=451p Itf=.1 Vtf=10 Xtf=2 Rb=10)
*
*
* CHECK DISTORTION WITH FOURIER SERIES ANALYSIS
.FOUR 10KHZ V(3,4)
*
* ANALYSIS
```

```
.TRAN   5US  200US
.AC     DEC     5 1K 100MEG
*
* VIEW RESULTS
.PRINT  TRAN    V(3)
.PRINT  AC      V(3)
.PROBE
.END
```

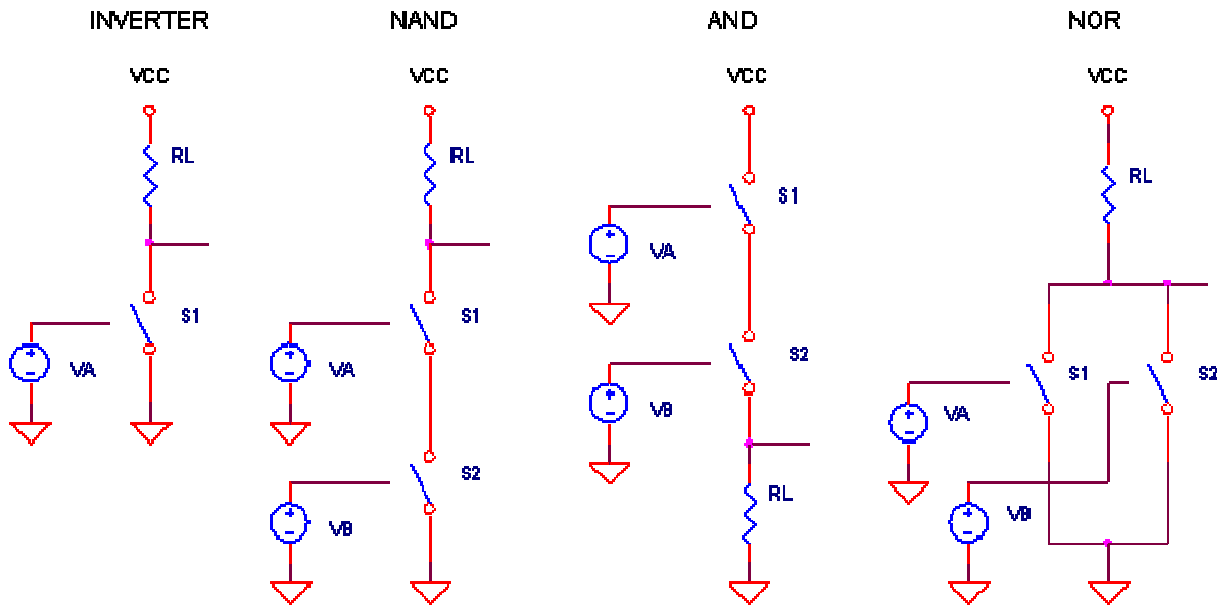
RESULT:


(H) diff (active)
14.3V
14.2V
14.1V
14.0V
13.9V
13.8V
0s
50us
100us
150us
200us
V(3)

PROGRAM: 15

AIM: To verify the characteristics of *Basic Digital Gates*

CIRCUIT



LOGIC_SW.CIR

You're simulating a circuit, it requires several digital gates, but you don't have a mixed-mode simulator. What to do? One solution involves creating simplified versions of the logic functions. To do this, we look to the NMOS transistor implementation of logic gates where the transistor acts like a voltage-controlled switch. But, instead of the transistor, we'll use the SPICE switch. Just like the transistor, the switch is defined to turn ON when the input voltage goes HI.

By placing the these switches in parallel or series, a variety of basic logic functions can come to life. Here's some helpful hints for logic circuit building:

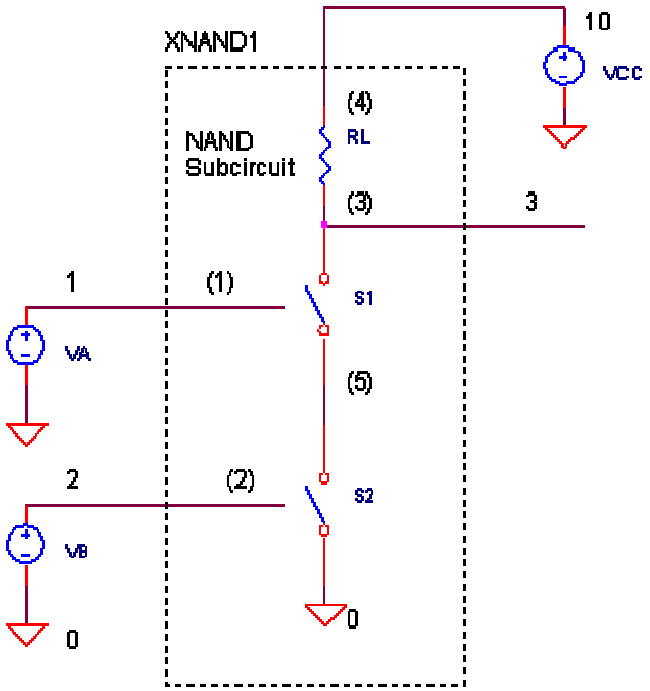
FUNCTION	***OUTPUT***
AND - Switches in Series	INVERTED - Pull-Up Resistor
OR - Switches in Parallel	NON-INVERTED - Pull-Down Resistor

THE NAND GATE

So let's have a go at simulating the NAND gate. How do you describe its function? When both A and B are HI, the output is LO. Or stated another way - it's the AND function with an inverted output. The Boolean expression looks like

$$Y = \overline{A \cdot B}$$

The circuit appears below. S1 and S2 in series create the AND function; RL in the pull-up position inverts the output. Defining the NAND gate as a subcircuit makes it easy to insert it into a few locations if you wish. The subcircuit nodes are listed in parenthesis.



S1 and S2 are defined by RON = 10 Ω and ROFF = 1 MΩ. Compared to the other resistances in the circuit, these should look like an ideal switches. More on the SPICE switch below.

CIRCUIT INSIGHT Simulate the SPICE circuit named LOGIC_SW.CIR. VA and VB create two binary signals that form the sequence 00, 01, 10 and 11. VCC = +5V supplies power to the logic gate. Plot the inputs V(1), V(2) and the output V(3). For a clearer view, you might want to plot V(3) in a separate plot window. Does the output go LO when V(1) and V(2) are HI?

Note the finite rise and fall times of V(1) and V(2). You may have also noticed that the output V(3) quickly changes when the inputs pass through 2.5 V. This is the approximate logic threshold level defined for the SPICE switches.

OTHER GATES

You can test drive some of the other gates defined in SPICE file. Place an asterisk * in front of the NAND statement and call one of the other gates. Simulating the XNOR gate, for example, would like this.

```
*XNAND1 1 2 3 10 NAND
XNOR1 1 2 3 10 NOR
```

After running a simulation, plot the inputs V(1), V(2) and output V(3). Does the output NOR gate go LO when either A or B are HI?

HANDS-ON DESIGN Try your hand at creating a gate such as the OR function. It might be easier if you make a copy of an existing subcircuit, like the NOR gate, then change it as needed. As a design guide, refer to table at the top of the page.

3-INPUT GATES

HANDS-ON DESIGN What if your circuit calls for a three-input device? Just draw the three input circuit, label the nodes and create the SPICE netlist. The device and subcircuit definition for a three-input NAND gate might look something like

```
XNAND1  1 2 3 4  10  NAND3

.SUBCKT NAND3 1 2 3 4  5
* TERMINALS A B C OUT VCC
   .
   . (circuit goes here)
   .
.ENDS
```

where nodes 1, 2, 3 = inputs, node 4 = output and node 5 = VCC. Remember to add a third input signal VC (creating a binary sequence 000, 001, ..., 111 using VA, VB and VC).

```
VC 3 0 PULSE(5V 0V 0NS 10NS 10NS 390NS 800NS)
```

and extend the simulation by a factor of two.

```
.TRAN 5NS 800NS
```

When you're ready to test your circuit, run a simulation, plot the inputs V(1), V(2), V(3) and the output V(4). You might get a better view by plotting V(4) in a separate plot window. Does the output go LO only when all inputs are HI?

ADDING GATE DELAY

You could run into trouble when running a transient analysis on devices with fast transitions. SPICE algorithms may fail under these conditions. This is especially true with complex circuits having feedforward or feedback paths. (Like RS flip-flops created from NAND gates.) The solution is to sprinkle a little RC delay on the devices slowing the transitions enough to where SPICE successfully computes the simulation.

HANDS-ON DESIGN You can include 10 pF in the NAND gate output by adding the following statement in the subcircuit.

```
CL 3 0 10PF
```

Run a simulation and plot the output V(3). Can you see the slowed transitions at the output? You may have noticed the rising edge is slower than the falling edge. That's because the RC time-constant is defined by RL = 500 Ω ohms when the switch is OFF and RON = 10 Ω when the switch is ON.

FURTHER ADVENTURES

By combining gates, you can create more complex functions like the Exclusive-OR gate. Knowing the XOR output is 1 when (A,B) = (0,1) or (1,0), you can write the Boolean expression as

$$A \oplus B = \overline{A} \cdot B + A \cdot \overline{B}$$

How can you wire up several gates (AND, OR and NOT) to accomplish the XOR function?

SIMULATION NOTES

S1 and S2 are voltage controlled switches. These handy SPICE components let you define the ON and OFF resistances and corresponding control voltages. Switches are defined by two statements: the device itself and its model.

```
S1  3 5  1 0  SW

.MODEL SW VSWITCH(VON=2.6 VOFF=2.4 RON=10 ROFF=1MEG)
```

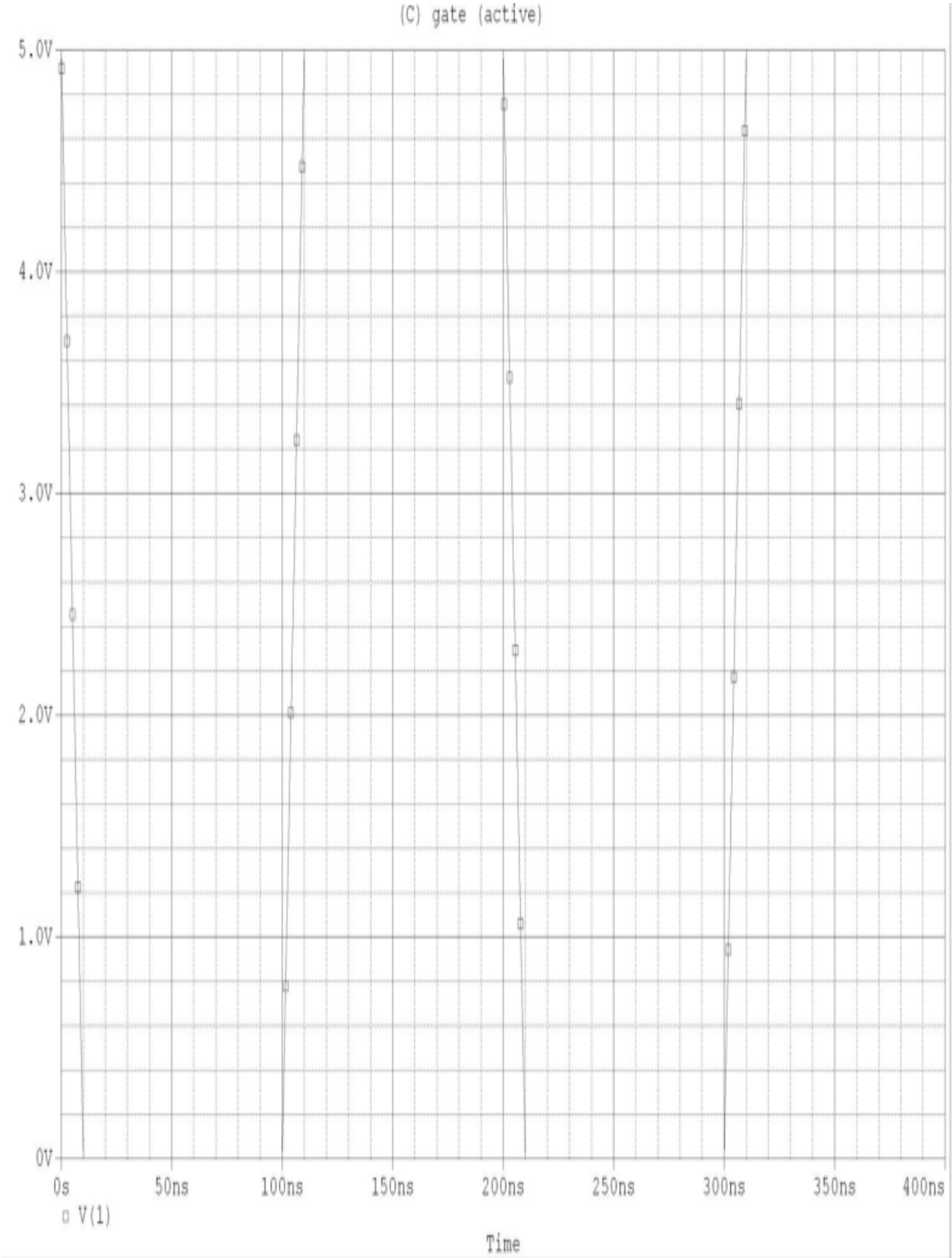
Defining the term R(3,5) as the resistance between switch nodes 3 and 5, you can interpret the model as follows. If V(1,0) ≥ 2.6V then R(3,5) = 10 Ω. Similarly, if V(1,0) ≤ 2.4V then R(3,5) = 1 MΩ. Between the ON and OFF voltages, 2.4V ≤ V(1,0) ≤ 2.6V, the resistance varies continuously between RON and ROFF. (Using RON, ROFF, you could define a switch that turns OFF when the input goes HI.)

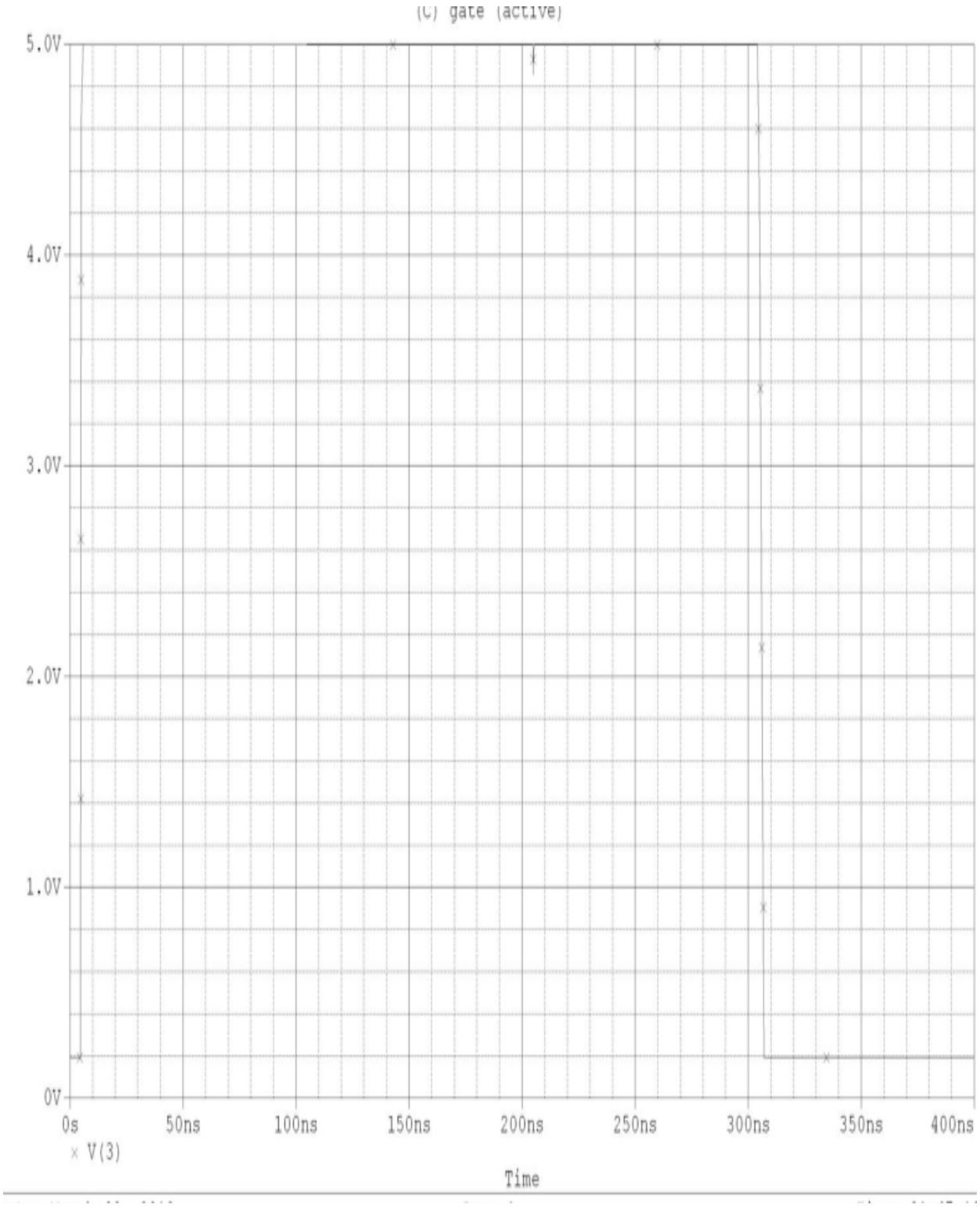
SPICE FILE

```
LOGIC_SW.CIR - BASIC LOGIC GATES USING SWITCHES
*
VCC     10      0       5V
*
* INPUT A AND B, COUNT IN BINARY 0 - 3
VA      1       0       PULSE(5V 0V 0NS 10NS 10NS 90NS 200NS)
VB      2       0       PULSE(5V 0V 0NS 10NS 10NS 190NS 400NS)
*
XNAND1  1 2 3 10        NAND
*
*
* LOGIC GATE SUBCIRCUITS ****************************************
*
.SUBCKT NAND 1 2 3 4
* TERMINALS A B OUT VCC
RL      3       4       500
S1      3 5     1 0     SW
S2      5 0     2 0     SW
.ENDS
*
.SUBCKT AND 1 2 3 4
* TERMINALS A B OUT VCC
S1      4 5     1 0     SW
S2      5 3     2 0     SW
RL      3       0       500
.ENDS
*
.SUBCKT NOR 1 2 3 4
* TERMINALS A B OUT VCC
RL      3       4       500
S1      3 0     1 0     SW
S2      3 0     2 0     SW
.ENDS
*
.SUBCKT NOT 1 3 4
* TERMINALS A OUT VCC
RL      3       4       500
```

```
S1      3 0     1 0     SW
.ENDS
*
*
.MODEL  SW      VSWITCH(VON=2.6 VOFF=2.4 RON=10 ROFF=1MEG)
*
* ANALYSIS ************************************************
.TRAN   5NS     400NS
*
* VIEW RESULTS
.PRINT  TRAN    V(1) V(2) V(3)
.PROBE
.END
```

RESULT:


(C) gate (active)
5.0V
4.0V
3.0V
2.0V
1.0V
0V
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
V(1)
Time


(C) gate (active)
5.0V
4.0V
3.0V
2.0V
1.0V
0V
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
V(3)
Time


(C) gate (active)
5.0V
4.0V
3.0V
2.0V
1.0V
0V
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
V(3)
Time