BAPATLA ENGINEERING COLLEGE

BAPATLA

Electronic Devices

(EE-252) Lab Manual

Prepared by

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ECE DEPARTMENT

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LIST OF EXPERIMENTS

1. Characteristics of PN junction and Zener diodes
2. Characteristics of Common Emitter Configuration
3. Design and verification of self bias circuit
4. Characteristics of JFET
5. Characteristics of UJT
6. Characteristics of Silicon Controlled Rectifier
7. Realization of Gates using Discrete Components and Universal Building block (NAND only)
8. Design of Combinational Logic Circuits.
9. Design of Code Converters, of Multiplexers & Decoders.
10. Verification of Truth Table of Flip-Flops using Gates.
11. Design of shift register, Ring & Johnson Counters using Flip-Flops.
12. Design Asynchronous Counter, Mod Counter, Up Counter, Down Counter and Up/Down Counter
13. Design Synchronous Counter, Mod Counter, Up Counter, Down Counter and Up/Down Counter
14. Design of sequence generator using shift registers and multiplexers.

STUDENTS GUIDELINES

There are 3 hours allocated to a laboratory session in Digital Electronics. It is a necessary part of the course at which attendance is compulsory.

Here are some guidelines to help you perform the experiments and to submit the reports:

1. Read all instructions carefully and carry them all out.
2. Ask a demonstrator if you are unsure of anything.
3. Record actual results (comment on them if they are unexpected!)
4. Write up full and suitable conclusions for each experiment.
5. If you have any doubt about the safety of any procedure, contact the demonstrator beforehand.
6. **THINK** about what you are doing!

The Breadboard

The breadboard consists of two terminal strips and two bus strips (often broken in the centre). Each bus strip has two rows of contacts. Each of the two rows of contacts are a node. That is, each contact along a row on a bus strip is connected together (inside the breadboard). Bus strips are used primarily for power supply connections, but are also used for any node requiring a large number of connections. Each terminal strip has 60 rows and 5 columns of contacts on each side of the centre gap. Each row of 5 contacts is a node.

You will build your circuits on the terminal strips by inserting the leads of circuit components into the contact receptacles and making connections with 22-26 gauge wire. There are wire cutter/strippers and a spool of wire in the lab. It is a good practice to wire +5V and 0V power supply connections to separate bus strips.

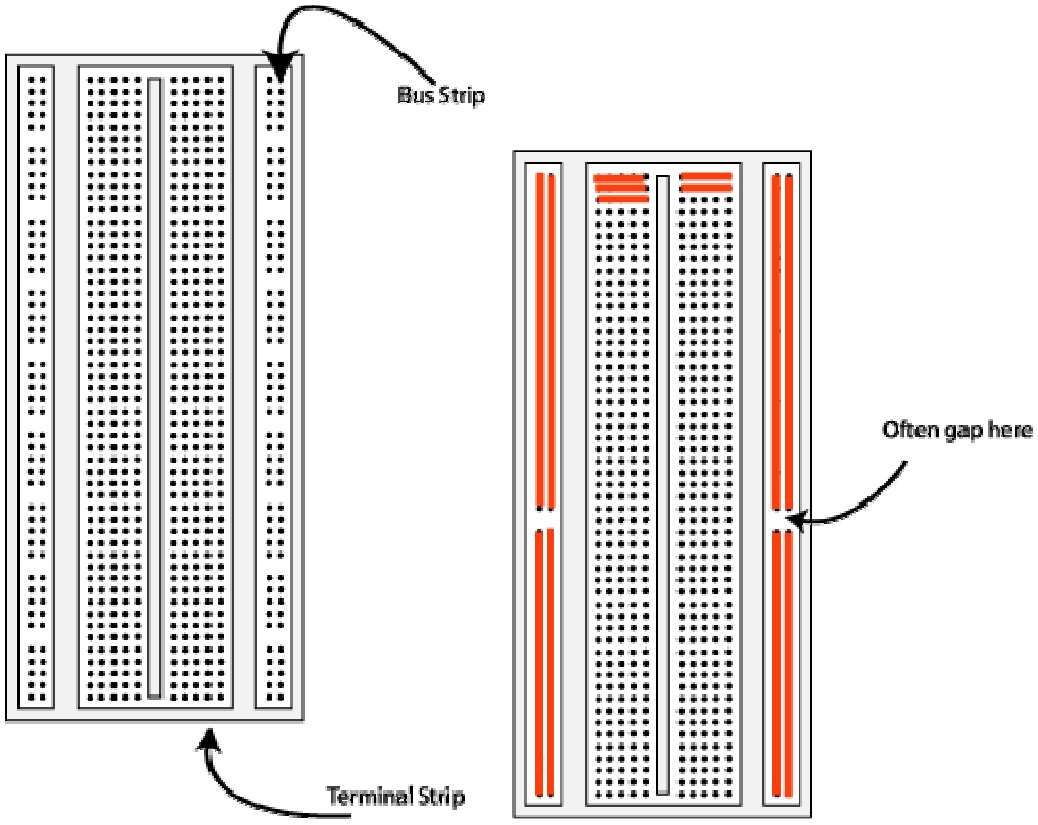


Fig 1. The breadboard. The lines indicate connected holes.

The 5V supply **MUST NOT BE EXCEEDED** since this will damage the ICs (Integrated circuits) used during the experiments. Incorrect connection of power to the ICs could result in them exploding or becoming very hot - with the **possible serious injury occurring to the people working on the experiment! Ensure that the power supply polarity and all components and connections are correct before switching on power .**

Building the Circuit:

Throughout these experiments we will use TTL chips to build circuits. The steps for wiring a circuit should be completed in the order described below:

1. Turn the power (Trainer Kit) off before you build anything!
2. Make sure the power is off before you build anything!

3. Connect the +5V and ground (GND) leads of the power supply to the power and ground bus strips on your breadboard.
4. Plug the chips you will be using into the breadboard. Point all the chips in the same direction with pin 1 at the upper-left corner. (Pin 1 is often identified by a dot or a notch next to it on the chip package)
5. Connect +5V and GND pins of each chip to the power and ground bus strips on the breadboard.
6. Select a connection on your schematic and place a piece of hook-up wire between corresponding pins of the chips on your breadboard. It is better to make the short connections before the longer ones. Mark each connection on your schematic as you go, so as not to try to make the same connection again at a later stage.
7. Get one of your group members to check the connections, **before you turn the power on**.
8. If an error is made and is not spotted before you turn the power on. Turn the power off immediately before you begin to rewire the circuit.
9. At the end of the laboratory session, collect you hook-up wires, chips and all equipment and return them to the demonstrator.
10. Tidy the area that you were working in and leave it in the same condition as it was before you started.

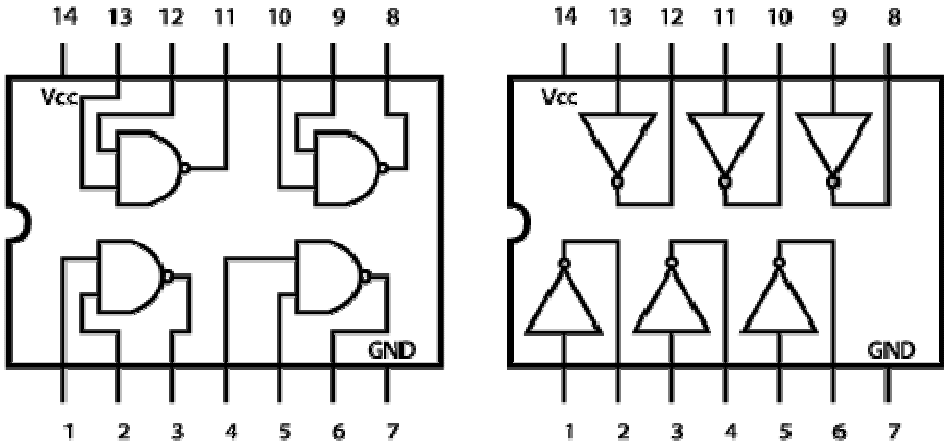
Common Causes of Problems:

1. Not connecting the ground and/or power pins for all chips.
2. Not turning on the power supply before checking the operation of the circuit.
3. Leaving out wires.
4. Plugging wires into the wrong holes.
5. Driving a single gate input with the outputs of two or more gates
6. Modifying the circuit with the power on.

In all experiments, you will be expected to obtain all instruments, leads, components at the start of the experiment and return them to their proper place after you have finished the experiment. Please inform the demonstrator or technician if you locate faulty equipment. If you damage a chip, inform a demonstrator, don't put it back in the box of chips for somebody else to use.

Example Implementation of a Logic Circuit:

Build a circuit to implement the Boolean function F = /(/A./B), please note that the notation **/A** refers to $\overline{A}$. You should use that notation during the write-up of your laboratory experiments.



Quad 2 Input 7400 Hex 7404 Inverter

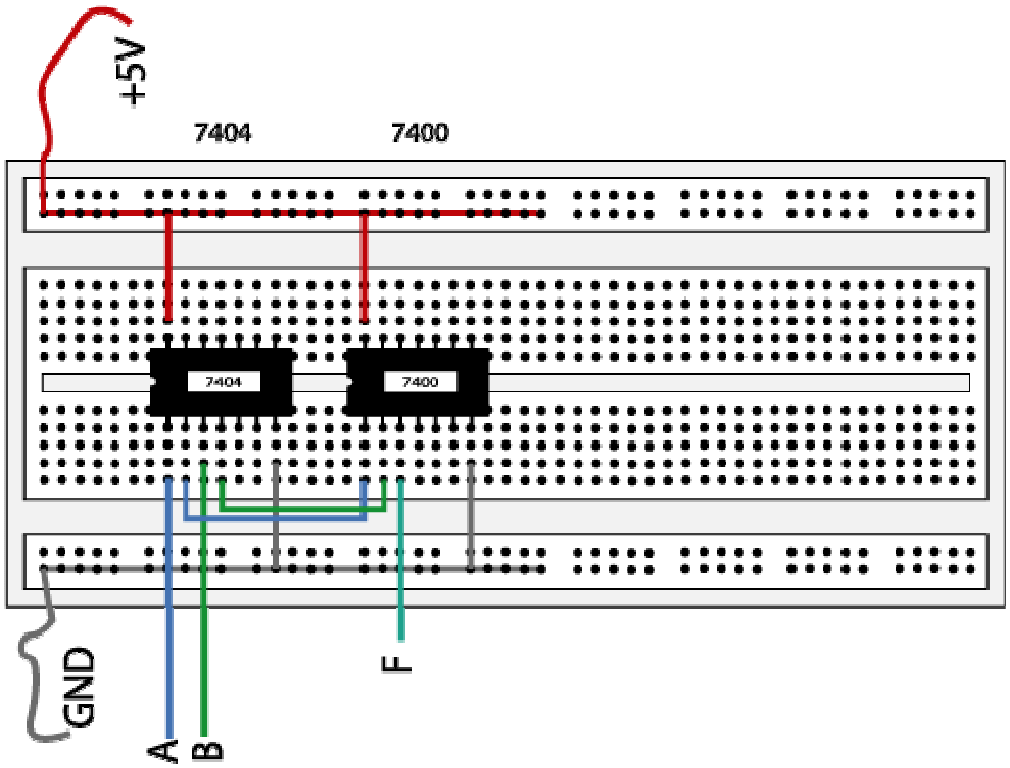


Fig 2. The complete designed and connected circuit

Sometimes the chip manufacturer may denote the first pin by a small indented circle above the first pin of the chip. Place your chips in the same direction, to save confusion at a later stage. Remember that you must connect power to the chips to get them to work.**Useful IC Pin details** **IC NUMBER**	**Description of IC**
7400	Quad 2 input NAND GATE
7401	Quad 2input NAND Gate (open collector)
7402	Quad 2 input NOR Gate
7403	Quad 2 input NOR Gates (open collector)
7404	Hex Inverts

7421	Dual 4 input AND Gates
7430	8 input NAND Gate
7432	Quad 2 input OR Gates
7486	Quad 2 input EX-OR Gate
74107	Dual j-k Flip Flop
74109	Dual j-k Flip Flop
74174	Hex D Flip Flop
74173	Quad D Flip Flop
7473	Dual j-k Flip Flop
7474	Dual D Flip Flop
7475	Quad Bi-stable latch
7476	Dual j-k Flip Flop

1.(a) P-N Junction Diode Characteristics

AIM:- To find out the V-I characteristics of silicon and germanium diodes in Forward and Reverse bias configurations.

APPARATUS:-

P-N Diodes DR25, BY126

Regulated Power supply (0-30v)

Resistor 1KΩ

Ammeters (0-200 mA, 0-200μA), Voltmeter (0-20 V)

Bread board and Connecting wires

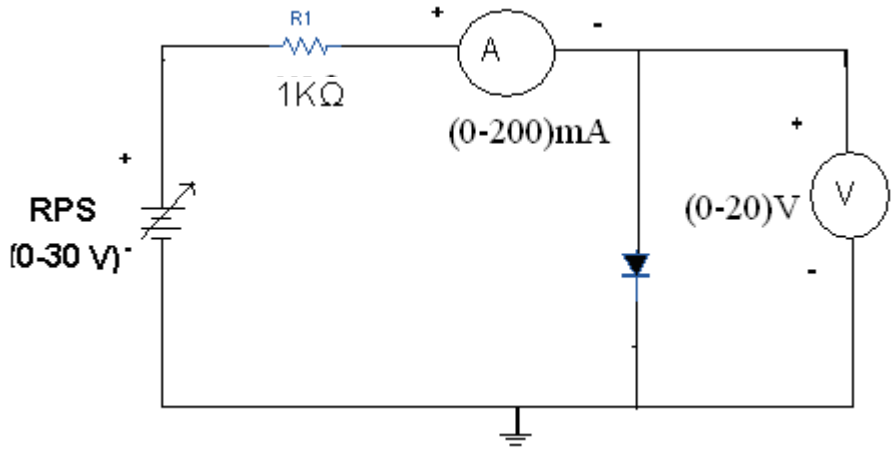
THEORY:-

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage.

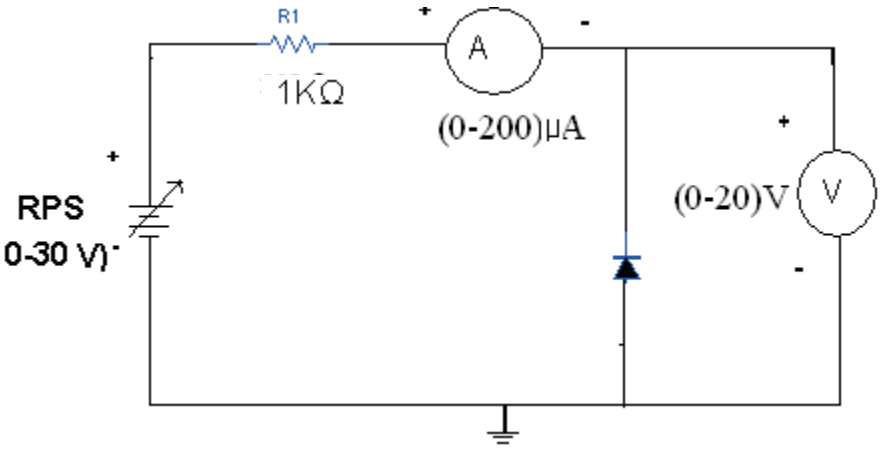
When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected to the –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current is due to minority charge carriers.

CIRCUIT DIAGRAM:-

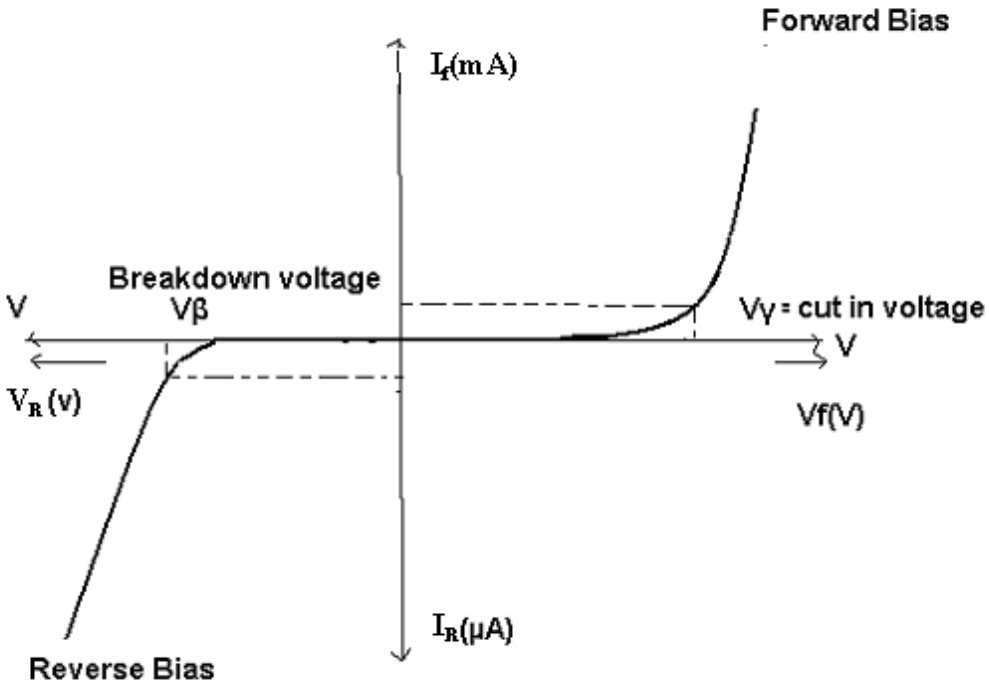
FORWARD BIAS:-



REVERSE BIAS:-



MODEL WAVEFORM:-



PROCEDURE:-

FORWARD BIAS:-

1. Connections are made as per the circuit diagram.

2. For forward bias, the RPS +ve is connected to the anode of the silicon diode and RPS –ve is connected to the cathode of the diode.

3. Switch on the power supply and increases the input voltage (supply voltage) in steps.

4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.

5. The readings of voltage and current are tabulated and a graph is plotted between voltage and current.

6. Repeat the above procedure for Germanium diode also and tabulate the results.

OBSERVATION:-

S.NO	APPLIED VOLTAGE (V)	VOLTAGE ACROSS DIODE (V)	DIODE CURRENT (mA)

PROCEDURE:-

REVERSE BIAS:-

1. Connections are made as per the circuit diagram

2. For reverse bias, the RPS +ve is connected to the cathode of the silicon diode and RPS –ve is connected to the anode of the diode.

3. Switch on the power supply and increase the input voltage (supply voltage) in steps.

4. Note down the corresponding current flowing through the diode voltage across the diode for each and every step of the input voltage.

5. The readings of voltage and current are tabulated and graph is plotted between voltage and current.

7. Repeat the above procedure for the given Germanium diode also and tabulate the results obtained.

OBSEVATION:-

S.NO	APPLIED VOLTAGE (V)	VOLTAGE ACROSS DIODE (V)	DIODE CURRENT (μA)

PRECAUTIONS:-

1. All the connections should be correct.

2. Parallax error should be avoided while taking the readings from the Analog meters.

VIVA QESTIONS:-

1. Define depletion region of a diode?

2. What is meant by transition & space charge capacitance of a diode?

3. Is the V-I relationship of a diode Linear or Exponential?

4. Define cut-in voltage of a diode and specify the values for Si and Ge diodes?

5. What are the applications of a p-n diode?

6. Draw the ideal characteristics of P-N junction diode?

7. What is the diode equation?

8. What is PIV?

9. What is the break down voltage?

10. What is the effect of temperature on PN junction diodes?

1(b). ZENER DIODE CHARACTERISTICS

AIM: - a) To observe and draw the static characteristics of a zener diode

b) To find the voltage regulation of a given zener diode

APPARATUS*: -* Zener diode (IZ5.1 or IZ9.1)

Regulated Power Supply (0-30v).

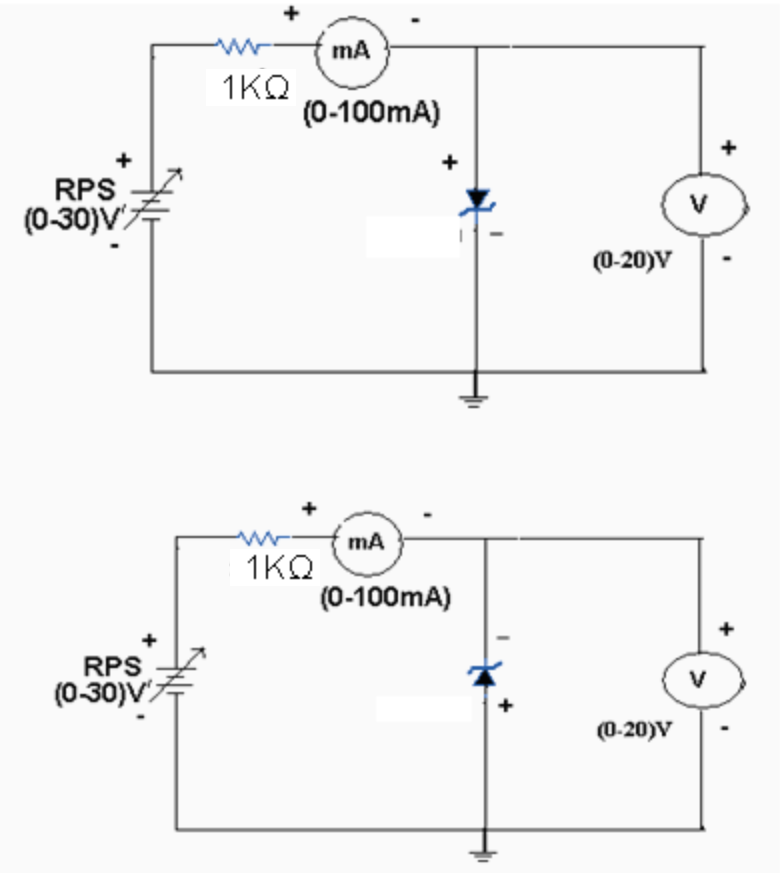
Voltmeter (0-20v) Ammeter (0-100mA)

Resistors (1Kohm)

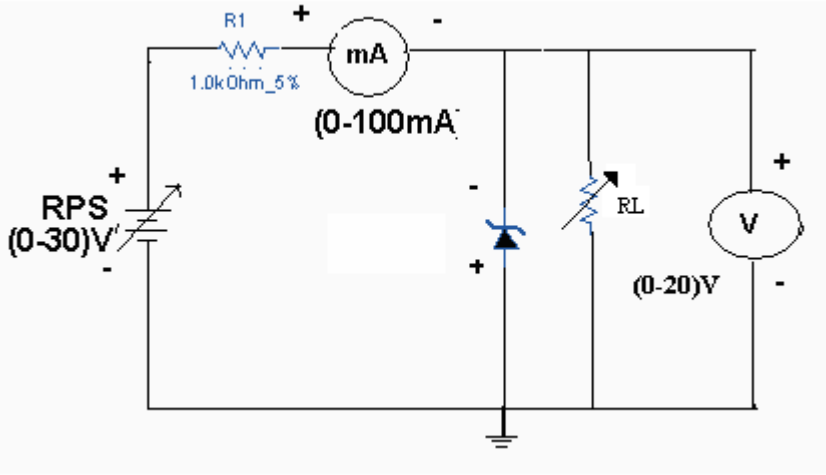
Bread Board and Connecting wires

CIRCUIT DIAGRAM:-

STATIC CHARACTERISTICS:-



REGULATION CHARACTERISTICS:-



Theory:-

A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device

To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals what ever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

PROCEDURE:-

Static characteristics:-

1. Connections are made as per the circuit diagram.

2. The Regulated power supply voltage is increased in steps.

3. The zener current (Iz), and the zener voltage (Vz.) are observed and then noted in the tabular form.

4. A graph is plotted between zener current (Iz) and zener voltage (Vz).

5. Do the above steps for forward as well as reverse bias connections as shown in the circuit diagrams.

Regulation characteristics:-

1. Connections are made as per the circuit diagram

2. The load resistance is fixed to known value and the zener voltage (V_z), and Zener current (I_z), are measured.

3. The load resistence is varied in steps and the corresponding values are noted down for each load resistance value.

4. All the readings are tabulated.

OBSERVATIONS:-

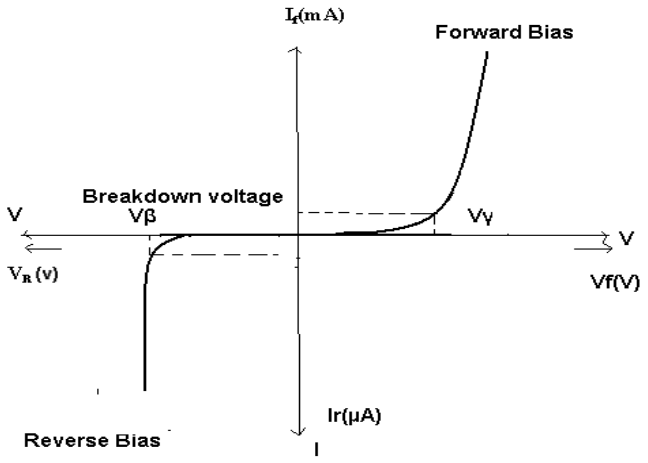
Static characteristics:-

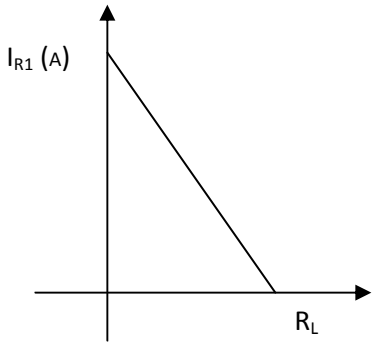
S.NO	ZENER VOLTAGE(V_Z)	ZENER CURRENT(I_Z)

Regulation characteristics:-

S.N0	V_Z(VOLTS)	I_{R1} (amperes)	R_L (Ω)

MODEL WAVEFORMS:-





PRECAUTIONS:-

1. The terminals of the zener diode should be properly identified.
2. Should be ensured that the applied voltages & currents do not exceed the diode ratings.

VIVAQUESTIONS:-

1. What type of temperature Coefficient does the zener diode have?
2. If the impurity concentration is increased, how the depletion width effected?
3. Does the dynamic impendence of a zener diode vary?
4. Explain briefly about avalanche and zener breakdowns?
5. Draw the zener equivalent circuit?
6. Differentiate between line regulation & load regulation?
7. In which region zener diode can be used as a regulator?
8. How the breakdown voltage of a particular diode can be controlled?
9. What type of temperature coefficient does the Avalanche breakdown has?

2. TRANSISTOR CE CHARACTERSTICS

AIM: To draw the input and output characteristics of transistor connected in CE configuration

APPARATUS:

Transistor (SL100 or BC107)

R.P.S (O-30V) 2Nos

Voltmeters (0-20V) 2Nos

Ammeters (0-200mA)

Resistors 100Kohm, 100ohm

Bread board and connecting wires

THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and out put is taken across the collector and emitter terminals.

Therefore the emitter terminal is common to both input and output.

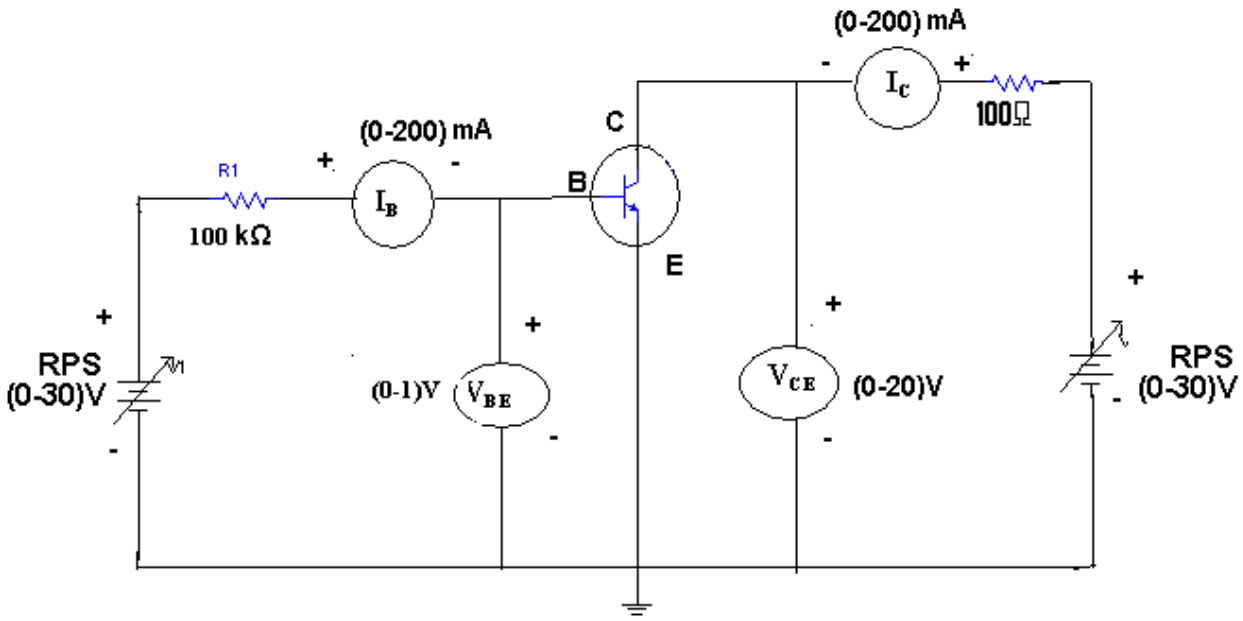
The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE} . Therefore input resistance of CE circuit is higher than that of CB circuit.

ximately equal to $I_{B.}$

The current amplification factor of CE configuration is given by

$$B = \Delta I_C / \Delta I_B$$

CIRCUIT DIAGRAM:



PROCEDURE:

INPUT CHARECTERSTICS:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 1V and for different values of V_{BE} . Note down the values of I_C
3. Repeat the above step by keeping V_{CE} at 2V and 4V.
4. Tabulate all the readings.
5. plot the graph between V_{BE} and I_B for constant V_{CE}

OUTPUT CHARACTERSTICS:

1. Connect the circuit as per the circuit diagram
2. for plotting the output characteristics the input current I_B is kept constant at 10μA and for different values of V_{CE} note down the values of I_C
3. repeat the above step by keeping IB at 75 μA 100 μA
4. tabulate the all the readings
5. plot the graph between V_{CE} and I_C for constant I_B

OBSERVATIONS:

INPUT CHARACTERISTICS:

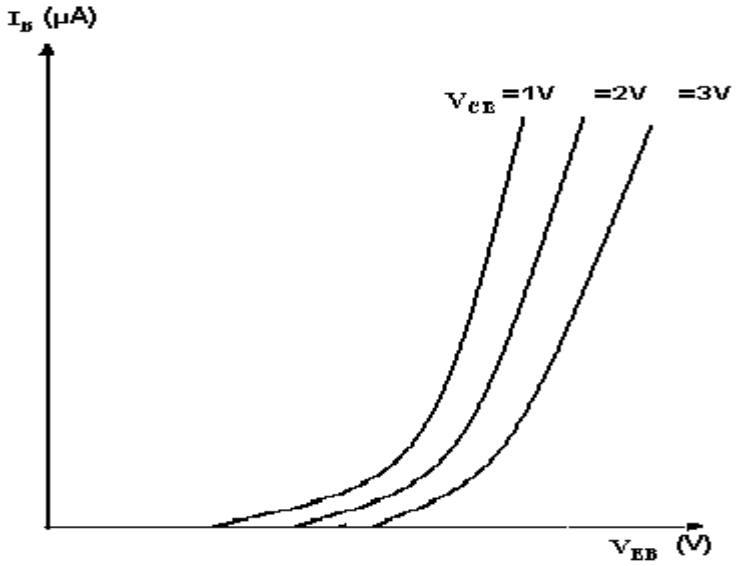
S.NO	V_{CE} = 1V		V_{CE} = 2V		V_{CE} = 4V	
	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)

OUT PUT CHAREACTARISTICS:

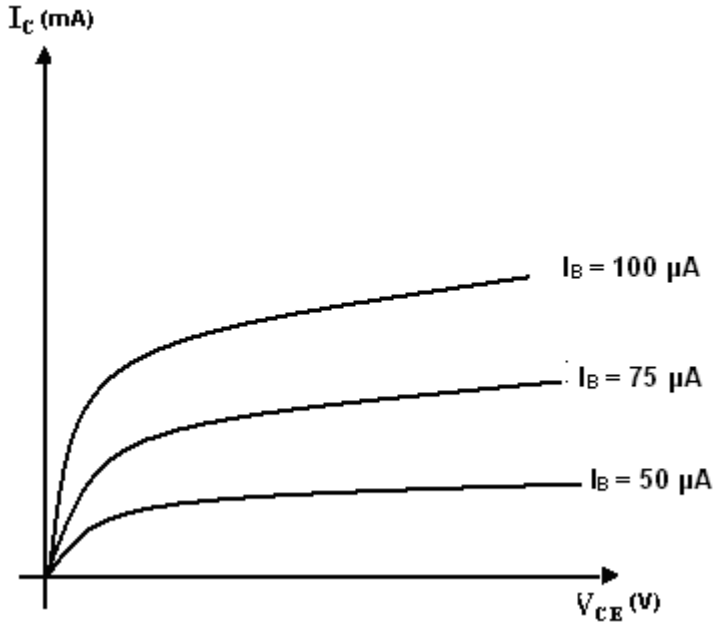
S.NO	I_B = 50 μA		I_B = 75 μA		I_B = 100 μA	
	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_CmA)	V_{CE}(V)	I_C(mA)

MODEL GRAPHS:

INPUT CHARACTERSTICS:



OUTPUT CHARECTERSTICS:



PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor

2. Meters should be connected properly according to their polarities

VIVA QUESTIONS:

1. What is the range of β for the transistor?
2. What are the input and output impedances of CE configuration?
3. Identify various regions in the output characteristics?
4. what is the relation between $\alpha and \beta$
5. Define current gain in CE configuration?
6. Why CE configuration is preferred for amplification?
7. What is the phase relation between input and output?
8. Draw diagram of CE configuration for PNP transistor?
9. What is the power gain of CE configuration?
10. What are the applications of CE configuration?

3 Design and Verification of Transistor Self bias circuit

AIM: To design a self bias circuit and observe stability by changing β of the transistor.

APPARATUS:

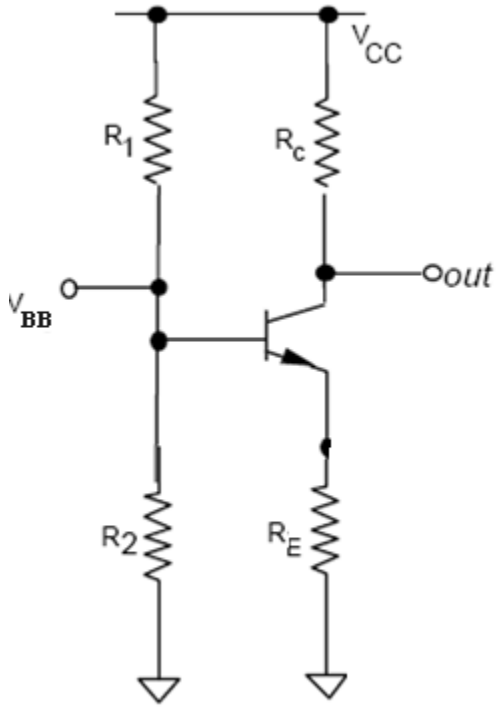
Transistors with different β values (SL100)

R.P.S (O-30V) 2Nos

Resistors (according to design values)

Bread board and connecting wires

CIRCUIT DIAGRAM:



Theory:

A self bias circuit stabilizes the bias point more appropriately than a fixed bias circuit. In this experiment CE configuration is used and a self bias circuit is designed and verified.

CALCULATIONS:

Given V_{CC}=10V, R_E=220 ohm I_C=4mA V_{CE}=6V V_{BE}=0.6V h_{fe}=229

$R_C=(V_{CC}-V_{CE})/I_C$

$I_B=I_C/\beta$

$R_B=\beta*R_E/10$

$V_{BB}=I_B*R_B+V_{BE}+(I_B+I_C)R_E$

$R_1=(V_{CC}/V_{BB})*R_B$

$R_2=R_B/(1-V_{BB}/V_{CC})$

PROCEDURE:

1. Assemble the circuit on a bread board with designed values of resistors and transistor.
2. Apply Vcc and measure VCE, VBE and VEE and record the readings in table I.
3. Without changing the values of biasing resistors, change the transistor with other β values and repeat the above steps and record the readings in the table.

OBSERVATIONS:

β value	V_{CE}	V_{BE}	V_{EE}	$I_C=(V_{CC}-V_{CE})/R_C$	$I_E=V_{EE}/R_E$

PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor
2. Connections must be tight.

VIVA QUESTIONS:

1. What are the advantages of self bias?
2. What are the various other configurations available for bias?

4. Characteristics of JFET

AIM: 1. To obtain the drain and transfer characteristics of the given JFET transistor.

2. To calculate r_d, g_m and μ from the curves obtained.

APPARATUS:

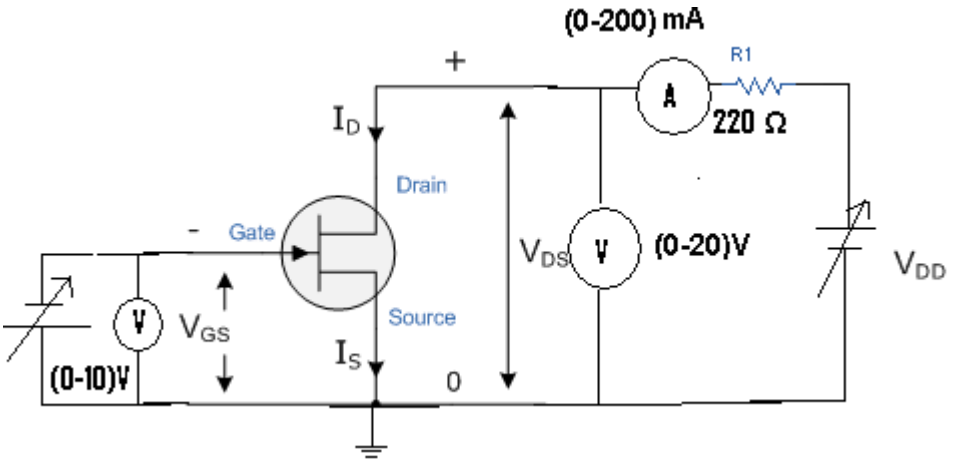
JFET transistor BFW10

R.P.S (O-30V) 2Nos

Resistors 220 ohm

Bread board and connecting wires

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Keeping V_{GS} as 0V, vary V_{DS} in steps of 0.1V from 0 to 1 V and in steps of 2V from 1 to 15V.
3. Note down the drain current Id for each step.
4. Now set V_{GS} to -1V, -2V and -3V and repeat the above steps for each V_{GS} value, record the readings in the table.

5. Keep V_{DS} at 4V and vary V_{GS} in steps of -5V till the drain current I_d is 0. Note I_d value for each value of V_{GS}.
6. With V_{DS} at 8V repeat the above step and record the readings in the table.
7. Plot the drain and transfer characteristics from tabulated readings.

OBSERVATIONS:

Drain Characteristics:

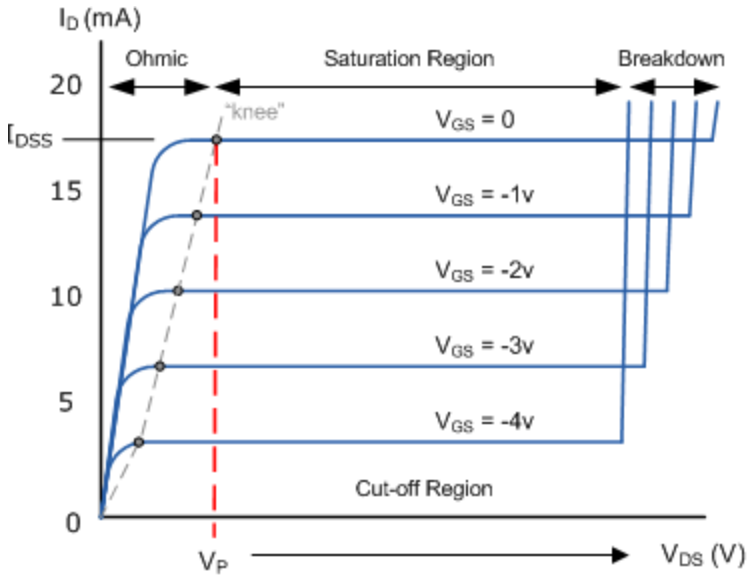
V_{DS}	I_D (V_{GS}=0V)	I_D (V_{GS}=-1V)	I_D (V_{GS}=-2V)

Transfer Characteristics:

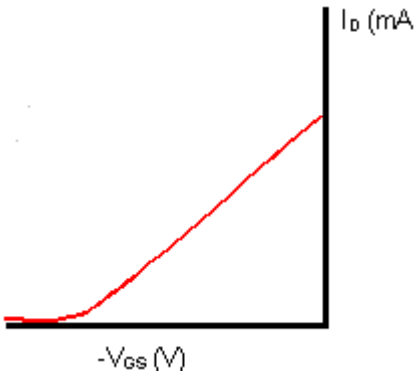
V_{GS}	I_D (V_{DS}=4V)	I_D (V_{DS}=8V)

MODEL GRAPHS:

Drain Characteristics:



Transfer Characteristics:



PRECAUTIONS:

1. The supply voltage should not exceed the rating of the FET.

2. Connections must be tight.

VIVA QUESTIONS:

1. What are the advantages of FET over transistor?
2. Is FET a current controlled device? Explain?
3. What is the operation of a N-channel JFET?
4. Can you compare JFET and a MOSFET?

5. UJT CHARACTERISTICS

AIM: To observe the characteristics of UJT and to calculate the Intrinsic Stand-Off Ratio (η).

APPARATUS:

Regulated Power Supply (0-30V, 1A) - 2Nos

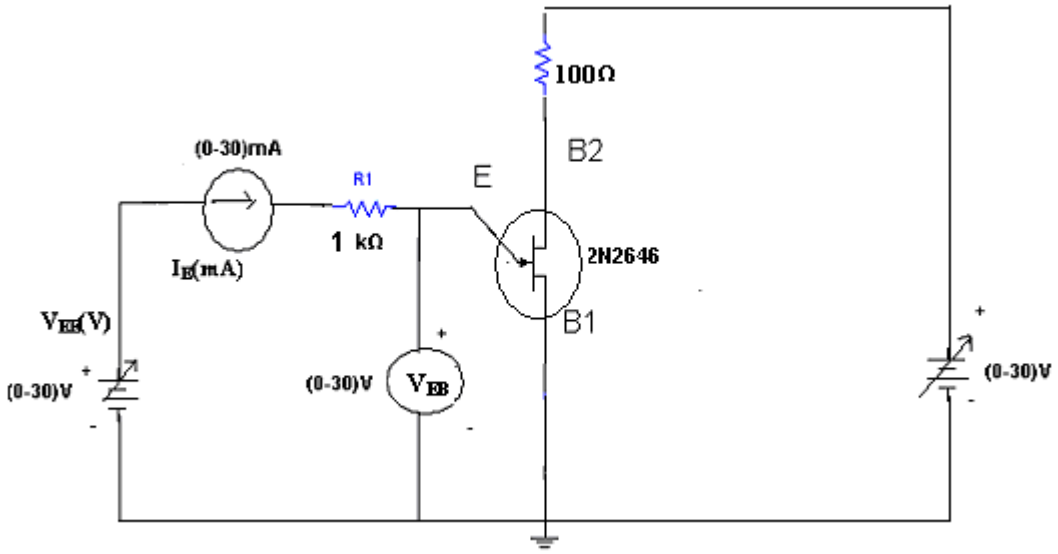
UJT 2N2646

Resistors 1kΩ, 100Ω

Multimeters - 2Nos

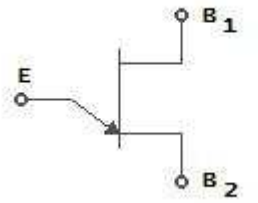
Breadboard and connecting Wires

CIRCUIT DIAGRAM



THEORY:

A Unijunction Transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT Unijunction Transistor (UJT) has three terminals an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance.The original unijunction transistor, or UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length. The 2N2646 is the most commonly used version of the UJT.



Circuit symbol

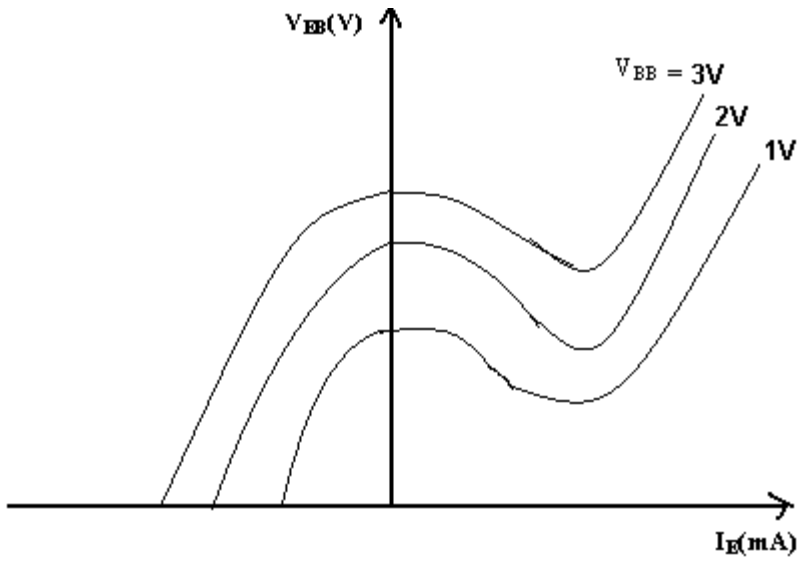
The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect

is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits.When the emitter voltage reaches V_p, the current startsto increase and the emitter voltage starts to decrease.This is represented by negative slope of the characteristics which is reffered to as the negative resistance region,beyond the valleypoint ,R_{B1} reaches minimum value and this region,V_{EB} propotional to I_E.

PROCEDURE:

1. Connection is made as per circuit diagram.
2. Output voltage is fixed at a constant level and by varying input voltage corresponding emitter current values are noted down.
3. This procedure is repeated for different values of output voltages.
4. All the readings are tabulated and Intrinsic Stand-Off ratio is calculated using $\eta = (V_p - V_D) / V_{BB}$
5. A graph is plotted between V_{EE} and I_E for different values of V_{BE}.

MODEL GRAPH:



OBSEVATIONS:

V_{BB}=1V		V_{BB}=2V		V_{BB}=3V	
V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)

CALCULATIONS:

$$V_P = \eta V_{BB} + V_D$$

$$\eta = (V_P - V_D) / V_{BB}$$

$$\eta = (\eta_1 + \eta_2 + \eta_3) / 3$$

VIVA QUESTIONS

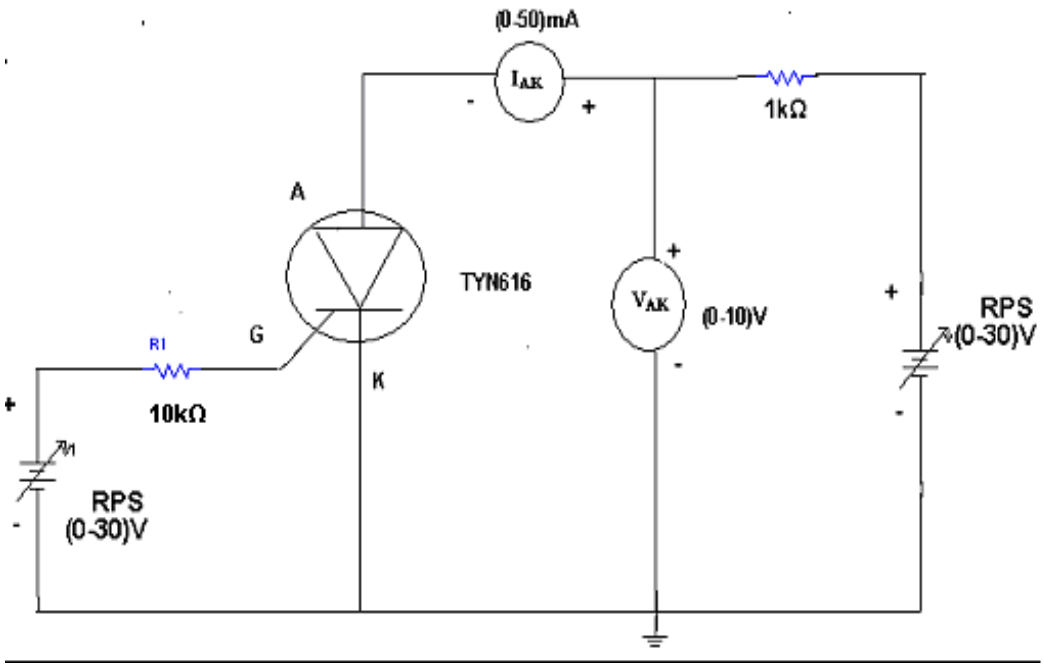
1. Wha is the symbol of UJT?
2. Draw the equivalent circuit of UJT?
3. What are the applications of UJT?
4. Formula for the intrinsic stand off ratio?
5. What does it indicates the direction of arrow in the UJT?
6. What is the difference between FET and UJT?
7. Is UJT is used an oscillator? Why?
8. What is the Resistance between B_1 and B_2 is called as?
9. What is its value of resistance between B_1 and $B_{2?}$
10. Draw the characteristics of UJT?

6. SILICON-CONTROLLED RECTIFIER (SCR) CHARACTERISTICS

AIM: To draw the V-I Characteristics of SCR.

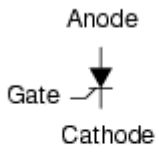
APPARATUS: SCR (TYN616)
Regulated Power Supply (0-30V)
Resistors 10kΩ, 1kΩ
Ammeter (0-50) µA
Voltmeter (0-10V)
Bread board and connecting wires.

CIRCUIT DIAGRAM:



THEORY:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists os 3 junctions J_1, J_2, J_3 the J_1 and J_3 operate in forward direction and J_2 operates in reverse direction and three terminals called anode A, cathode K , and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode.



Schematic symbol

When gate is open, no voltage is applied at the gate due to reverse bias of the junction J_2 no current flows through R_2 and hence SCR is at cutt off. When anode voltage is increased J_2 tends to breakdown.

When the gate positive,with respect to cathode J_3 junction is forward biased and J_2 is reverse biased .Electrons from N-type material move across junction J_3 towards gate while holes from P-type material moves across junction J_3 towards cathode. So gate current starts flowing ,anode current increaase is in extremely small current junction J_2 break down and SCR conducts heavily.

When gate is open thee breakover voltage is determined on the minimum forward voltage at which SCR conducts heavily.Now most of the supply voltage appears across the load resistance.The holfing current is the maximum anode current gate being open , when break over occurs.

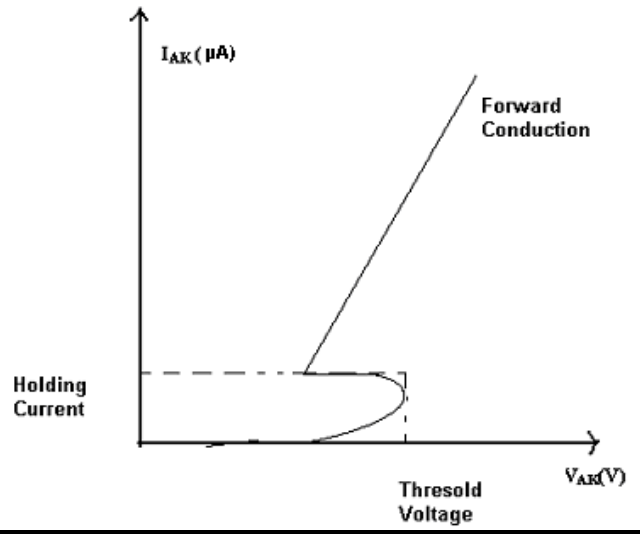
PROCEDURE:

1. Connections are made as per circuit diagram.
2. Keep the gate supply voltage at some constant value
3. Vary the anode to cathode supply voltage and note down the readings of voltmeter and ammeter.Keep the gate voltage at standard value.
4. A graph is drawn between V_{AK} and I_{AK} .

OBSERVATION

V_{AK}(V)	I_{AK} (µA)

MODEL WAVEFORM:



VIVA QUESTIONS

1. What the symbol of SCR?
2. IN which state SCR turns of conducting state to blocking state?
3. What are the applications of SCR?
4. What is holding current?
5. What are the important type's thyristors?
6. How many numbers of junctions are involved in SCR?
7. What is the function of gate in SCR?
8. When gate is open, what happens when anode voltage is increased?
9. What is the value of forward resistance offered by SCR?
10. What is the condition for making from conducting state to non conducting state?

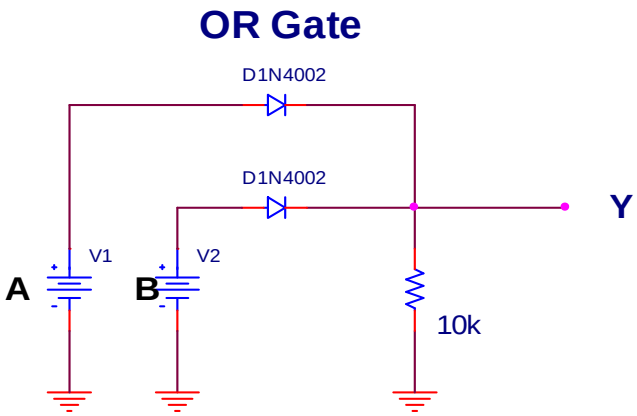
7(a).REALIZATION OF GATES USING DISCRETE COMPONENTS

Aim: To construct logic gates **OR, AND, NOT, NOR, NAND** gates using discrete components and verify their truth tables

Apparatus:

1. Electronic circuit designer
2. Resistors 10k,1k,220ohms
3. Transistors 2N2222(NPN)
4. Diodes 1N 4001
5. Connecting wires

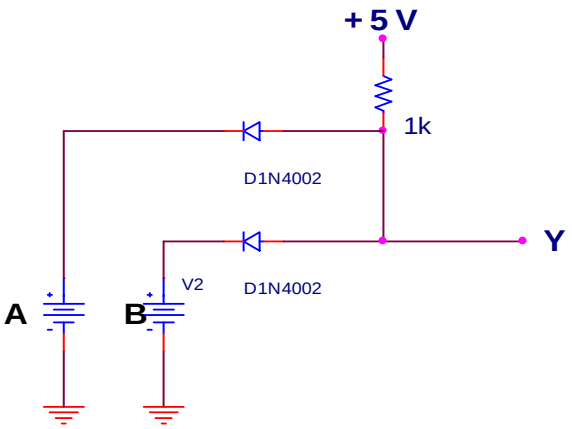
Circuit Diagrams:



TRUTH TABLE

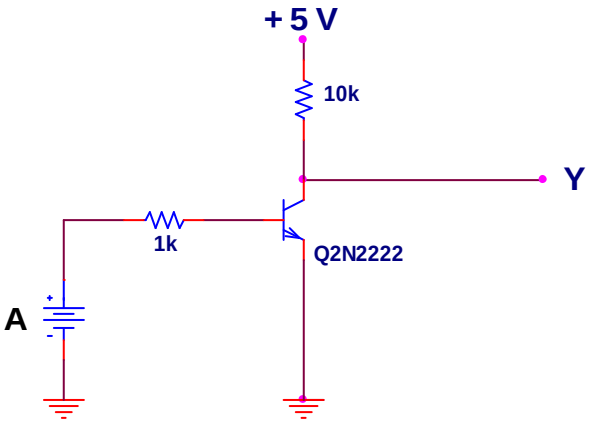
A	B	Y
0v	0v	0v
0v	5v	5v
5v	0v	5v
5v	5v	5v

AND Gate



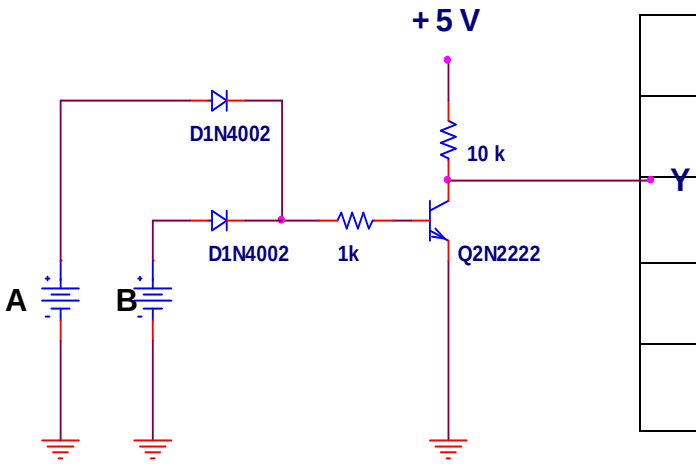
A	B	Y
0v	0v	0v
0v	5v	0v
5v	0v	0v
5v	5v	5v

NOT Gate



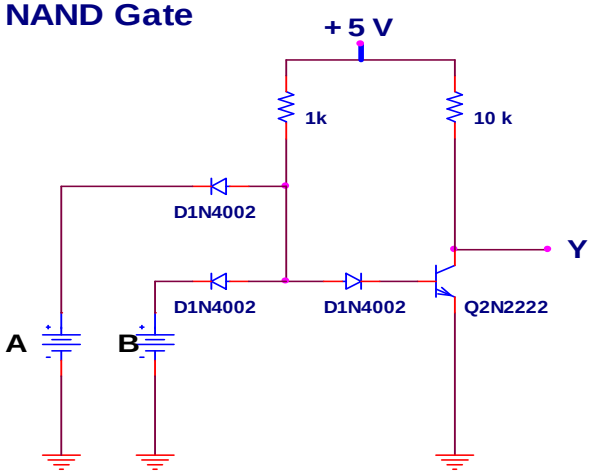
A	Y
0v	5v
5v	0v

NOR Gate



A	B	Y
0v	0v	5v
0v	5v	0v
5v	0v	0v
5v	5v	0v

NAND Gate



A	B	Y
0v	0v	5v
0v	5v	5v
5v	0v	5v
5v	5v	0v

Procedure:

1. Connections are made as per the circuit diagram

2. Switch on the power supply

3. Apply different combinations of inputs and observe the outputs; compare the outputs with the

truth tables.

Precautions:

All the connections should be made properly

Result: Different logic gates are constructed and their truth tables are verified.

Questions:

1. Explain the operation of each circuit.

7(b).REALIZATION OF GATES USING UNIVERSAL BUILDING BLOCKS (NAND ONLY)

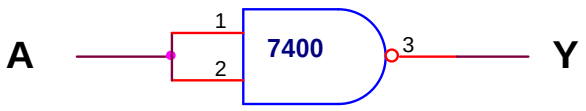
Aim: To construct logic gates NOT, AND, OR, EX-OR,EX-NOR of basic gates using NAND gate and verify their truth tables .

Apparatus:

1. IC's - 7400
2. Electronic Circuit Designer
3. Connecting patch chords.

Circuit Diagrams:

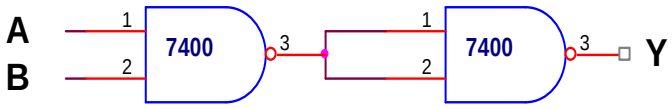
NOT Gate



TRUTH TABLE

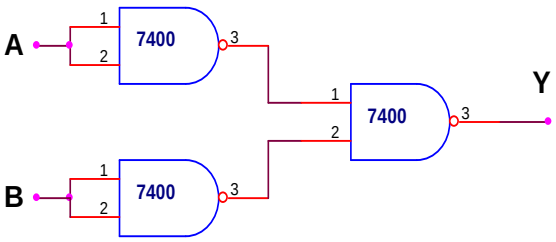
A	Y
0v	5v
5v	0v

AND Gate



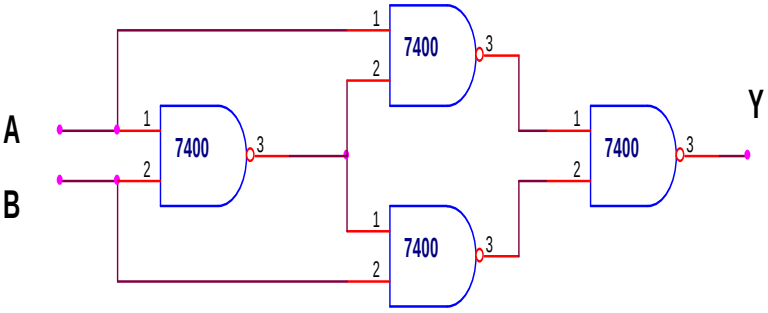
A	B	Y
0v	0v	0v
0v	5v	0v
5v	0v	0v
5v	5v	5v

OR Gate



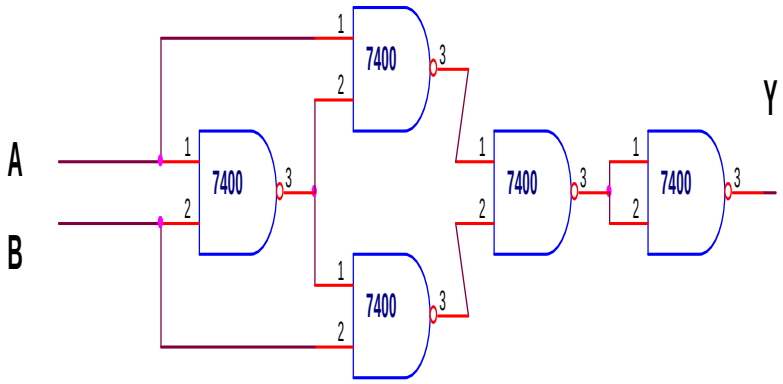
A	B	Y
0v	0v	0v
0v	5v	5v
5v	0v	5v
5v	5v	5v

EX-OR Gate



A	B	Y
0v	0v	0v
0v	5v	5v
5v	0v	5v
5v	5v	0v

EX-NOR Gate



A	B	Y
0v	0v	5v
0v	5v	0v
5v	0v	0v
5v	5v	5v

Procedure:

1. Connect the logic gates as shown in the diagrams.

2. Feed the logic signals 0 or 1 from the logic input switches in different combinations at the inputs A & B.

3. Monitor the output using logic output LED indicators.

4. Repeat steps 1 to 3 for NOT, AND, OR, EX – OR & EX-NOR operations.

and compare the outputs with the truth tables.

Precautions:1. All the connections should be made properly.

2. IC should not be reversed.

Result: Different logic gates are constructed using NAND gates and their truth tables are verified.

Questions:

1. Why NAND & NOR gates are called universal gates?

2. Realize the EX – OR gates using minimum number of NAND gates?

3. Give the truth table for EX-NOR (EX-OR+NOT) and realize using NAND gates.

4. Realize the given logic function using NAND gates?

$$f = ABC + ABC + ABC$$

8.DESIGN OF COMBINATIONAL LOGIC CIRCUITS

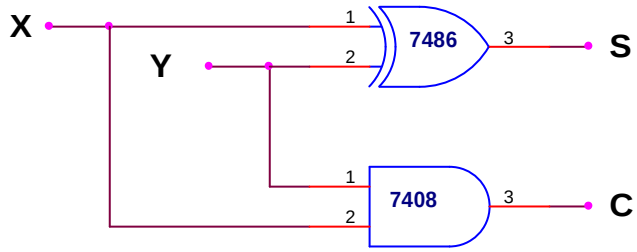
Aim: - To design and construct Half-adder, Full-adder, Half-subtractor, Full- subtractor

Apparatus: -

1. IC's - 7486, 7432, 7408, 7400
2. Electronic Circuit Designer
3. Connecting patch chords.

Circuit Diagram:-

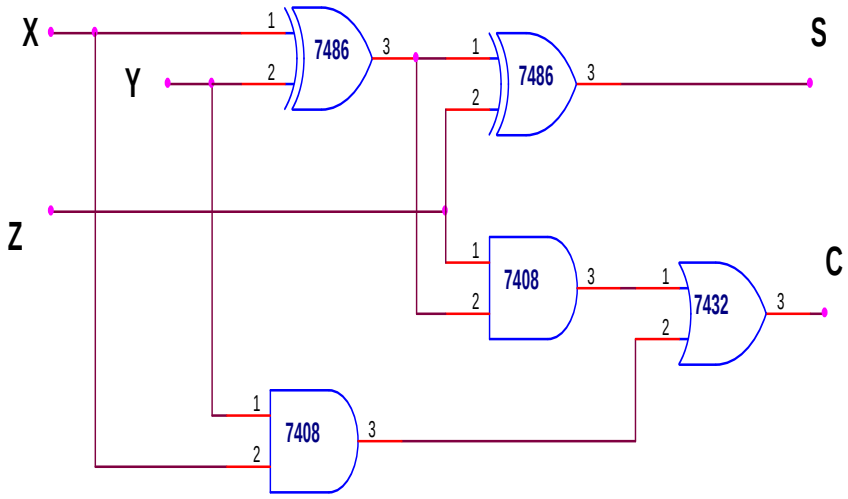
Half Adder:



TRUTH TABLE

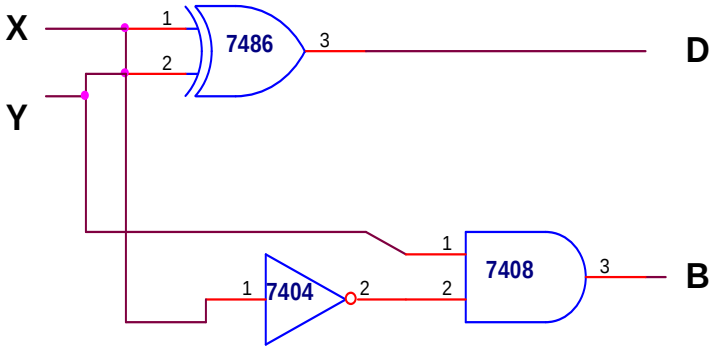
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder:



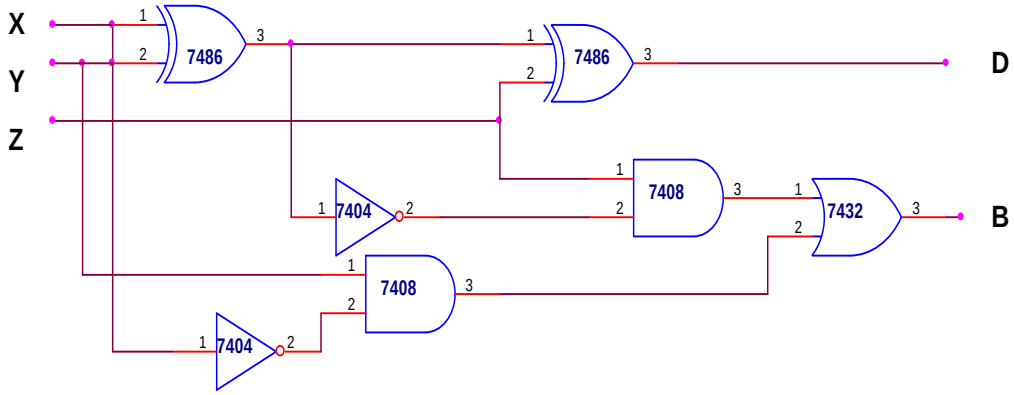
A	B	C_{N-1}	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Half Subtractor



A	B	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Full Subtractor



A	B	C_{N-1}	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Procedure: -1. Verify the gates.

2. Make the connections as per the circuit diagram.

3. Switch on V_{CC} and apply various combinations of input according to truth table.

4. Note down the output readings for half/full adder and half/full subtractor, Sum/difference and

the carry/borrow bit for different combinations of inputs verify their truth tables.

Precautions:

1. All the connections should be made properly.

2. IC should not be reversed.

Result: Combinational logic circuits like Half-adder, Full-adder, Half-subtractor, Full- sub tractor are constructed and truth tables are verified.

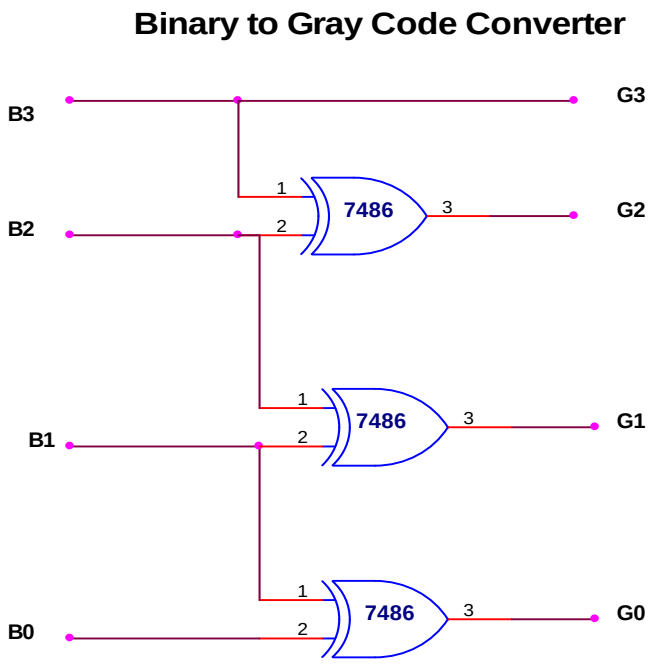
9(a).DESIGN OF CODE CONVERTORS (BINARY TO GRAY AND GRAY TO BINARYCONVERSION)

Aim: To design code converters and verify their truth tables

Apparatus:

1. IC - 7486
2. Electronic circuit designer
3. Connecting patch chords

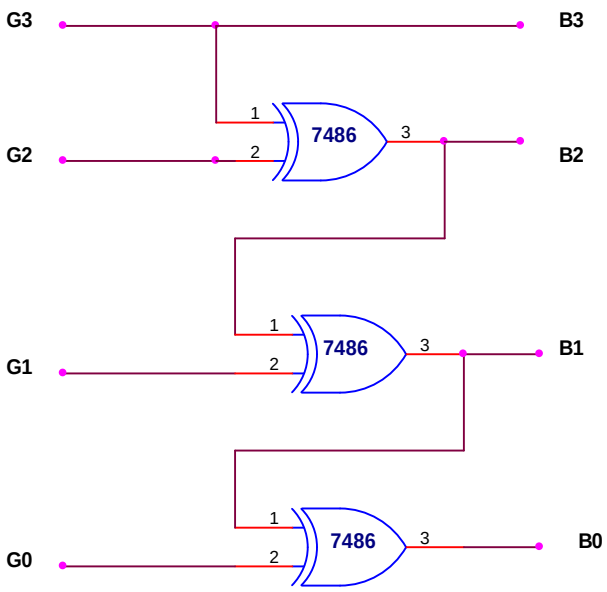
Circuit Diagrams:



Truth table

B3	B2	B1	BO	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Gray to Binary Code Converter



G3	G2	G1	GO	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

Procedure: -

1. The circuit connections are made as shown in fig.

2. Pin (14) is connected to +Vcc and Pin (7) to ground.

3 In the case of binary to gray conversion, the inputs B0, B1, B2 and B3 are given at

respective pins and outputs G0, G1, G2, G3 are taken for all the 16 combinations of the input.

4. In the case of gray to binary conversion, the inputs G0, G1, G2 and G3 are given at respective

Pins and outputs B0, B1, B2, and B3 are taken for all the 16 combinations of inputs.

5. The values of the outputs are tabulated.

Result: code converters are designed and their truth tables are verified.

Precautions: All the connections should be made properly.

Questions:1. Convert binary 100100 to gray code. **DESIGN OF**

9(b).MULTIPLEXERS/DECODERS

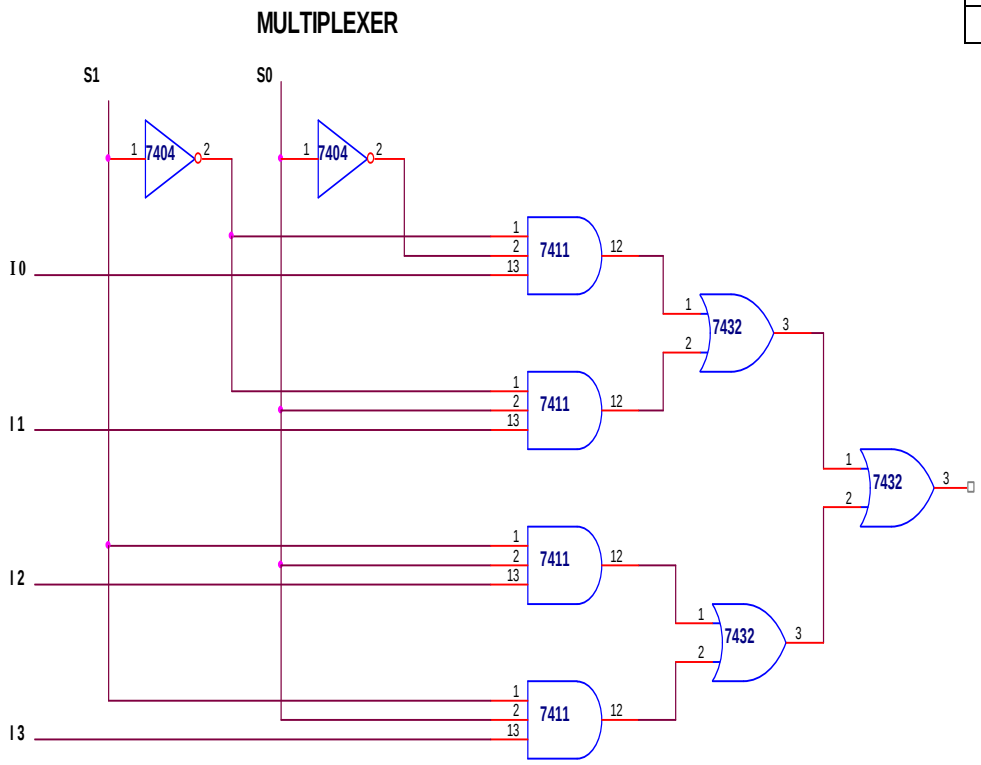
Aim: To design Multiplexer and Demultiplexer and verify their truth tables

Apparatus:

1. IC - 7404,7411,7432,7408
2. Electronic circuit designer
3. Connecting patch chords

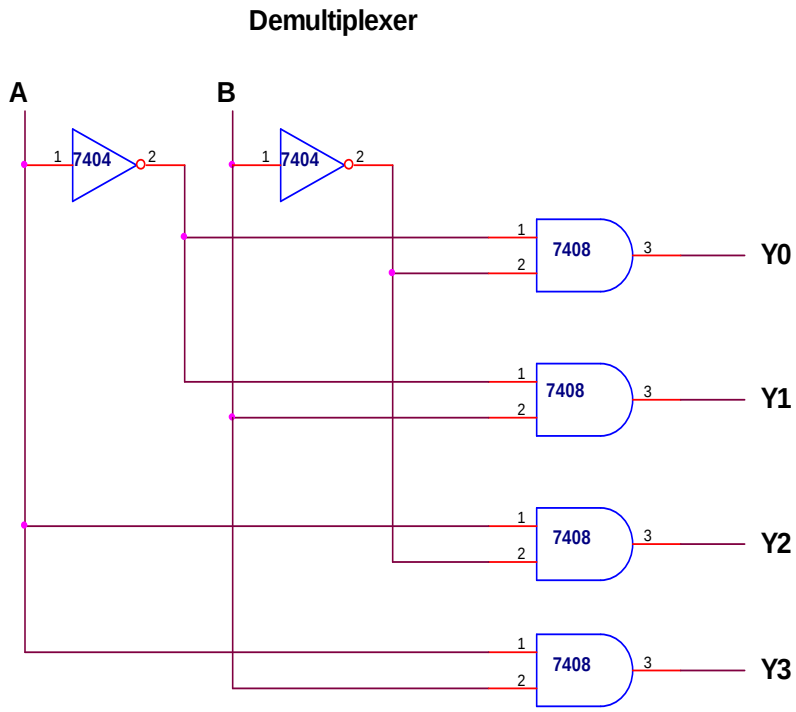
Circuit Diagrams:

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3



footer

A	B	Y3	Y2	Y1	Y0



0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Procedure:

1. Connections are made as per the circuit diagram

2. Switch on the power supply

3. Apply different combinations of inputs and observe the outputs; compare the outputs with the truth tables.

Precautions: All the connections should be made properly.

Result: Multiplexer and Demultiplexer are constructed and the truth tables are verified

Questions:

1. What is the difference between multiplexer and decoder

10.VERIFICATION OF TRUTH TABLES OF FLIPFLOPS USING GATES

Aim: - To design and construct basic flip-flops R-S ,J-K,J-K Master slave flip-flops using gates

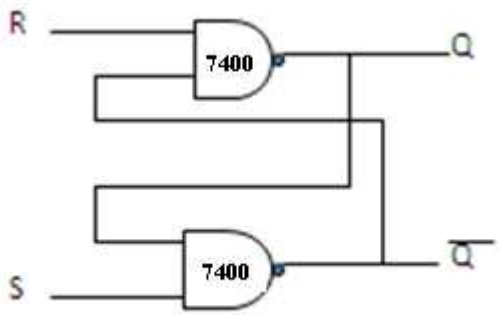
and verify their truth tables

Apparatus: -

1. IC's - 7404, 7402, 7400
2. Electronic circuit designer
3. Connecting patch chords

Circuit Diagrams:-

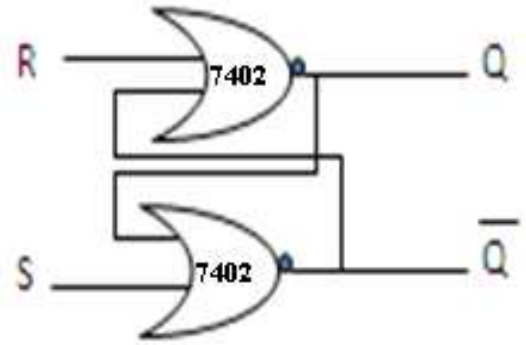
Basic flipflop using NAND gates



Truth Table

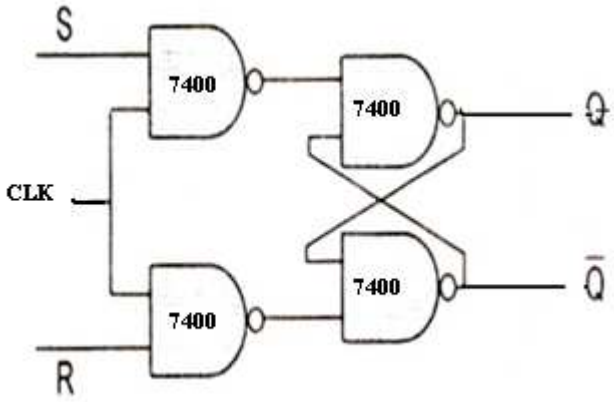
S	R	Q
0	0	Forbidden
0	1	1
1	0	0
1	1	No Change

Basic flipflop using NOR gates



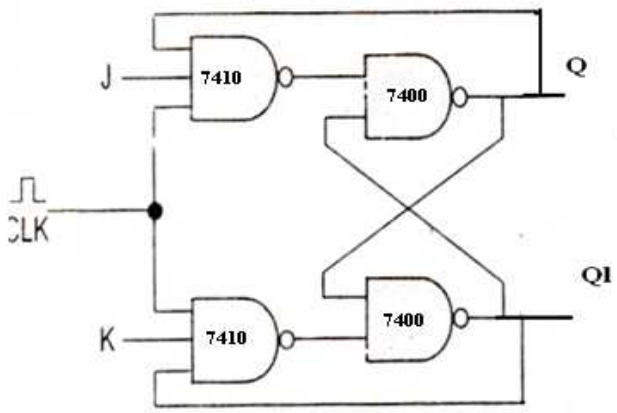
S	R	Q
0	0	No Change
0	1	0
1	0	1
1	1	Forbidden

R-S flip-flop using NAND gates



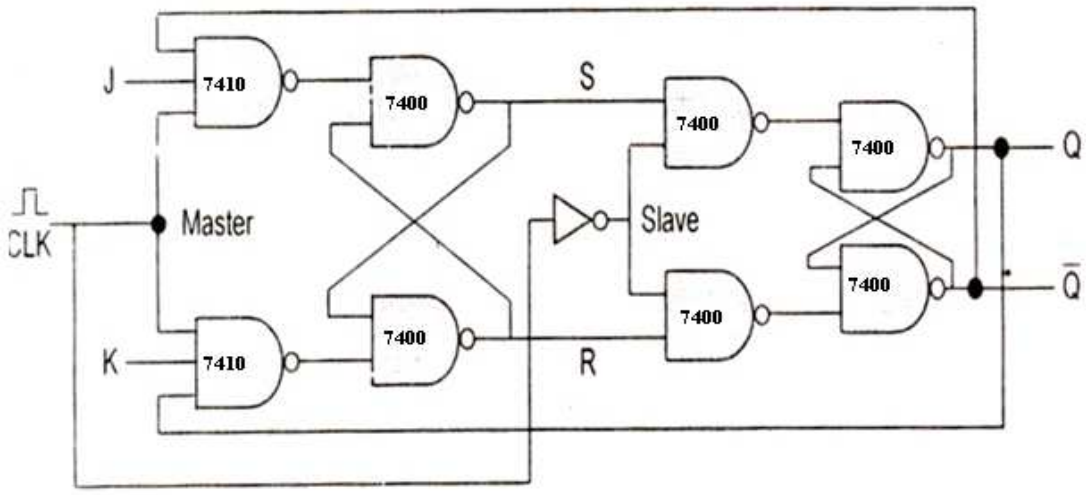
S	R	Q
0	0	No Change
0	1	0
1	0	1
1	1	Forbidden

J-k flip-flop using NAND gates



J	K	Q
0	0	No Change
0	1	0
1	0	1
1	1	Race around

J-K Master Slave using NAND gates



Procedure:

1. Connect the Flip-flop circuits as shown above.

2. Apply different combinations of inputs and observe the outputs

Precautions: All the connections should be made properly.

Result: Different Flip-flops using gates are constructed and their truth tables are verified

Questions: 1.List four Basic Flip-flop applications**?**

2. What advantage does a J-K Flip-flop have over an S-R**?**

3. What is meant by Race around condition**?**

11(a)DESIGN OF SHIFT REGISTER(TO VERIFY SERIAL TO PARALLEL,PARALLEL TO SERIAL,SERIAL TO SERIAL,PARALLEL TO PARALLEL)USING FLIP-FLOPS

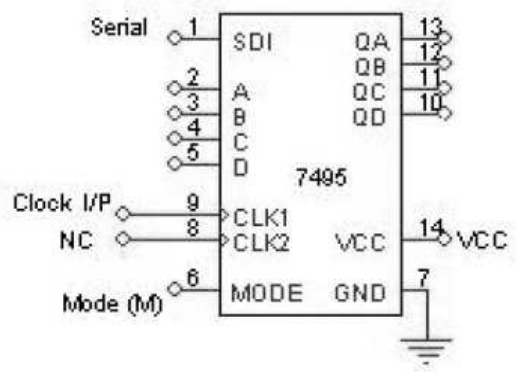
Aim:- To study shift register using IC 7495 in all its modes i.e.

SIPO/SISO, PISO/PIPO.

Apparatus: - IC 7495, etc.

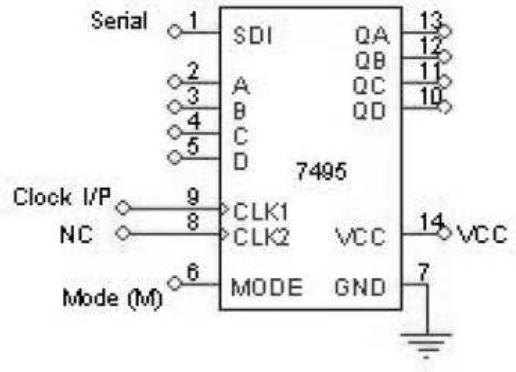
Circuit diagram :-

SIPO (Right Shift):-



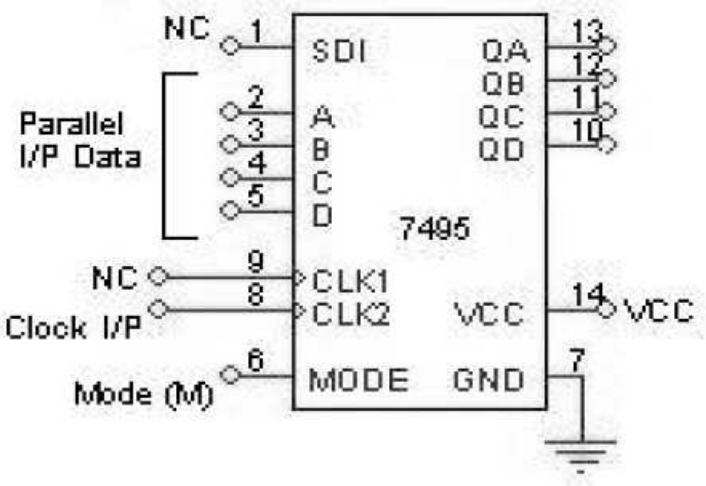
Clock	Serial i/p	QA	QB	QC	QD
1	0	0	X	X	X
2	1	1	0	X	X
3	1	1	1	0	X
4	1	1	1	1	0

SISO:-



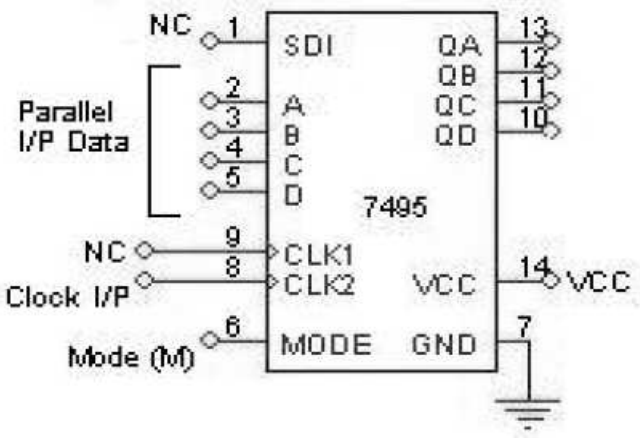
Clock	Serial i/p	QA	QB	QC	QD
1	do=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=do
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2
7	X	X	X	X	1=d3

PISO:-



Mode	Clock	Parallel i/p				Parallel o/p			
		A	B	C	D	QA	QB	QC	QD
1	1	1	0	1	1	1	0	1	1
0	2	X	X	X	X	X	1	0	1
0	3	X	X	X	X	X	X	1	0
0	4	X	X	X	X	X	X	X	1

PIPO:-



Clock	Parallel i/p				Parallel o/p			
	A	B	C	D	QA	QB	QC	QD
1	1	0	1	1	1	0	1	1

Procedure :

Serial In Parallel Out(SIPO):

1. Connections are made as per circuit diagram.
2. Apply the data at serial i/p
3. Apply one clock pulse at clock 1 (Right Shift) observe this data at QA.
4. Apply the next data at serial i/p.
5. Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new data applied will appear at QA.
6. Repeat steps 2 and 3 till all the 4 bits data are entered one by one into the shift register.

Serial In Serial Out (SISO):

1. Connections are made as per circuit diagram.
2. Load the shift register with 4 bits of data one by one serially.
3. At the end of 4th clock pulse the first data ‘d0’ appears at QD.
4. Apply another clock pulse; the second data ‘d1’ appears at QD.
5. Apply another clock pulse; the third data appears at QD.
6. Application of next clock pulse will enable the 4th data ‘d3’ to appear at QD. Thus the data applied serially at the input comes out serially at QD

Parallel In Serial Out (PISO):

1. Connections are made as per circuit diagram.
2. Apply the desired 4 bit data at A, B, C and D.

3. Keeping the mode control M=1 apply one clock pulse. The data applied at

   A, B, C and D will appear at QA, QB, QC and QD respectively.

4. Now mode control M=0. Apply clock pulses one by one and observe the

   Data coming out serially at QD

Parallel In Parallel Out (PIPO):

1. Connections are made as per circuit diagram.

2. Apply the 4 bit data at A, B, C and D.

3. Apply one clock pulse at Clock 2 (Note: Mode control M=1).

4. The 4 bit data at A, B, C and D appears at QA, QB, QC and QD

respectively.

Precautions: All the connections should be made properly.

Result: shift registers using IC 7495 in all its modes i.e.SIPO/SISO, PISO/PIPO are verified.

11(b).DESIGN OF RING AND JOHNSON COUNTERS USING FLIP-FLOPS

Aim: To design Ring counter and Johnson counter and verify their truth tables

Apparatus:

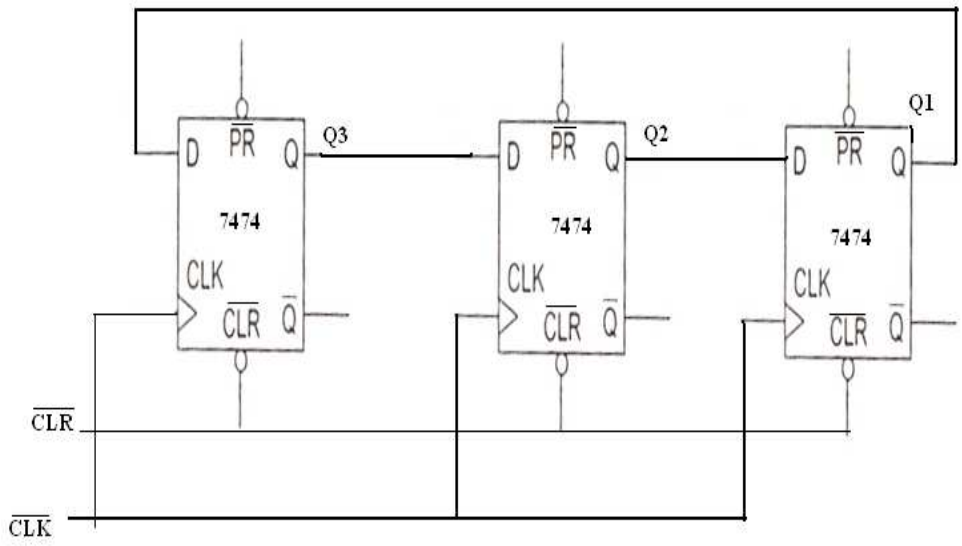
2. IC's - 7404, 7402, 7400

2. Electronic circuit designer

3. Connecting patch chords

Circuit Diagram:

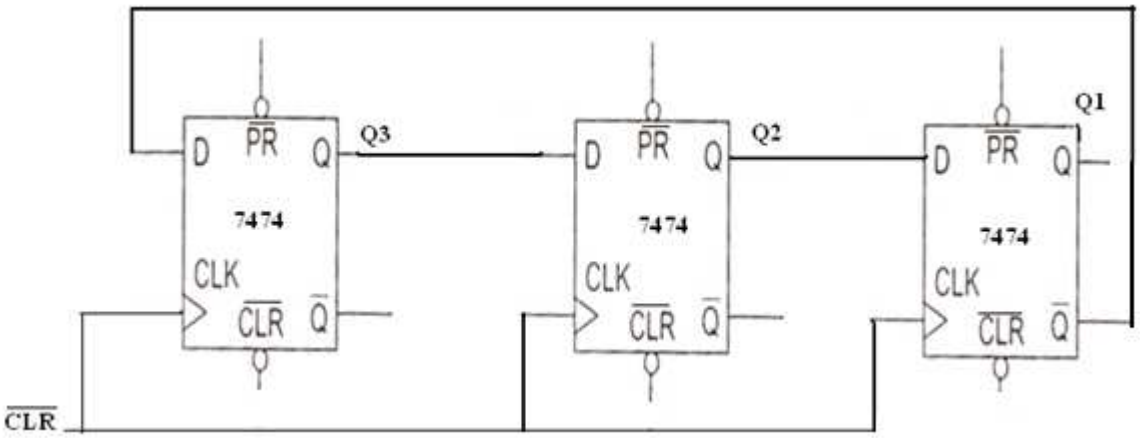
Ring Counter:



Truth Table

Clk	Q3	Q2	Q1
0	0	0	1
1	1	0	0
2	0	1	0

Johnson Counter:



Truth Table

Clk	Q3	Q2	Q1
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1

Procedure:

1. Connections are made as per the circuit diagram
2. Switch on the power supply.
3. Apply clock pulses and note the outputs after each clock pulse

Precautions:

1. All the connections should be made properly.

2. IC should not be reversed.

Result: Ring counter and Johnson counter are designed and their truth tables are verified.

12.DESIGN OFASYNCHRONOUS COUNTER, MOD COUNTER, UP COUNTER, DOWN COUNTER AND UP/DOWN COUNTER USING FLIP FLOPS

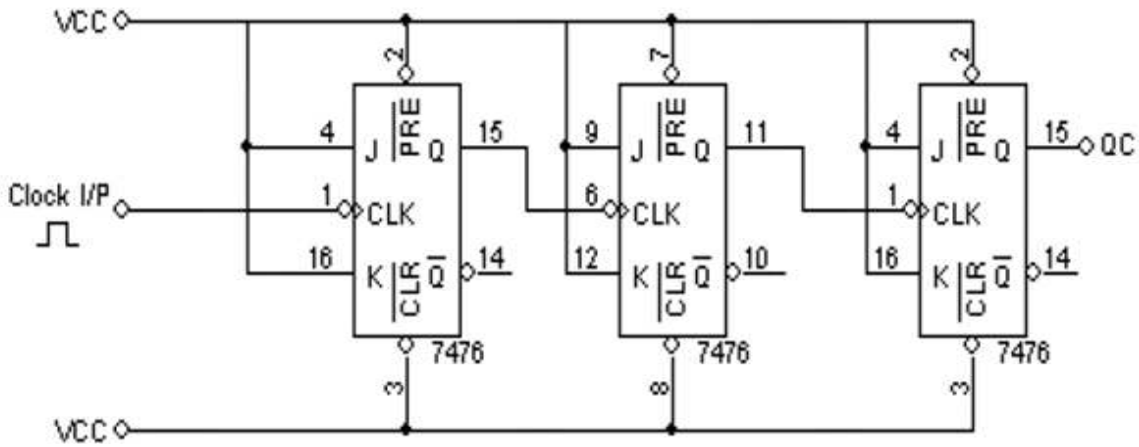
Aim:- To design and construct of 3-bit Asynchronous up and down counters,2-bit up/down counter.

Apparatus:

1. IC's - 7408,7476,7400,7432
2. Electronic circuit designer
3. Connecting patch chords

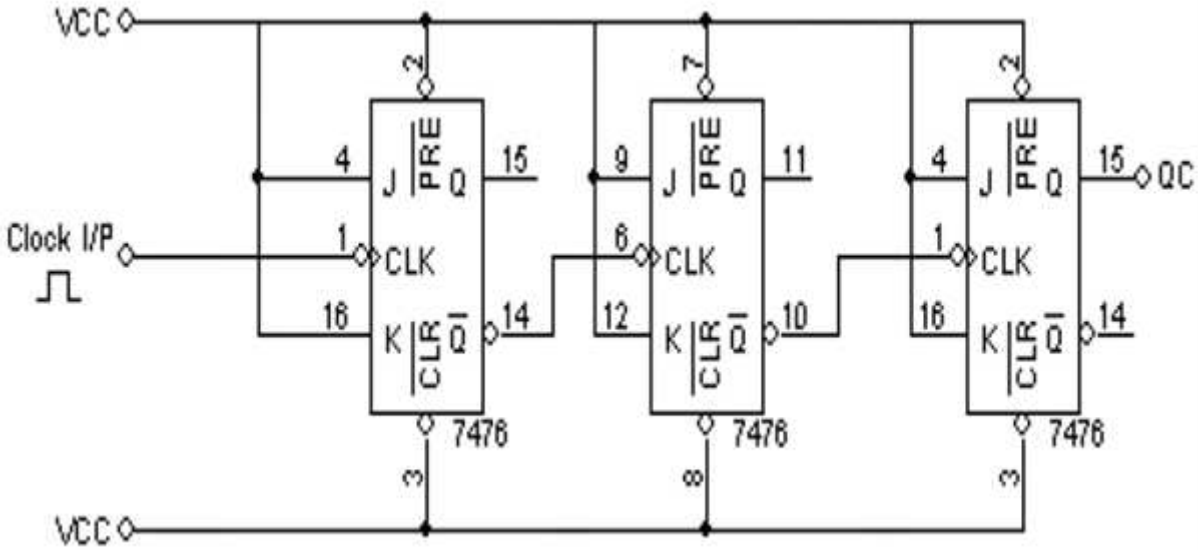
Circuit Diagram:

3-bit Asynchronous up counter:



3-bit Asynchronous up counter			
Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

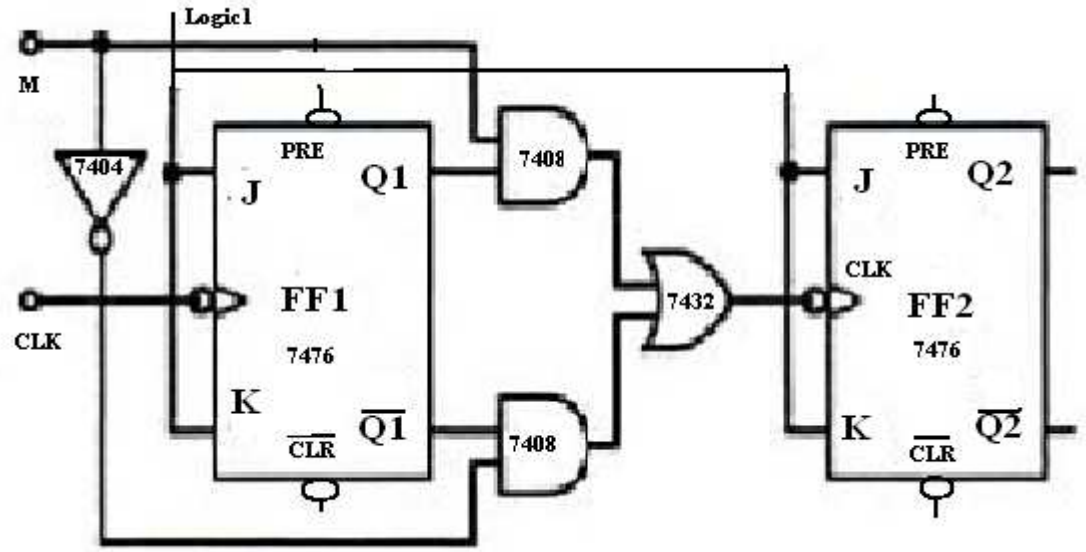
3-bit Asynchronous down counter:



TRUTH TABLE

3-bit Asynchronous down counter			
Clock	QC	QB	QA
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0
8	1	1	1
9	1	1	0

Two Bit up/Down Counter using negative edge-triggered flip-flops



WHEN M=1

CLK	Q2	Q1
0	0	0
1	0	1
2	1	0
3	1	1

WHEN M=0

CLK	Q2	Q1
0	1	1
1	1	0
2	0	1
3	0	0

Procedure:

1. Connections are made as per the circuit diagram

2. Switch on the power supply.

3. Apply clock pulses and note the outputs after each clock pulse and note done the out puts.

Precautions:

1. All the connections should be made properly.

2. IC should not be reversed.

Result: 3-bit Asynchronous up and down counters,2-bit up/down counter are designed and truth tables are verified.

13.DESIGN OF SYNCHRONOUS COUNTER, MOD COUNTER, UP COUNTER, DOWN COUNTER AND UP/DOWN COUNTER USING FLIP FLOPS

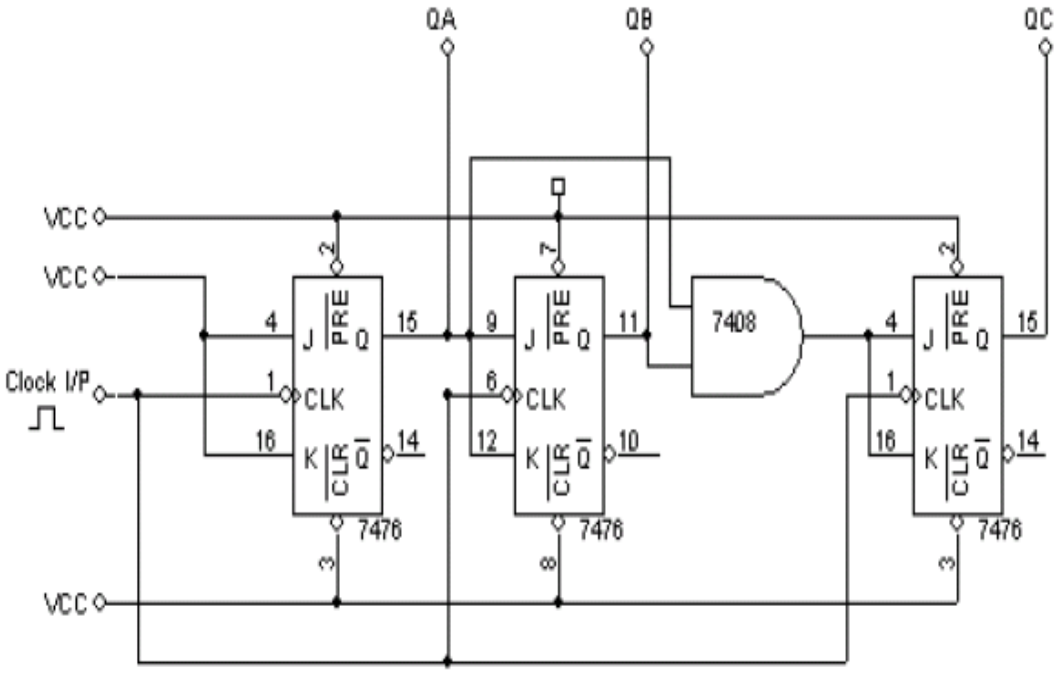
Aim:- To design and construct of 3-bit Synchronous up and down counters,2-bit up/down counter.

Apparatus:

1. IC's - 7408,7476,7400,7432
2. Electronic circuit designer
3. Connecting patch chords

Circuit Diagram:

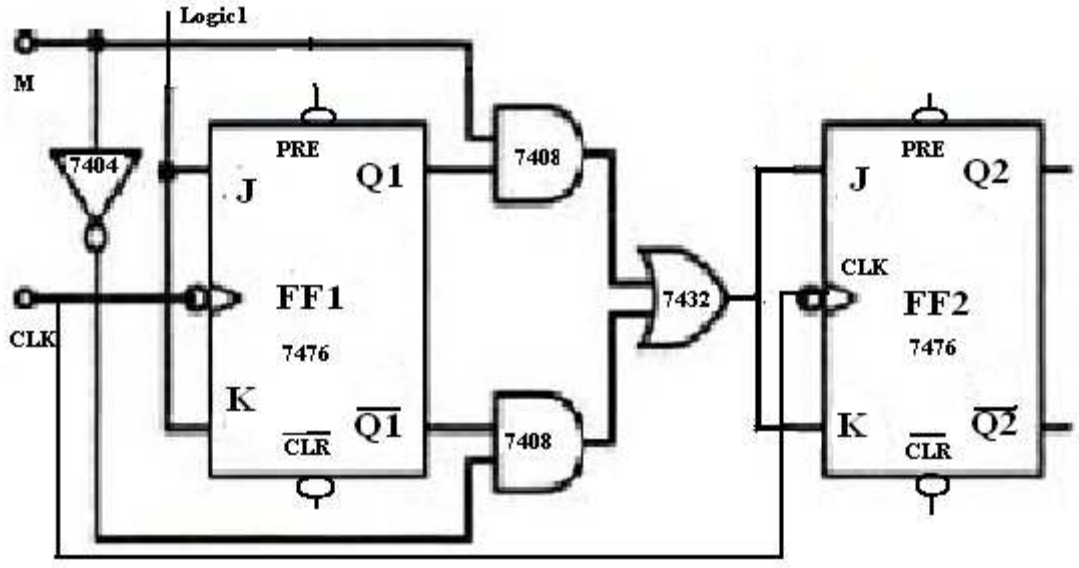
3-bit Synchronous Counter:-



Truth Table

3-bit synchronous up counter			
Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Two Bit up/Down Counter using negative edge-triggered flip-flops



WHEN M=1

CLK	Q2	Q1
0	0	0
1	0	1
2	1	0
3	1	1

WHEN M=0

CLK	Q2	Q1
0	1	1
1	1	0
2	0	1
3	0	0

Procedure:

1. Connections are made as per the circuit diagram

2. Switch on the power supply.

3. Apply clock pulses and note the outputs after each clock pulse and note done the out puts.

Precautions:

1. All the connections should be made properly.

2. IC should not be reversed.

Result: 3-bit Synchronous up and down counters,2-bit up/down counter are designed and truth tables are verified.

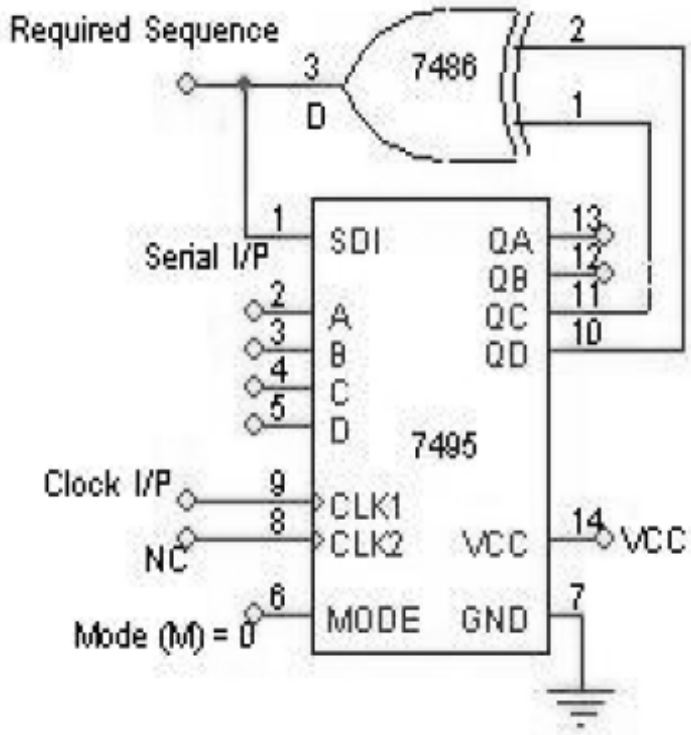
14. SEQUENCE GENERATOR

AIM: To design a sequence generator

APPARATUS: - IC7495

IC7486

Circuit Diagram



Truth Table

Map Value	Clock	QA	QB	QC	QD	o/p D
15	1	1	1	1	1	0
7	2	0	1	1	1	0
3	3	0	0	1	1	0
1	4	0	0	0	1	1
8	5	1	0	0	0	0
4	6	0	1	0	0	0
2	7	0	0	1	0	1
9	8	1	0	0	1	1
12	9	1	1	0	0	0
6	10	0	1	1	0	1
11	11	1	0	1	1	0
5	12	0	1	0	1	1
10	13	1	0	1	0	1
13	14	1	1	0	1	1
14	15	1	1	1	0	1

K-map for D

QCQD \ QA QB	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

Procedure:

1. Connections are made as per the circuit diagram

2. Switch on the power supply

3. Apply different combinations of inputs and observe the outputs; compare the outputs with the truth tables.

Precautions: All the connections should be made properly.

Result: Sequence generator is constructed and truth tables is verified