BASIC ELECTRONICS AND MICROPROCESSORS LAB MANUAL

ME-353

Prepared by

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(Any Ten Experiments)

1. P-N JUNCTION DIODE CHARACTERISTICS

AIM:-To observe and draw the Forward and Reverse bias V-I Characteristics of a P-N Junction diode.

APPARATUS:-

P-N Diode IN4007.
Regulated Power supply (0-30v)
Resistor 1KΩ
Ammeters (0-200 mA, 0-500mA)
Voltmeter (0-20 V)
Bread board
Connecting wires

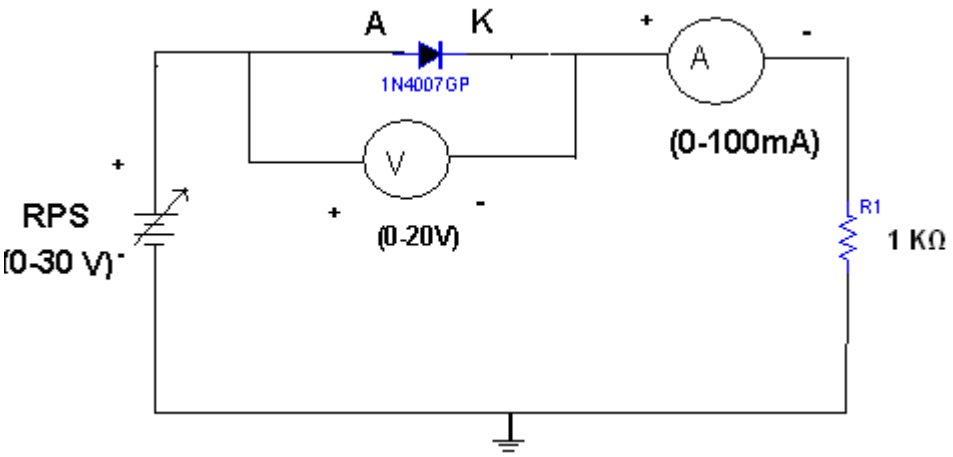
THEORY:-

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage.

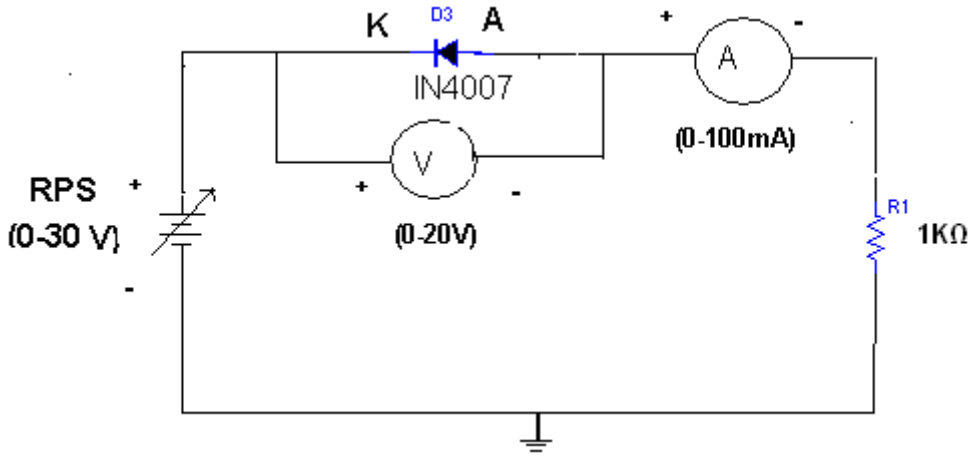
When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current due to minority charge carriers.

CIRCUIT DIAGRAMs:-

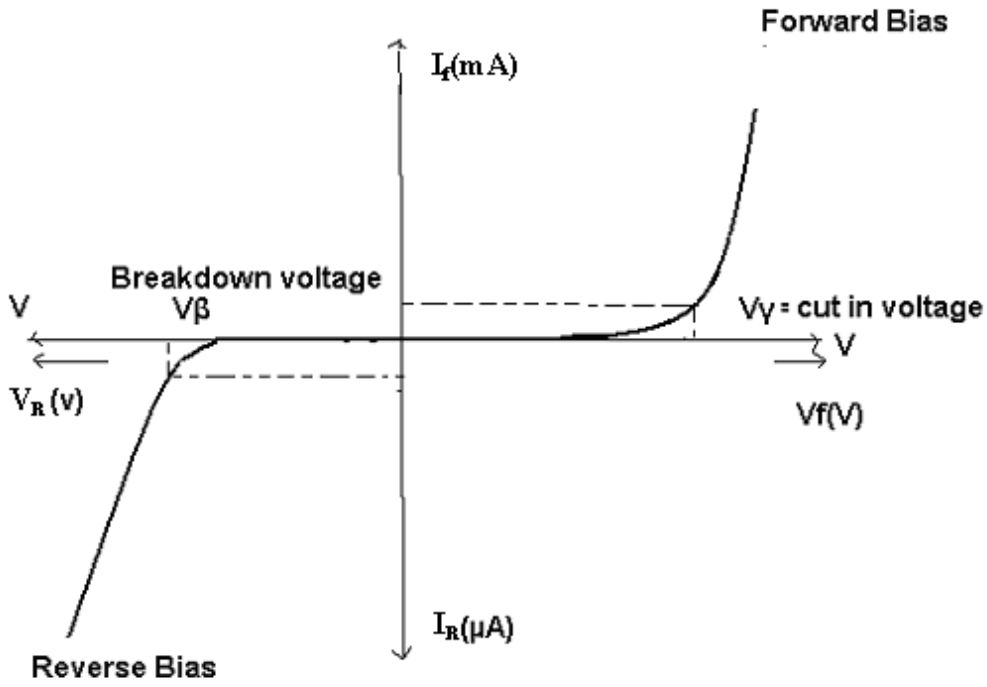
FORWARD BIAS:-



REVERSE BIAS:-



MODEL WAVEFORM:-



PROCEDURE:-

FORWARD BIAS:-

1. Connections are made as per the circuit diagram.
2. For forward bias, the RPS +ve is connected to the anode of the diode and RPS –ve is connected to the cathode of the diode.
3. Switch on the power supply and increases the input voltage (supply voltage) in Steps.
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The reading of voltage and current are tabulated.
6. Graph is plotted between voltage and current.

OBSERVATION:-

S.NO	APPLIED VOLTAGE (V)	VOLTAGE ACROSS DIODE(V)	CURRENT THROUGH DIODE(mA)

PROCEDURE:-

REVERSE BIAS:-

1. Connections are made as per the circuit diagram
2. For reverse bias, the RPS +ve is connected to the cathode of the diode and RPS –ve is connected to the anode of the diode.
3. Switch on the power supply and increase the input voltage (supply voltage) in Steps
4. Note down the corresponding current flowing through the diode voltage across the diode for each and every step of the input voltage.
5. The readings of voltage and current are tabulated
6. Graph is plotted between voltage and current.

OBSEVATION:-

S.NO	APPLIEDVOLTAGE ACROSSDIODE(V)	VOLTAGE ACROSS DIODE(V)	CURRENT THROUGH DIODE(mA)

PRECAUTIONS:-

1. All the connections should be correct.
2. Parallax error should be avoided while taking the readings from the Analog meters.

RESULT:- Forward and Reverse Bias characteristics for a p-n diode is observed

2. ZENER DIODE CHARACTERISTICS

AIM: - a) To observe and draw the static characteristics of a zener diode

b) To find the voltage regulation of a given zener diode

APPARATUS*: -*

Zener diode.

Regulated Power Supply (0-30v).

Voltmeter (0-20v)

Ammeter (0-100mA)

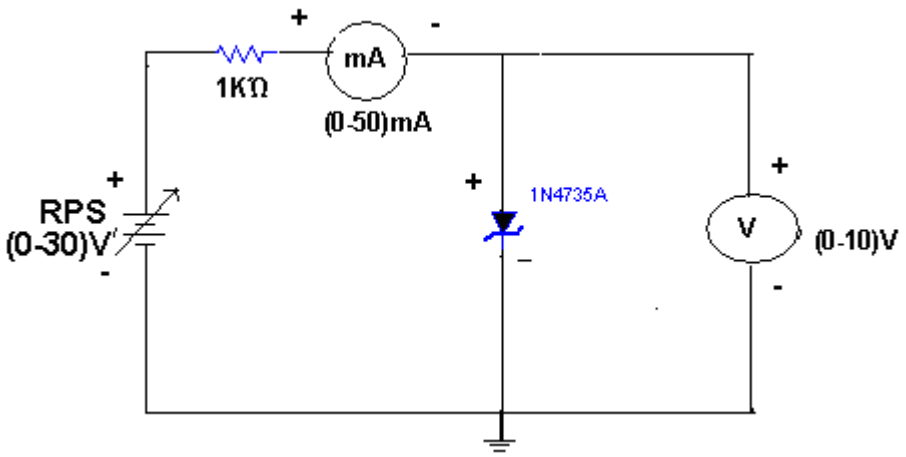
Resistor (1KΩ)

Bread Board

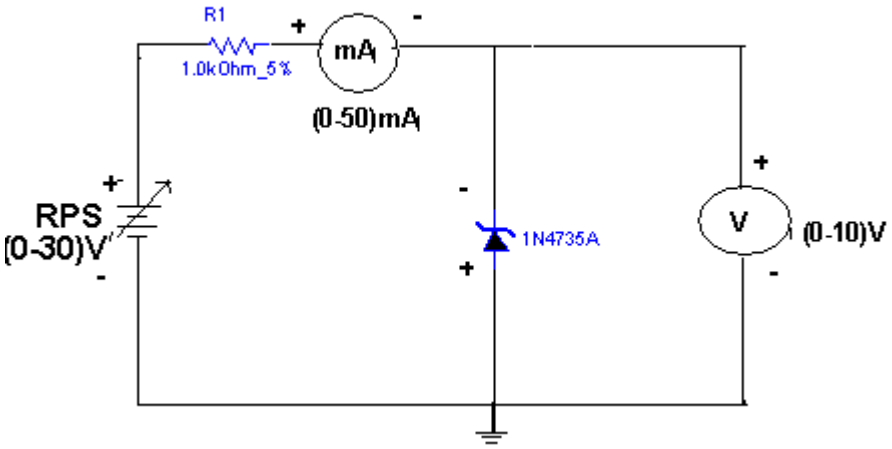
Connecting wires

CIRCUIT DIAGRAM:-

STATIC CHARACTERISTICS:-



REGULATION CHARACTERISTICS:-



Theory:-

A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device

To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals what ever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

PROCEDURE:-

Static characteristics:-

1. Connections are made as per the circuit diagram.
2. The Regulated power supply voltage is increased in steps.
3. The zener current (lz), and the zener voltage (Vz.) are observed and then noted in the tabular form.
4. A graph is plotted between zener current (Iz) and zener voltage (Vz).

Regulation characteristics:-

1. The voltage regulation of any device is usually expressed as percentage regulation
2. The percentage regulation is given by the formula

$((V_{NL}-V_{FL})/V_{FL})X100$

V_{NL}=Voltage across the diode, when no load is connected.

V_{FL}=Voltage across the diode, when load is connected.

3. Connection are made as per the circuit diagram
4. The load is placed in full load condition and the zener voltage (Vz), Zener current (Iz), load current (I_L) are measured.
5. The above step is repeated by decreasing the value of the load in steps.
6. All the readings are tabulated.
7. The percentage regulation is calculated using the above formula

OBSERVATIONS:-

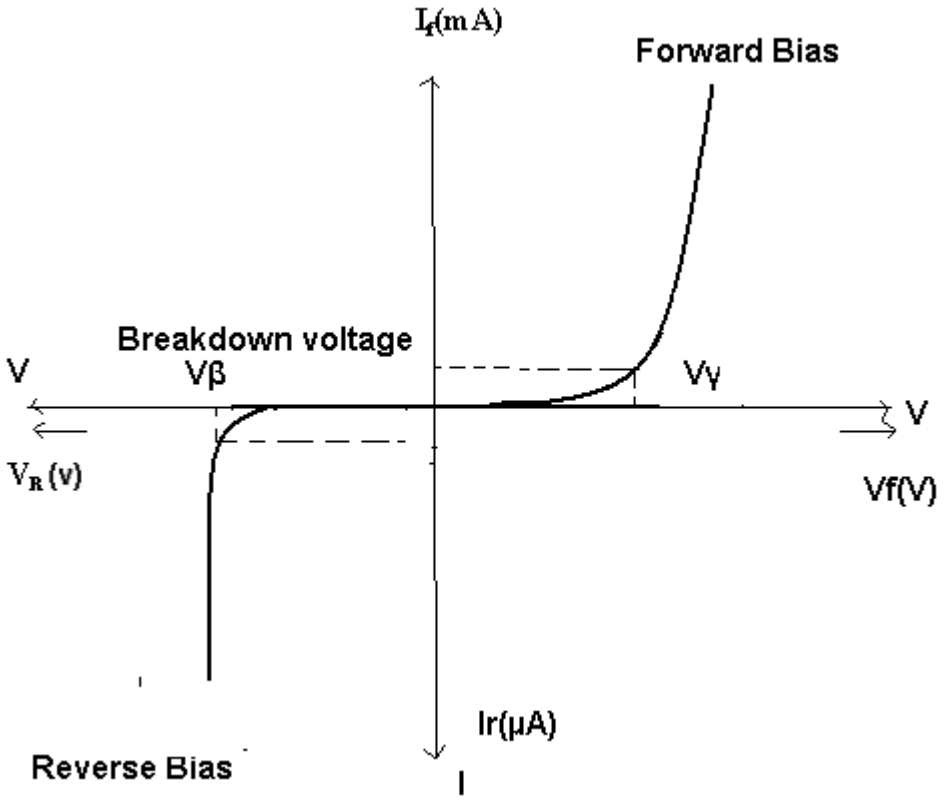
Static characteristics:-

S.NO	ZENER VOLTAGE(V_Z)	ZENER CURRENT(I_Z)

Regulation characteristics:-

S.N0	V_{NL}(VOLTS)	V_{FL} (VOLTS)	R_L (KΩ)	% REGULATION

MODEL WAVEFORMS:-



PRECAUTIONS:-

1. The terminals of the zener diode should be properly identified
2. While determined the load regulation, load should not be immediately shorted.
3. Should be ensured that the applied voltages & currents do not exceed the ratings of the diode.

RESULT:-

a) Static characteristics of zener diode are obtained and drawn.

b) Percentage regulation of zener diode is calculated.

3. HALF – WAVE RECTIFIER

AIM: - To obtain the load regulation and ripple factor of a half-rectifier.

1. with Filter
2. without Filter

APPARATUS:-

Experimental Board
Multimeters –2No's.
Transformer (6-0-6).
Diode, 1N 4007
Capacitor 100µf.
Resistor 1KΩ.
Connecting wires

THEORY: -

During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage.

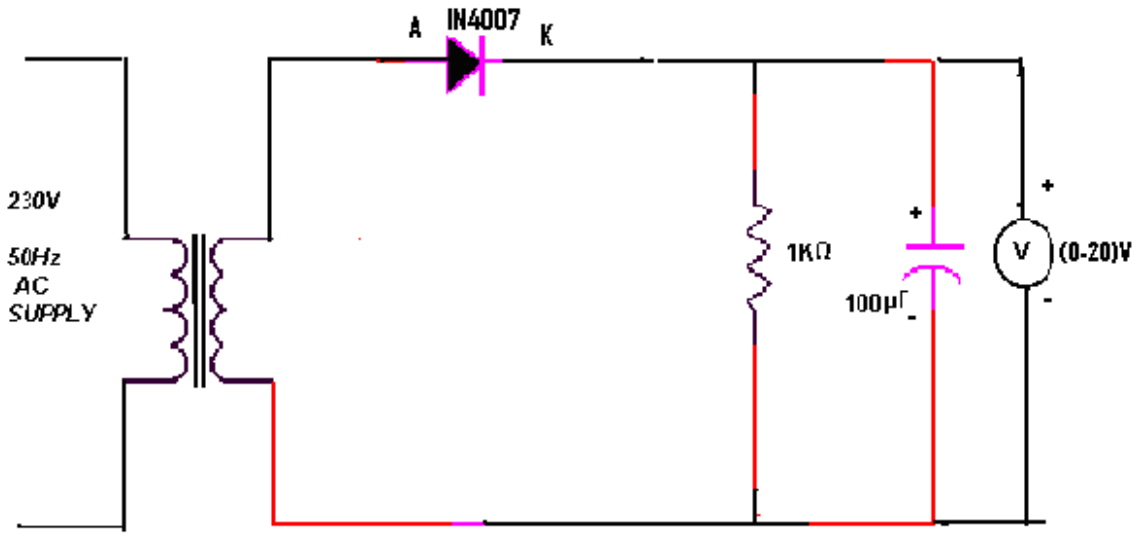
During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e, the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter.

For practical circuits, transformer coupling is usually provided for two reasons.

1. The voltage can be stepped-up or stepped-down, as needed.

2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit.

CIRCUIT DIAGRAM:-



PROCEDURE:-

1. Connections are made as per the circuit diagram.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltage at the output of the rectifier.
4. Find the theoretical of dc voltage by using the formula,

$$V_{dc}=V_m/\pi$$

Where, $V_m=2V_{rms}$, (V_{rms}=output ac voltage.)

The Ripple factor is calculated by using the formula

r=ac output voltage/dc output voltage.

REGULATION CHARACTERSTICS:-

1. Connections are made as per the circuit diagram.
2. By increasing the value of the rheostat, the voltage across the load and current flowing through the load are measured.
3. The reading is tabulated.
4. Draw a graph between load voltage (V_L and load current (I_L) taking V_L on X-axis and I_L on y-axis
5. From the value of no-load voltages, the %regulation is calculated using the formula,

Theoretical calculations for Ripple factor:-

Without Filter*:-*

Vrms=Vm/2

Vm=2Vrms

Vdc=Vm/ π

Ripple factor r=$\sqrt{}$ (Vrms/ Vdc)^2 -1 =1.21

With Filter:-

Ripple factor, r=1/ (2$\sqrt{}$3 f C R)

Where f =50Hz

C =100μF

R_L=1KΩ

PRACTICAL CALCULATIONS:-

Vac=

Vdc=

Ripple factor with out Filter =

Ripple factor with Filter =

OBSERVATIONS:-

WITHOUT FILTER:-

Vdc=Vm/π, Vrms=Vm/2, Vac=√ ($Vrms^2$- Vdc^2)

V_m(v)	V_{ac}(v)	V_{dc}(v)	r= V_{ac}/ V_{dc}

WITH FILTER

V_1(V)	V_2(V)	V_{dc}= (V_1+V_2)/2	V_{ac}= (V_1- V_2)/2√3	r = V_{ac}/ V_{dc}

PRECAUTIONS:

1. The primary and secondary sides of the transformer should be carefully identified.
2. The polarities of the diode should be carefully identified.
3. While determining the % regulation, first Full load should be applied and then it should be decremented in steps.

RESULT:-

1. The Ripple factor for the Half-Wave Rectifier with and without filters is measured.
2. The % regulation of the Half-Wave rectifier is calculated

4. TRANSISTOR CE CHARACTERSTICS

AIM: 1. To draw the input and output characteristics of transistor connected in CE configuration

2. To find β of the given transistor.

APPARATUS:

Transistor (BC 107)

R.P.S (O-30V) 2Nos

Voltmeters (0-20V) 2Nos

Ammeters (0-200μA), (0-500mA)

Resistors 1KΩ

Bread board

THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and out put is taken across the collector and emitter terminals.
Therefore the emitter terminal is common to both input and output.

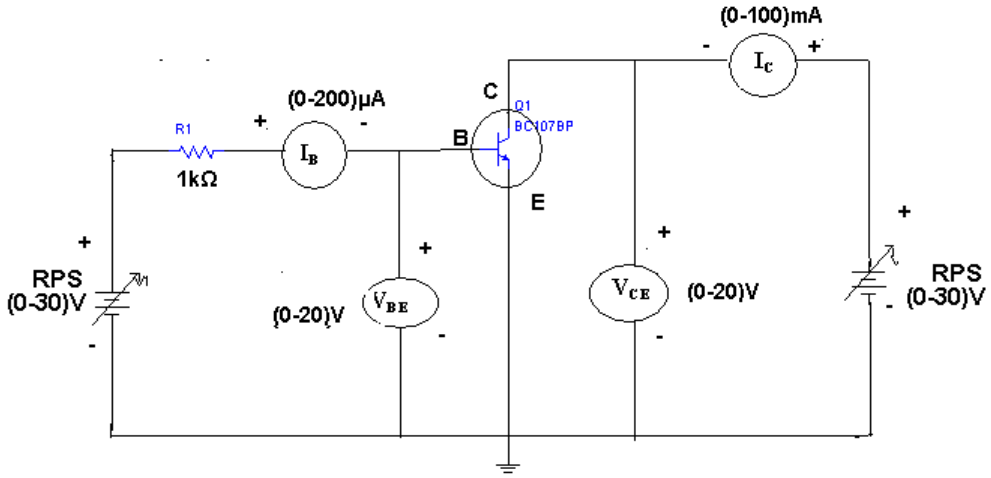
The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE} . Therefore input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between I_c and V_{CE} at constant I_B. the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to I_B.

The current amplification factor of CE configuration is given by

$$B = \Delta I_C / \Delta I_B$$

CIRCUIT DIAGRAM:



PROCEDURE:

INPUT CHARECTERSTICS:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 1V and for different values of V_{BE} . Note down the values of I_C
3. Repeat the above step by keeping V_{CE} at 2V and 4V.
4. Tabulate all the readings.
5. plot the graph between V_{BE} and I_B for constant V_{CE}

OUTPUT CHARACTERSTICS:

1. Connect the circuit as per the circuit diagram
2. for plotting the output characteristics the input current I_B is kept constant at 10µA and for different values of V_{CE} note down the values of I_C
3. repeat the above step by keeping IB at 75 µA 100 µA
4. tabulate the all the readings
5. plot the graph between V_{CE} and I_C for constant I_B

OBSERVATIONS:

INPUT CHARACTERISTICS:

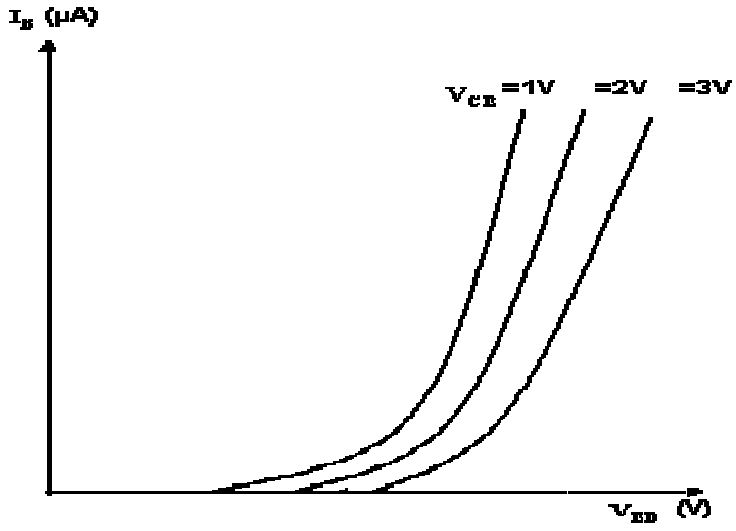
S.NO	V_{CE} = 1V		V_{CE} = 2V		V_{CE} = 4V	
	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)

OUT PUT CHAREACTARISTICS:

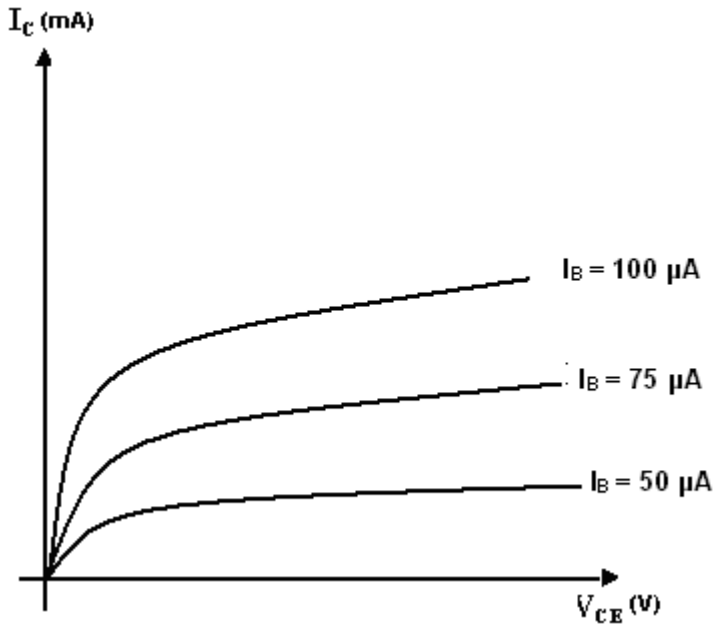
S.NO	I_B = 50 μA		I_B = 75 μA		I_B = 100 μA	
	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_CmA)	V_{CE}(V)	I_C(mA)

MODEL GRAPHS:

INPUT CHARACTERSTICS:



OUTPUT CHARECTERSTICS:



PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor
2. Meters should be connected properly according to their polarities

RESULT:

1. the input and out put characteristics of a transistor in CE configuration are Drawn
2. the β of a given transistor is calculated

5. FET CHARACTERISTICS

AIM: a). To draw the drain and transfer characteristics of a given FET.

b). To find the drain resistance (r_d) amplification factor (μ) and Tran conductance (g_m) of the given FET.

APPARATUS: FET (BFW-11)
Regulated power supply
Voltmeter (0-20V)
Ammeter (0-100mA)
Bread board
Connecting wires

THEORY:

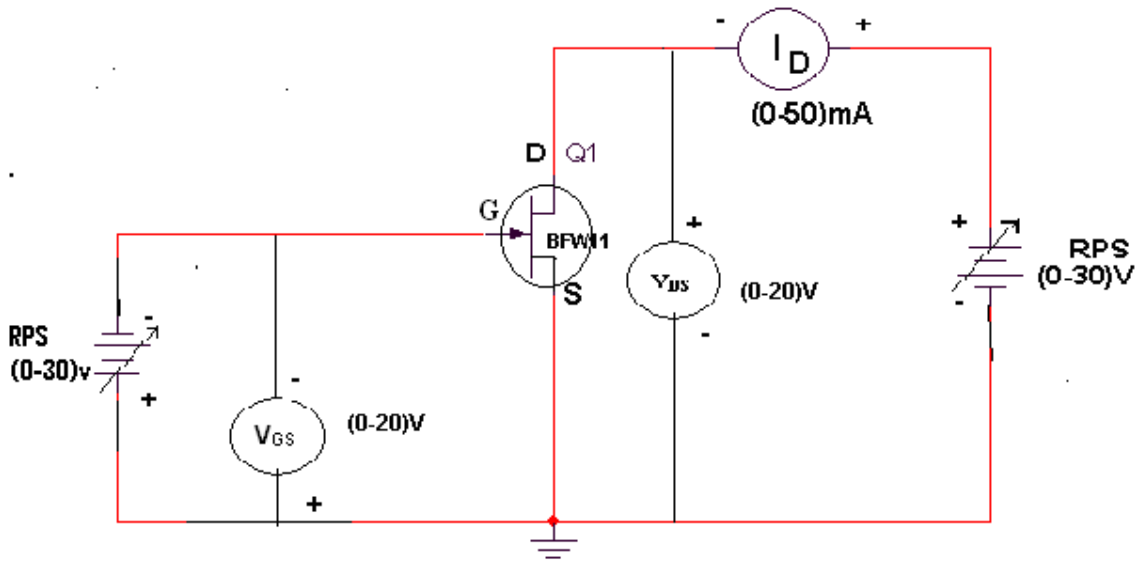
A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with $V_{DS.}$ With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The V_{DS} at this instant is called “pinch of voltage”.

If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage ill is decreased.

In amplifier application, the FET is always used in the region beyond the pinch-off.

$$F_{DS}=I_{DSS}(1-V_{GS}/V_P)\text{^}2$$

CIRCUIT DIAGRAM



PROCEDURE:

1. All the connections are made as per the circuit diagram.
2. To plot the drain characteristics, keep V_{GS} constant at 0V.
3. Vary the V_{DD} and observe the values of V_{DS} and I_D.
4. Repeat the above steps 2, 3 for different values of V_{GS} at 0.1V and 0.2V.
5. All the readings are tabulated.
6. To plot the transfer characteristics, keep V_{DS} constant at 1V.
7. Vary V_{GG} and observe the values of V_{GS} and I_D.
8. Repeat steps 6 and 7 for different values of V_{DS} at 1.5 V and 2V.
9. The readings are tabulated.
10. From drain characteristics, calculate the values of dynamic resistance (r_d) by using the formula

$$r_d = \Delta V_{DS}/\Delta I_D$$

11. From transfer characteristics, calculate the value of transconductace (g_m) By using the formula

$$G_m = \Delta I_D/\Delta V_{DS}$$

12. Amplification factor (μ) = dynamic resistance. Tran conductance

$$\mu = \Delta V_{DS}/\Delta V_{GS}$$

OBSERVATIONS:

DRAIN CHARACTERISTICS:

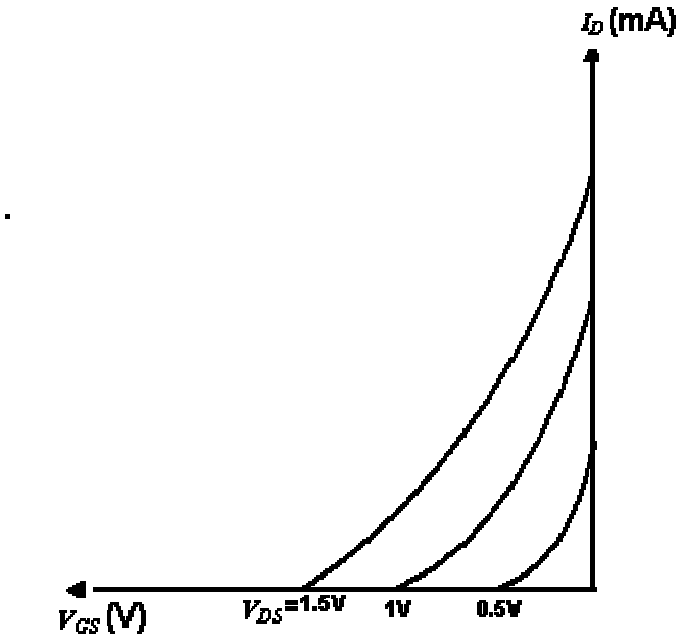
S.NO	V_{GS}=0V		V_{GS}=0.1V		$V_{GS=}$0.2V	
	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)

TRANSFER CHARACTERISTICS:

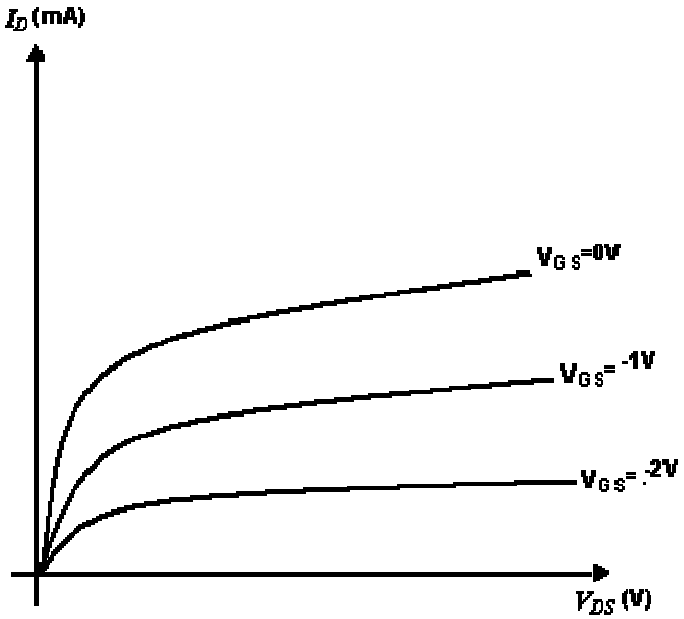
S.NO	V_{DS} =0.5V		V_{DS}=1V		V_{DS} =1.5V	
	V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)

MODEL GRAPH:

TRANSFER CHARACTERISTICS



DRAIN CHARACTERISTICS



PRECAUTIONS:

1. The three terminals of the FET must be care fully identified
2. Practically FET contains four terminals, which are called source, drain, Gate, substrate.
3. Source and case should be short circuited.
4. Voltages exceeding the ratings of the FET should not be applied.

RESULT :

1. The drain and transfer characteristics of a given FET are drawn
2. The dynamic resistance (r_d), amplification factor (μ) and Tran conductance (g_m) of the given FET are calculated.

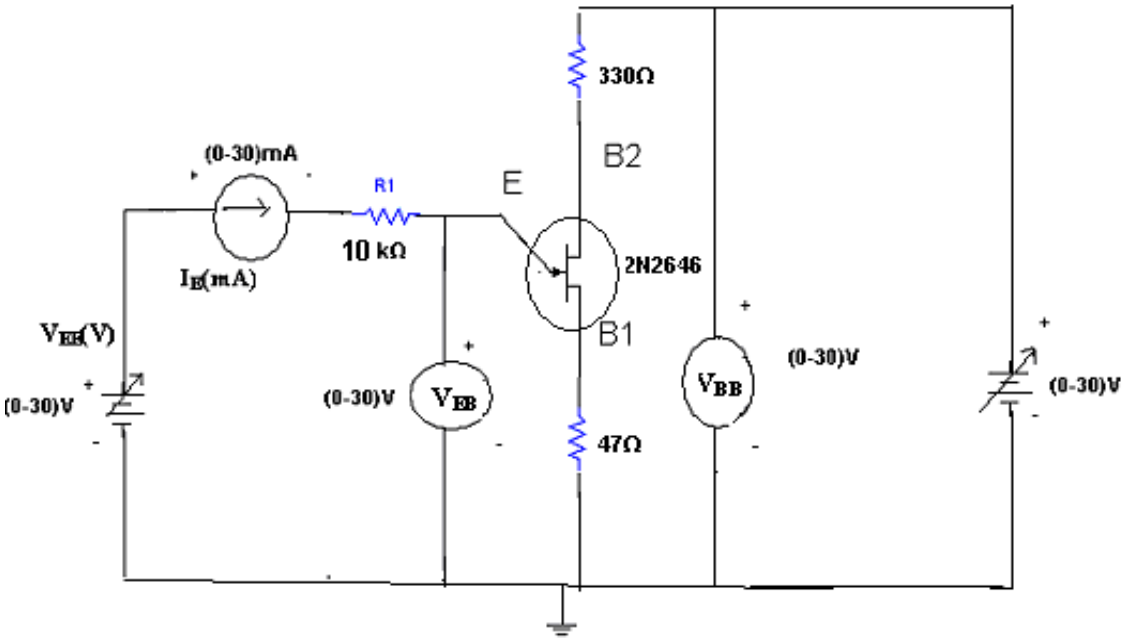
6 UJT CHARACTERISTICS

AIM: To observe the characteristics of UJT and to calculate the Intrinsic Stand-Off Ratio (η).

APPARATUS:

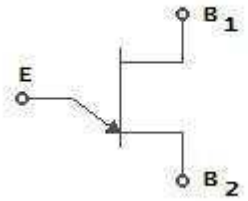
Regulated Power Supply (0-30V, 1A) - 2Nos
UJT 2N2646
Resistors 10kΩ, 47Ω, 330Ω
Multimeters - 2Nos
Breadboard
Connecting Wires

CIRCUIT DIAGRAM



THEORY:

A Unijunction Transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT Unijunction Transistor (UJT) has three terminals an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance.The original unijunction transistor, or UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length. The 2N2646 is the most commonly used version of the UJT.



Circuit symbol

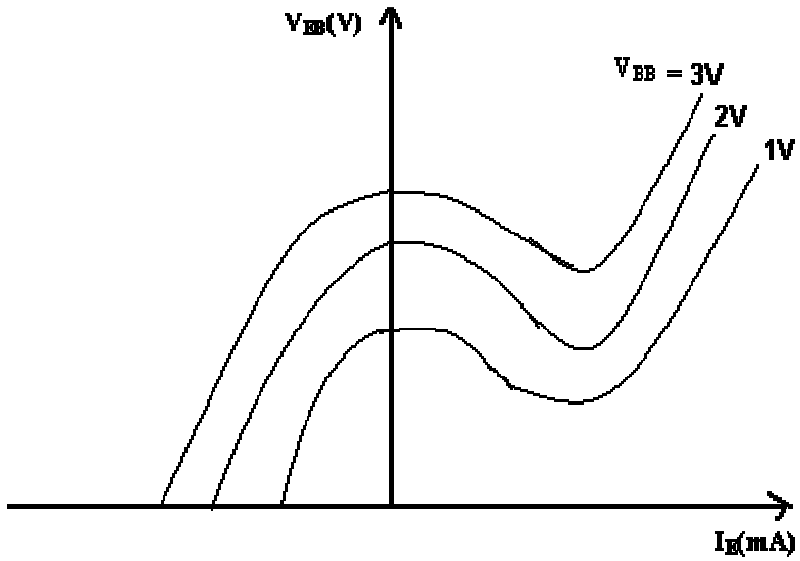
The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits.When the emitter voltage reaches V_p, the current startsto increase and the emitter voltage starts to decrease.This is represented by negative slope of the characteristics which is reffered to as the negative

resistance region,beyond the valleypoint ,R_{B1} reaches minimum value and this region,V_{EB} propotional to $I_{E.}$

PROCEDURE:

1. Connection is made as per circuit diagram.
2. Output voltage is fixed at a constant level and by varying input voltage corresponding emitter current values are noted down.
3. This procedure is repeated for different values of output voltages.
4. All the readings are tabulated and Intrinsic Stand-Off ratio is calculated using $\eta = (V_p - V_D) / V_{BB}$
5. A graph is plotted between V_{EE} and I_E for different values of $V_{BE.}$

MODEL GRAPH:



OBSEVATIONS:

V_{BB}=1V		V_{BB}=2V		V_{BB}=3V	
V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)

CALCULATIONS:

$$V_P = \eta V_{BB} + V_D$$

$$\eta = (V_P - V_D) / V_{BB}$$

$$\eta = (\eta_1 + \eta_2 + \eta_3) / 3$$

RESULT: The characteristics of UJT are observed and the values of Intrinsic Stand-Off Ratio is calculated

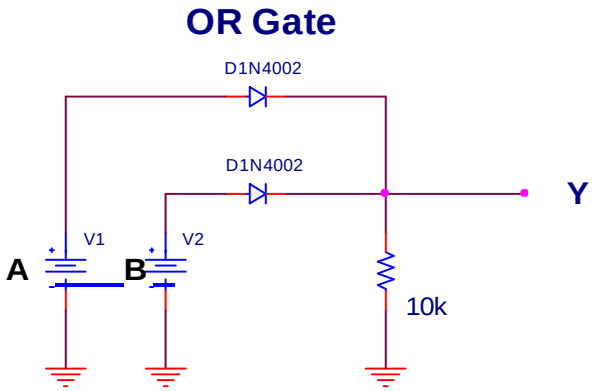
7 Logic Gates using Discrete Components.

Aim: To construct logic gates **OR, AND, NOT, NOR, NAND** gates using discrete components and verify their truth tables

Apparatus:

1. Digital circuit designer
2. Resistors 10k,1k,220ohms
3. Transistors 2N2222(NPN)
4. Diodes 1N 4001
5. Connecting wires

Circuit Diagram:

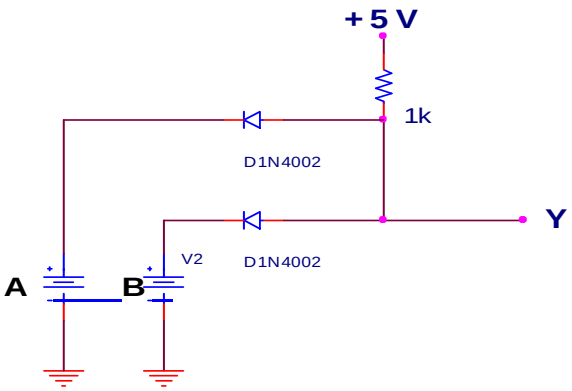


Truth Table

A	B	Y

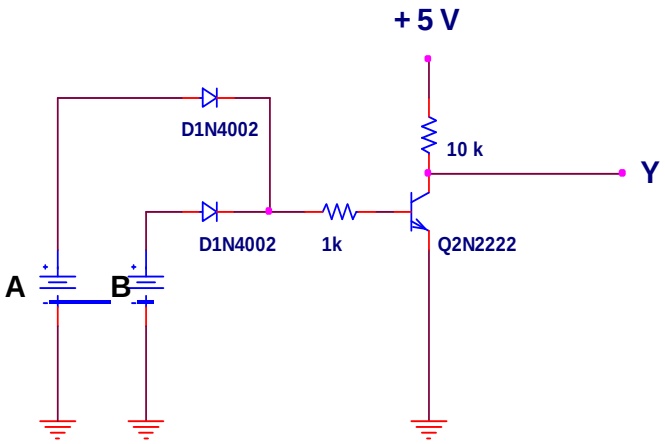
Truth Table

AND Gate

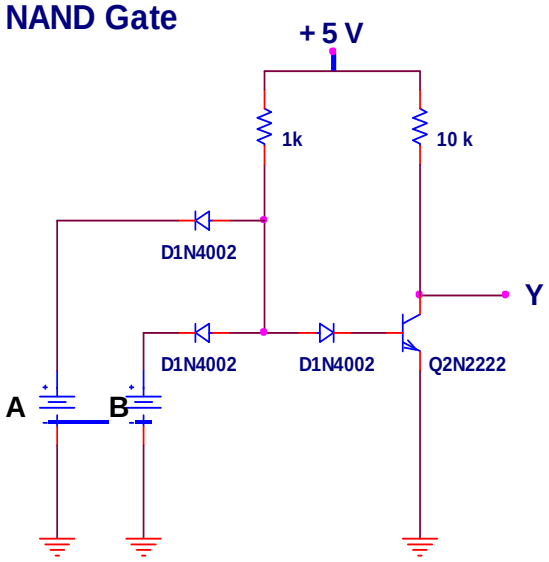


Truth Table

NOR Gate



NAND Gate



PROCEDURE:

1 Connections are made as per the circuit diagram

2 Switch on the power supply

3 Apply different combinations of inputs and observe the out puts

PRECAUTIONS:

1. All the connections should be properly.

2. IC should not be reverse.

Results:

8 Logic Gates using Universal Gate (NAND)

AIM: To construct logic gates AND, NOT, EX-NOR and EX-OR using NANAD gates and verify their truth tables.

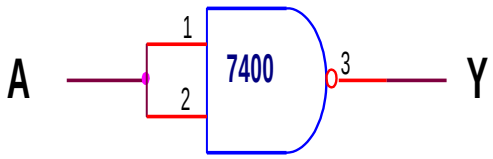
APPARATUS: IC 7400

Digital circuit designer

Connecting wires

Circuit Diagram:

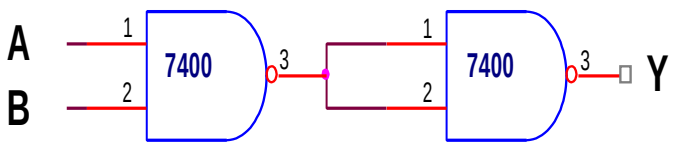
NOT Gate



Truth Table

A	Y
1	0
0	1

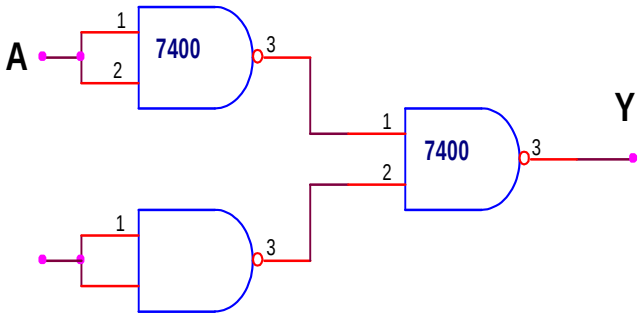
AND Gate



Truth Table

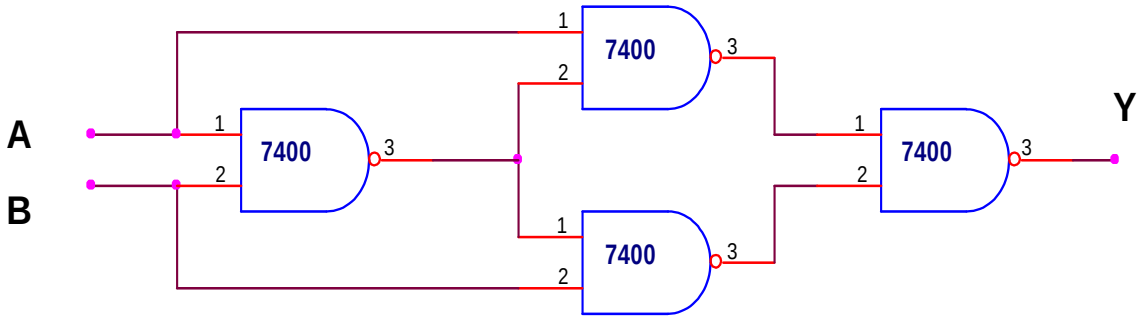
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate



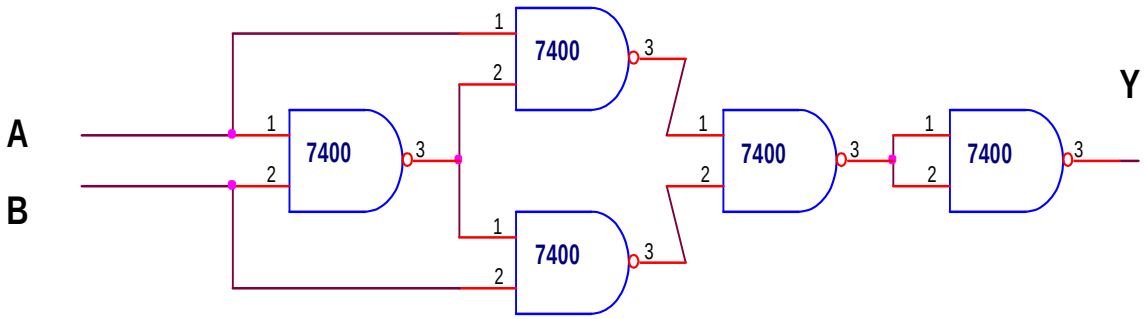
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

EX-OR Gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

EX-NOR Gate



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

PROCEDURE:

4 Connections are made as per the circuit diagram

5 Switch on the power supply

6 Apply different combinations of inputs and observe the out puts

PRECAUTIONS:

1. All the connections should be properly.

2. IC should not be reverse.

Results:

9 Combinational Circuits (half adder, full adder, half subtractor).

Aim: - To realize half/full adder and half/full subtractor.

i. Using X-OR and basic gates

ii. Using only nand gates.

Apparatus Required: -

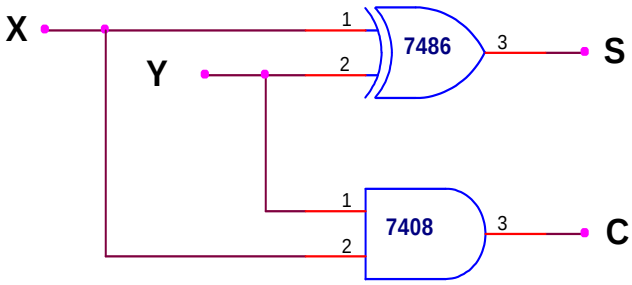
1.Digital circuit designer.

2. IC 7486, IC 7432, IC 7408, IC 7400, etc.

3. Connecting wires.

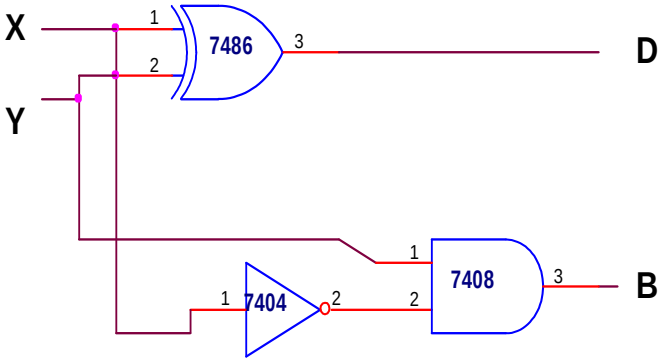
Circuit Diagram:

Half Adder:



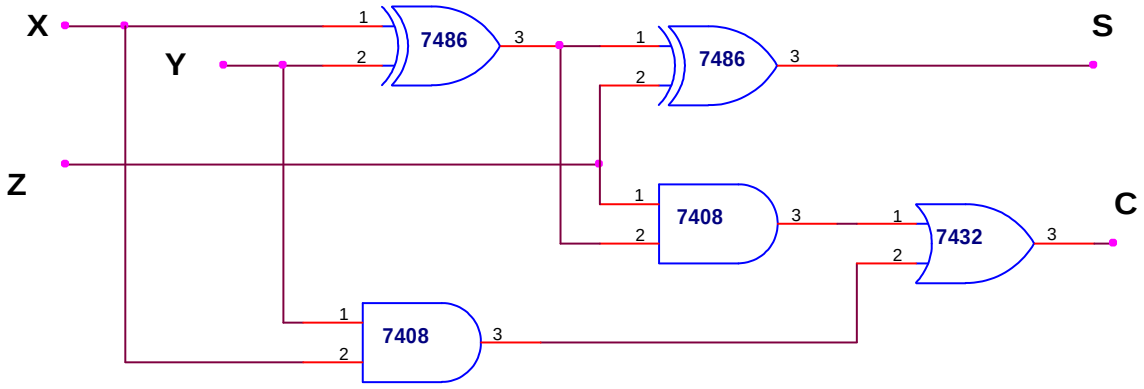
Half Adder					
A	B	S	C	S(V)	C(V)
	0	0	0		
0	1	1	0		
1	0	1	0		
1	1	0	1		

Half Subtractor



Half Subtractor					
A	B	D	B	D(V)	B(V)
0	0	0	0		
0	1	1	1		
1	0	1	0		
1	1	0	0		

Full Adder:



Full Adder						
A	B	Cn-1	S	C	S(V)	C(V)
0	0	0	0	0		
0	0	1	1	0		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	0	1		
1	1	0	0	1		
1	1	1	1	1		

Procedure: -

1. Verify the gates.

2. Make the connections as per the circuit diagram.

3. Switch on V_{CC} and apply various combinations of input according to the truth table.

4. Note down the output readings for half/full adder and half subtractor sum/difference and the carry/borrow bit for different combinations of inputs.

Results:

10. Verification of Flip-Flop (JK & D etc.,)

AIM: To study the fundamentals of basic memory units and to become familiar with various types of flip-flops and verifying the Truth tables of Flip- Flops:

(i) RS-Type (ii) JK-Type (iii) T- Type. (iv) D- Type

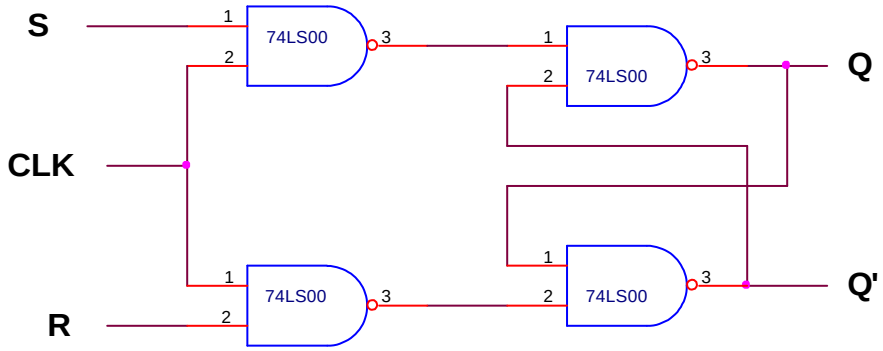
APPARATUS

1.Digital circuit designer.

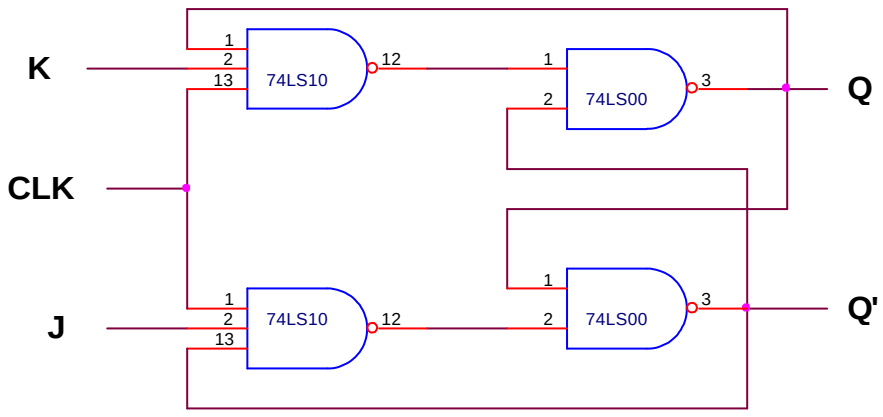
2. IC 7476, IC 7404, IC 7400, etc.

3. Connecting wires.

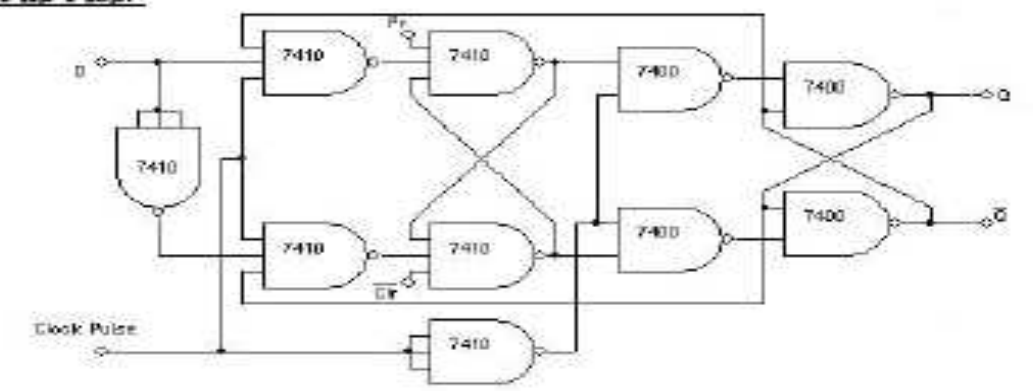
R S Flip Flop Using NAND Gates



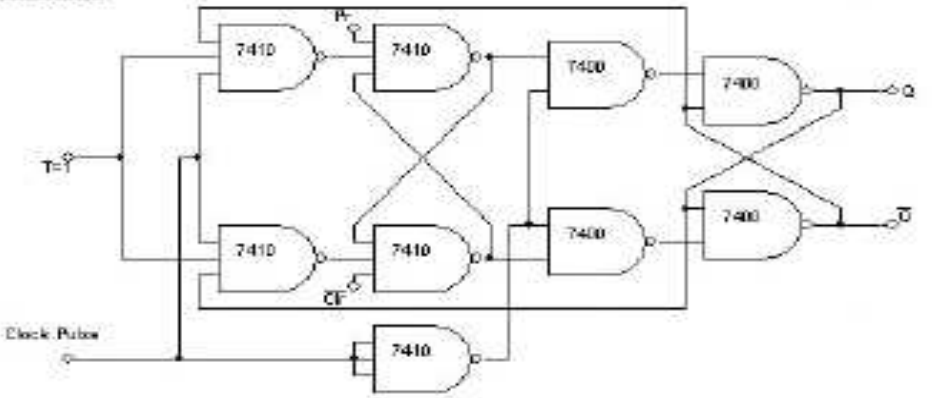
J K Flip Flop Using NAND Gates



D Flip-Flop:-



T Flip-Flop:-



11 Code Converters (Gray to Binary & Binary to Gray)

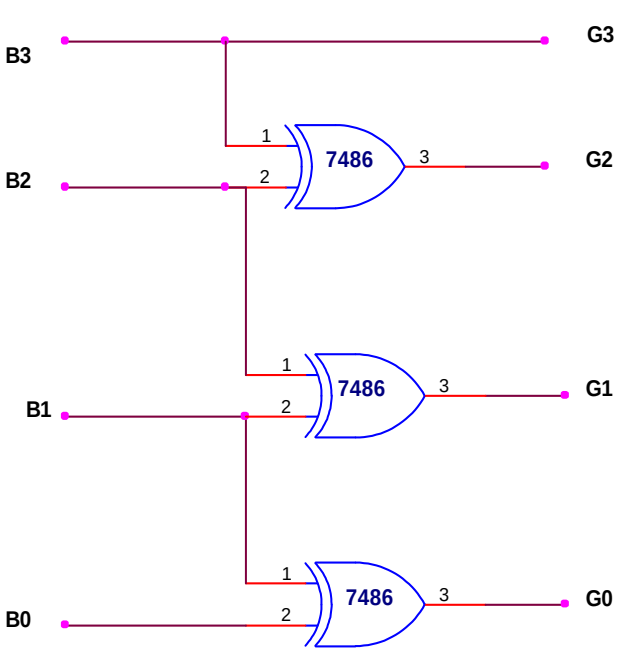
AIM: To design and construct Binary to Gray and Gray to Binary circuits and verify their truth tables.

APPARATUS: 1.Digital circuit designer.

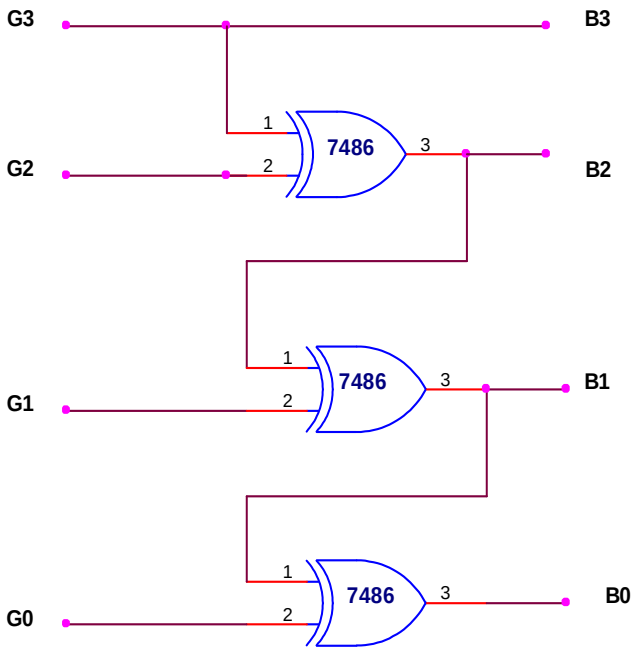
2. IC 7486, 7408,7432,7404,7411

3. Connecting wires.

Binary to Gray Code Converter



Gray to Binary Code Converter



Inputs				Outputs			
B3	B2	B1	B0	G3 (V)	G2 (V)	G1 (V)	G0 (V)
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Procedure: -

1. The circuit connections are made as shown in fig.

2. Pin (14) is connected to +Vcc and Pin (7) to ground.

3. In the case of binary to gray conversion, the inputs B0, B1, B2 and B3 are given at respective pins and outputs G0, G1, G2, G3 are taken for all the 16 combinations of the input.

4. In the case of gray to binary conversion, the inputs G0, G1, G2 and G3 are given at respective pins and outputs B0, B1, B2, and B3 are taken for all the 16 combinations of inputs.

5. The values of the outputs are tabulated.

12 Multiplexer and Demultiplexer.

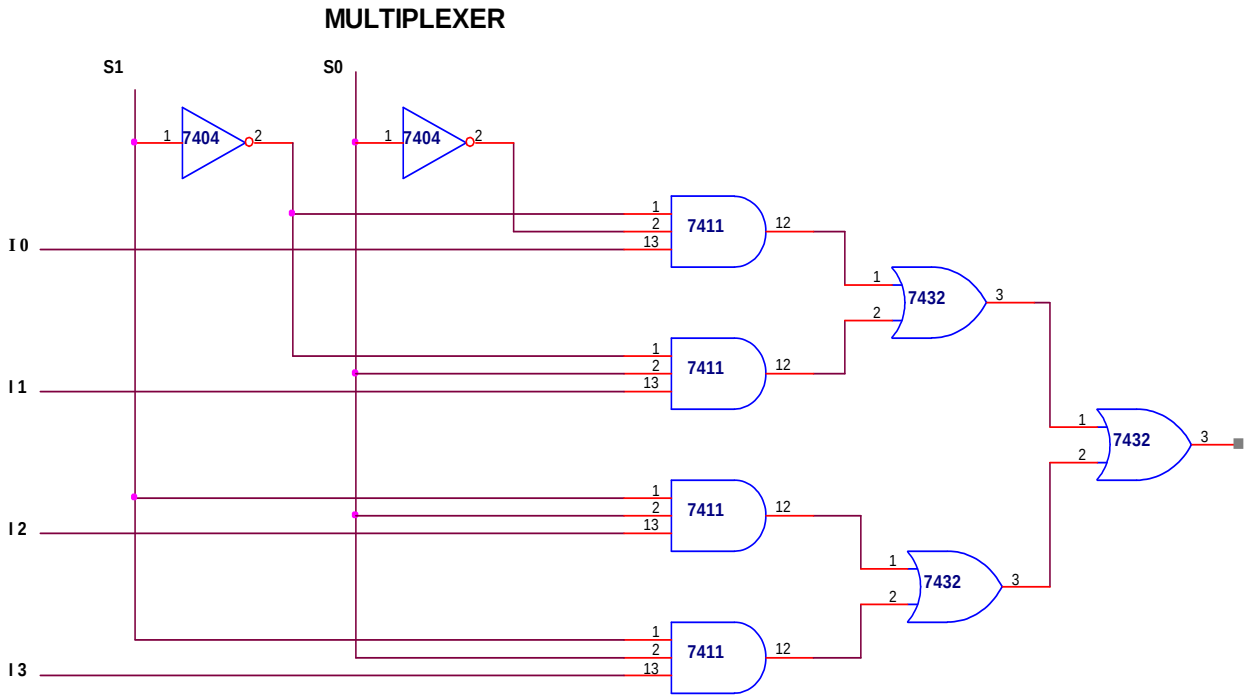
AIM: To design and construct multiplexer and demultiplexer and verify their truth tables.

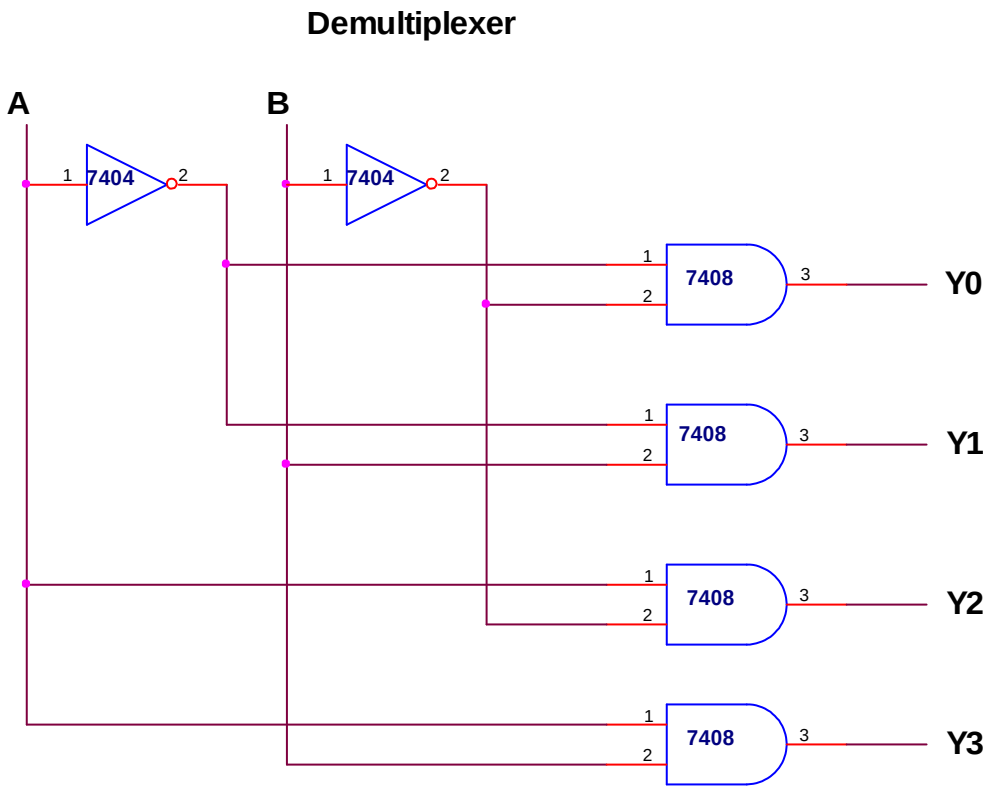
APPARATUS: Digital circuit designer.

IC 7486,7408,7432,7404,7411.

Connecting wires.

CIRCUTE DIAGRAMS:





PROCEDURE:

1. Connect circuit as per the circuit diagram.
2. Apply different combinations of inputs as shown in truth table and observe the outputs.
3. Tabulate the input and outputs.

PRECAUTIONS:

1. All the connections should be properly.

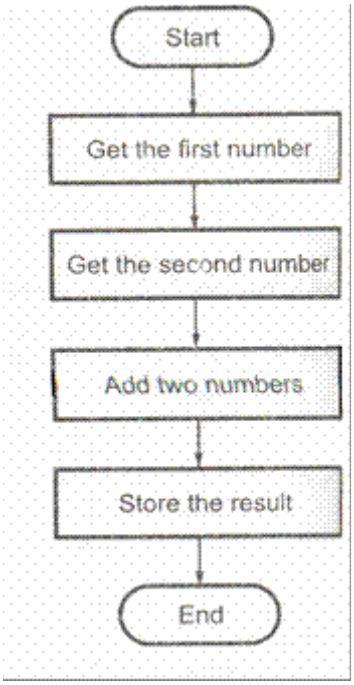
2. IC should not be reverse.

RESULT:

13 ADDITION OF TWO 8 BIT NUMBERS

AIM: To perform addition of two 8 bit numbers using 8085.

FLOW CHART



PROGRAM:

LXI H 4000H	: HL points 4000H
MOV A, M	: Get first operand
INX H	: HL points 4001H
ADD M	: Add second operand
INX H	: HL points 4002H
MOV M, A	: Store result at 4002H
HLT	: Terminate program execution

OBSERVATION:

Input: (4000H) = 14H

(4001H) = 89H

Output: 14H + 89H = 9DH

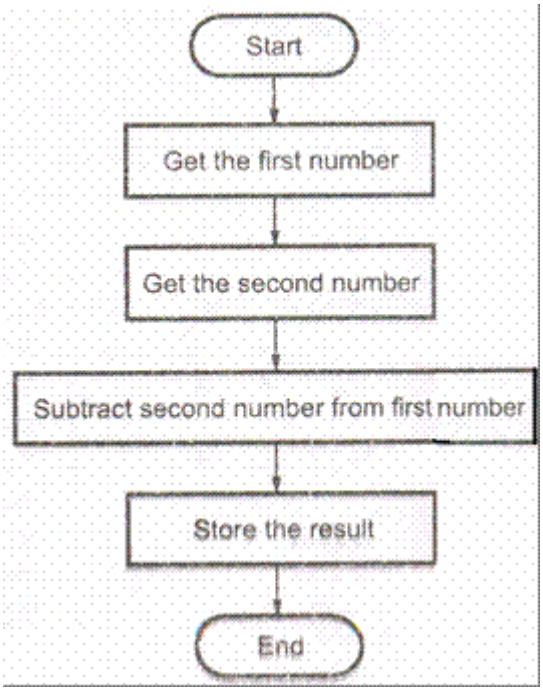
RESULT:

Thus the program to add two 8-bit numbers was executed.

14: SUBTRACTION OF TWO 8 BIT NUMBERS

AIM: To perform the subtraction of two 8 bit numbers using 8085.

FLOW CHART:



.

PROGRAM:

LXI H, 4000H	: HL points 4000H
MOV A, M	: Get first operand
INX H	: HL points 4001H
SUB M	: Subtract second operand
INX H	: HL points 4002H
MOV M, A	: Store result at 4002H.
HLT	: Terminate program execution

OBSERVATION:

Input: (4000H) = 51H

(4001H) = 19H

Output: 51H - 19H = 38H

RESULT:

Thus the program to subtract two 8-bit numbers was executed.

15 Addition of n numbers using 8085 Microprocessor

AIM: To perform the addition of n numbers using 8085 microprocessor.

PROGRAM:

```
MOV BX, offset array
MOV AL,[BX]
LOOP: INC BX
ADD AL,[BX]
INC N
CMP N, 06H
JLE LOOP
HLT
```

OBSERVATION:

Input: 01H,02H,03H,04H,05H,06H

Output: 01H+02H+03H+04H+05H+06H = 15H

RESULT:

Thus the program to add n numbers was executed.