18EE001

Hall Ticket Number:

I/IV B.Tech (Regular/Supplementary) DEGREE EXAMINATION

December, 2018 — **Common for (CSE,IT,MECH)**

First/Second Semester — **Basic Electrical & Electronics Engineering**

Time: Three Hours — **Maximum:** 50 Marks

Answer Question No.1 compulsorily. (1X10 = 10 Marks)

Answer ONE question from each unit. (4X10=50 Marks)

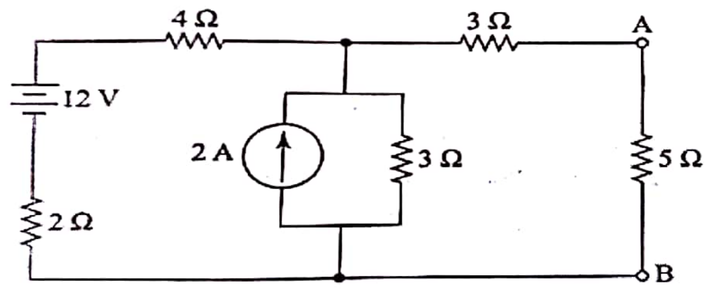
1. Answer all questions (1X10=10 Marks)

   a. Define ohms law
   b. State super position Theorem.
   c. Draw Phasor diagram for RL circuit.
   d. What is transformer?
   e. What is Hysteresis loss.
   f. Define CMRR
   g. Draw the circuit of voltage follower.
   h. What are the regions of operation of a transistor?
   i. Draw the circuit of a simple clamper
   j. Distinguish contact potential and cut-in voltage of a diode.

UNIT I

2.a State Thevenin`s Theorem with neat diagrams and explain them. 5M

2.b Use Thevenin`s theorem to calculate the current flowing through the 5Ω resistor in the circuit shown below 5M



(OR)

3.a A 230V, 50Hz sinusoidal supply is connected across a (i) resistor of 25Ω; (ii)inductance of 0.5H; (iii) capacitance of 100uF. Write the expressions for instantaneous current in each case. 5M

3.b Define the following 5M

a) Average value b) Form factor c) Active power d) Reactive power e) power factor.

UNIT II

4.a Explain the construction and working principle of a three-phase induction motor. 6M

4.b Draw the equivalent circuit of a practical Transformer and explain the terms in it. 4M

(OR)

5.a Explain different types of losses present in the Transformer. Write the formula for efficiency and regulation of a transformer 6M

5.b What are the different starting methods of a Induction motor 4M

UNIT III

6.a Explain the operation of a diode in both forward and reverse bias conditions. Also write the current-voltage relation — 5M

6.b Draw the circuit of Full wave rectifier without filter and find its ripple factor. — 5M

(OR)

7.a Which of the transistor currents is always the largest? Which is always the smallest? Which two currents are relatively close in magnitude? Also give explanation for each answer. — 5M

7.b For a transistor, given an α of 0.998, determine I_C if $I_E = 4mA$. — 5M

UNIT IV

8.a Draw the basic construction of a p-channel JFET. Apply the proper biasing between drain and source and sketch the region for $V_{GS} = 0V$. — 5M

8.b Explain in your own words why the application of a positive voltage to the gate of an n-channel depletion type MOSFET will result in a drain current exceeding I_{DSS}. Show necessary diagrams — 5M

(OR)

9.a Calculate the CMRR (in dB) for the circuit measurements of $V_d = 1$ mV, $V_0 = 120$ mV, and — 5M

$V_c = 1mV$, $V_0 = 20\ \mu V$.

9.b Explain the operation of the following circuits built using op-amp — 5M

(i) Inverting amplifier (ii) Integrator

I/IV B.Tech (Regular/supply) Degree Examination

Dec, 2018

Information Technology

first semester.

Basic Electrical & Electronics Engineering

1. Answer all Questions.

a) Ohms law :- Voltage between two terminals of a current carrying conductor is directly praportional to the current flowing through it.

This relation will hold good provided the temperature do not change.

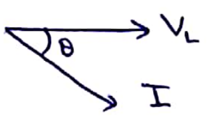
b) Superposition theorem:-

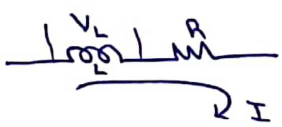
The superposition theorem states that in a linear network containing more than one source, the current flowing in any branch is algebraic sum of currents that would have been produced by each source taken seperately with all the other sources replaced by their respective internal resistances.

i.e., Voltage source ⟶ short circuit.

current source ⟶ open circuit.

c) Phasor diagram of RL circuit





I lags V by an angle ϕ

$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right)$

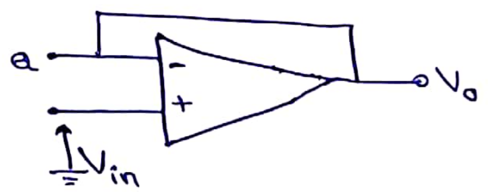
d] **Transformer :-** It is a device which can stepup or step down AC voltage without change in its frequency and power.

e] **Hysterisis loss :-** When alternating voltage is applied to the primary windings of T/F, the core gets magnetized. The magnetization of core takes place in alternate directions every half cycle. Magnetization in alternating direction means magnetic dipoles changes their orientation. This gives rise to loss of energy which is expressed as $W_h = \eta B_m^{1.6} f V$;

f) CMRR stands for Common mode rejection ratio and it is defined as the ratio of differential voltage gain to common mode voltage gain

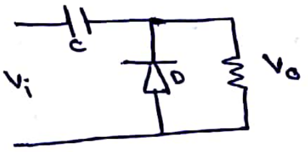
CMRR = A_d / A_c ; A_d : differential voltage gain.
A_c : Common mode voltage gain.

g) **Voltage follower**

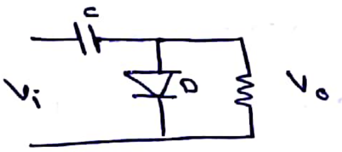


h) The regions of operation of a transistor are
1. Cutoff region
2. active region
3. Saturation region.

i] Positive clamper



Negative clamper



j] Contact Potential is the Voltage applied at the terminals of the device (diode)

Cut in Voltage of a diode is the voltage formed at the barriers. i.e., Junction of the pn layers.

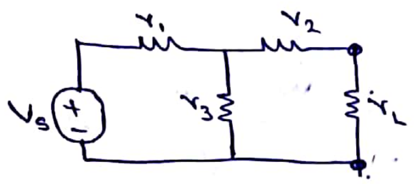
Unit I

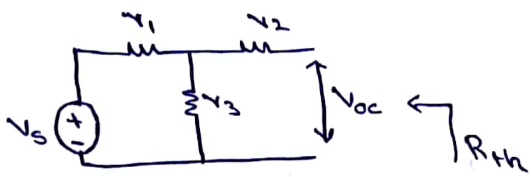
2a] <u>Thevenin's theorem statement</u>

Any two terminals bilateral linear dc circuits can be replaced by an equivalent circuit consisting of a voltage source in series with a resistance.

The series resistance (Thevenin resistance) is obtained by removing voltage source as short circuit and current source as open circuit and calculate Req wrt target element terminals. 2M

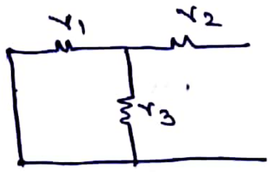
Simple dc circuit





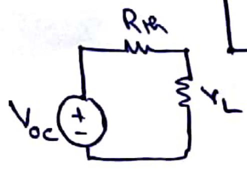
3M

$$V_{oc} = \frac{V_s r_3}{r_1 + r_3}$$



$$R_{th} = r_2 + \frac{r_1 r_3}{r_1 + r_3};$$

final circuit is



Steps

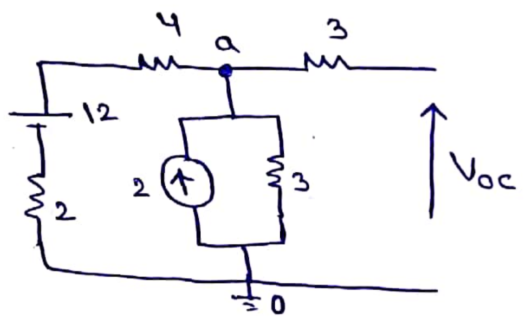
1. Remove the load resistor (R_L) and find the open circuit voltage V_{oc}, across the open circuited terminals of load.

2. Deactive the sources by their internal ideal resistances & cort target elements calculate equivalent resistance.

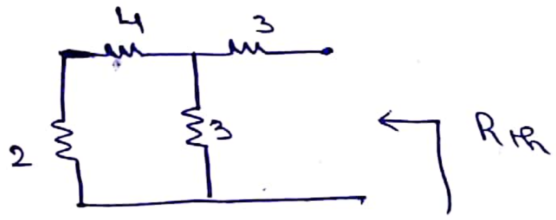
3. Obtain thevenin's equivalent circuit by placing R_{th} in series with V_{oc}

4. Reconnect R_L across the load terminals.

b]



$V_{oc} = V_{ao}$



nodal analysis at a

$$\frac{V_a - 12}{6} - 2 + \frac{V_a}{3} = 0$$

$$V_a\left(\frac{1}{6} + \frac{1}{3}\right) = 2 + 2$$

$$V_a = \frac{4 \times 6}{3} = 8V$$

$$V_{oc} = 8V$$

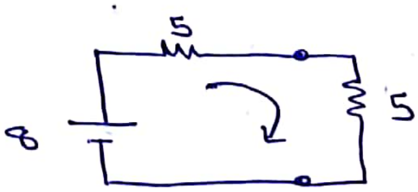
2M

$3 + 3 // 6$

$3 + \frac{3 \times 6}{9} = 5$

$R_{th} = 5\Omega$

2M



$I_{5\Omega} = \frac{8}{10} = 0.8A$

1M

3a] 230V, 50HZ Sinusoid supply

$V = 230V$

$V_m = 230\sqrt{2} = 324.3V$ $\therefore v_s = V_m \sin\omega t$

$\omega = 2\pi f = 314 r/s$ $= 324.3 \sin 314t$

Inductive reactance $X_L = \omega L = 314 \times 0.5 = 157 \Omega$

Capacitive reactance $X_C = \frac{1}{\omega C} = \frac{1}{314 \times 100 \times 10^{-6}}$

$= 32.2 \Omega$

When Voltage is applied across 25Ω, the Current will be $i = \frac{V_m}{R} \sin\omega t = 12.97 \sin 314t$ 1M

Current through inductor is $i = \frac{V_m}{X_L} \sin(\omega t - \pi/2)$

$i = \frac{324.3}{157} \sin(314t - \pi/2)$

$i = 2.06 \sin(314t - 90)$ A 2M

Current through the Capacitor is

$i = \frac{V_m}{X_C} \sin(\omega t + \pi/2)$

$i = \frac{324.3}{32.2} \sin(314t + \pi/2)$

$i = 10.07 \sin(314t + 90)$ A 2M

3b] 1M each

a] Average Value :- Average Value of a sinusoidally varying Quantity over one cycle is zero because for first half cycle current is in +ve cycle and in second half cycle current is in -ve half cycle. So avg. value can be calculated for one half cycle as

$$I_{av} = \frac{1}{\pi}\int_0^{\pi} I_m \sin\theta \, d\theta = 2I_m/\pi = 0.637 I_m$$

b] form factor :- It is the ratio of RMS value to the average value of alternating Quantity. $ff = \frac{RMS}{avg} = 1.11$.

c] Active Power :- It is the power which is actually dissipated in circuit resistant

$P = VI\cos\phi$ watts or Kwatts.

d] Reactive Power :- It is the power developed in the inductive reactance of circuit

$Q = I^2 X_L = VI\sin\phi$ VAR

e] PowerFactor :- It is defined as cosine of angle between Voltage and Current. $\cos\phi$; ratio of resistance to impedance R/Z; for pure sine waves.

It is also defined as ratio of active power to apparent power

$$P.F = \frac{\text{active power}}{\text{apparent power}} = P/S$$

Unit - II

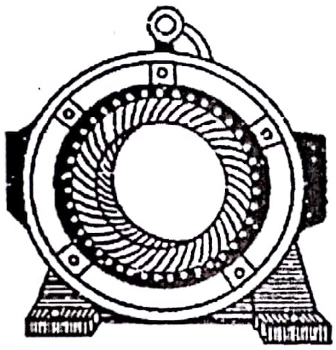
4a]

Construction

A 3-phase induction motor has two main parts (i) stator and (ii) rotor. The rotor is separated from the stator by a small air-gap which ranges from 0.4 mm to 4mm, depending on the power of the motor.

1. Stator

It consists of a steel frame which encloses a hollow, cylindrical core made up of thin laminations of silicon steel to reduce hysteresis and eddy current losses. A number of evenly spaced slots are provided on the inner periphery of the laminations. The insulated connected to form a balanced 3-phase star or delta connected circuit. The 3-phase stator winding is wound for a definite number of poles as per requirement of speed. Greater the number of poles, lesser is the speed of the motor and vice-versa. When 3-phase supply is given to the stator winding, a rotating magnetic field (See Sec. 8.3) of constant magnitude is produced. This rotating field induces currents in the rotor by electromagnetic induction. 2M



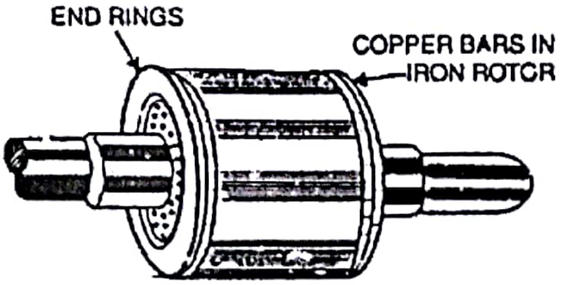
2. Rotor

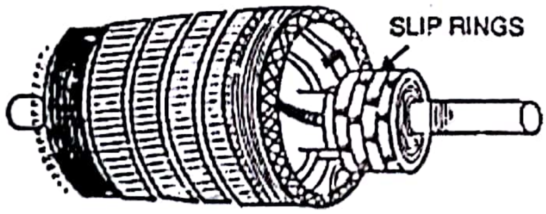
The rotor, mounted on a shaft, is a hollow laminated core having slots on its outer periphery. The winding placed in these slots (called rotor winding) may be one of the following two types:

(i) Squirrel cage type (ii) Wound type

(i) **Squirrel cage rotor**. It consists of a laminated cylindrical core having parallel slots on its outer periphery. One copper or aluminum bar is placed in each slot. All these bars are joined at each end by metal rings called end rings [See Fig. (8.2)]. This forms a permanently short-circuited winding which is indestructible. The entire construction (bars and end rings) resembles a squirrel cage and hence the name. The rotor is not connected electrically to the supply but has current induced in it by transformer action from the stator. Those induction motors which employ squirrel cage rotor are called squirrel cage induction motors. Most of 3-phase induction motors use squirrel cage rotor as it has a remarkably simple and robust construction enabling it to operate in the most adverse circumstances. However, it suffers from the disadvantage of a low starting torque. It is because the rotor bars are permanently short-circuited and it is not possible to add any external resistance to the rotor circuit to have a large starting torque. 2M

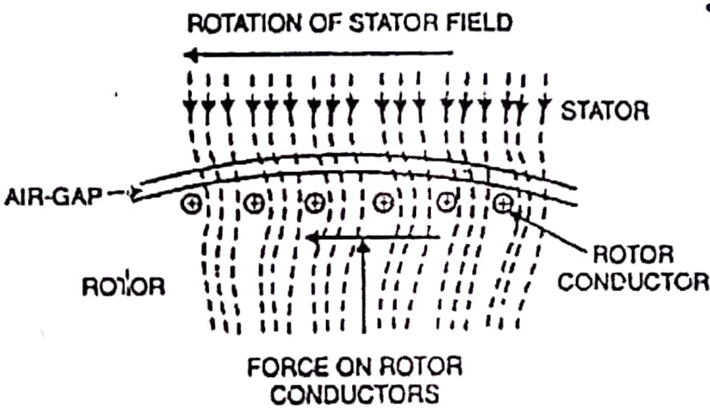
(ii) **Wound rotor**. It consists of a laminated cylindrical core and carries a 3- phase winding, similar to the one on the stator [See Fig. (8.3)]. The rotor winding is uniformly distributed in the slots and is usually star-connected. The open ends of the rotor winding are brought out and joined to three insulated slip rings mounted on the rotor shaft with one brush resting on each slip ring. The three brushes are connected to a 3-phase star-connected rheostat as shown in Fig. (8.4). At starting, the external resistances are included in the rotor circuit to give a large starting torque. These resistances are gradually reduced to zero as the motor runs up to speed. The external resistances are used during starting period only. When the motor attains normal speed, the three brushes are short-circuited so that the wound rotor runs like a squirrel cage rotor.





Principle of Operation

Consider a portion of 3-phase induction motor as shown in Fig. The operation of the motor can be explained as under:



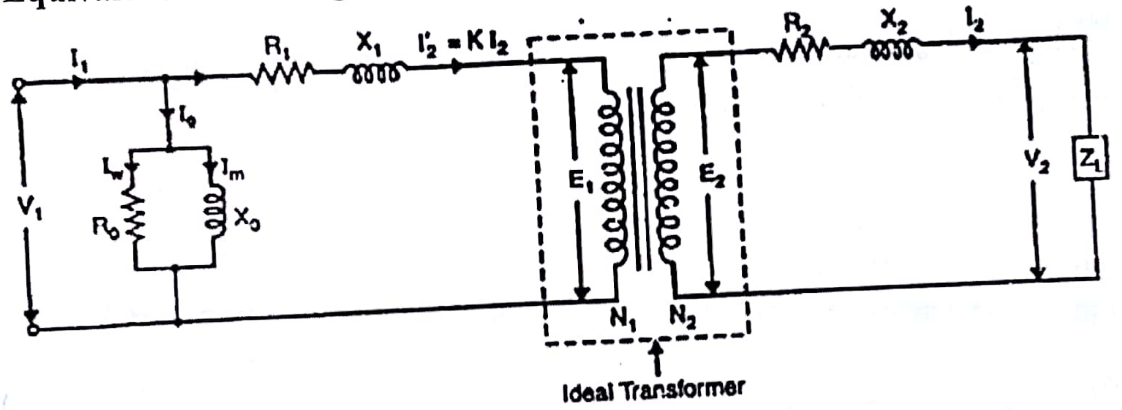
(i) When 3-phase stator winding is energized from a 3-phase supply, a rotating magnetic field is set up which rotates round the stator at synchronous speed N_s (= 120 f/P).

(ii) The rotating field passes through the air gap and cuts the rotor conductors, which as yet, are stationary. Due to the relative speed between the rotating flux and the stationary rotor, e.m.f.s are induced in the rotor conductors. Since the rotor circuit is short-circuited, currents start flowing in the rotor conductors.

(iii) The current-carrying rotor conductors are placed in the magnetic field produced by the stator. Consequently, mechanical force acts on the rotor conductors. The sum of the mechanical forces on all the rotor conductors produces a torque which tends to move the rotor in the same direction as the rotating field.

(iv) The fact that rotor is urged to follow the stator field (i.e., rotor moves in the direction of stator field) can be explained by Lenz's law. According to this law, the direction of rotor currents will be such that they tend to oppose the cause producing them. Now, the cause producing the rotor currents is the relative speed between the rotating field and the stationary rotor conductors. Hence to reduce this relative speed, the rotor starts running in the same direction as that of stator field and tries to catch it.

4b] **Equivalent circuit diagram of a Practical transformer**



(i) A resistance R_1 in the primary becomes $K^2 R_1$ when transferred to the secondary.

(ii) A resistance R_2 in the secondary becomes R_2/K^2 when transferred to the primary.

(iii) A reactance X_1 in the primary becomes $K^2 X_1$ when transferred to the secondary.

(iv) A reactance X_2 in the secondary becomes X_2/K^2 when transferred to the primary.

(v) A resistance R_0 to represent the core losses in a transformer.

(vi) A reactance X_0 to represent the Magnetizing component of the transformer.

5a]

Losses in a Transformer

The power losses in a transformer are of two types, namely;

1. Core or Iron losses 2. Copper losses

These losses appear in the form of heat and produce (i) an increase in temperature and (ii) a drop in efficiency.

1. Core or Iron losses (P_i)

These consist of hysteresis and eddy current losses and occur in the transformer core due to the alternating flux. These can be determined by open-circuit test.

Hysteresis loss, $= k_h f B_m^{1.6}\, watts/m^3$

Eddy current loss $= k_e f^2 B_m^2 t^2\, watts/m^3$

Both hysteresis and eddy current losses depend upon (i) maximum flux density B_m in the core and (ii) supply frequency f. Since transformers are connected to constant-frequency, constant voltage supply, both f and B_m are constant. Hence, core or iron losses are practically the same at all loads.

Iron or Core losses, P_i = Hysteresis loss + Eddy current loss = Constant losses

The hysteresis loss can be minimized by using steel of high silicon content whereas eddy current loss can be reduced by using core of thin laminations.

2. Copper losses

These losses occur in both the primary and secondary windings due to their ohmic resistance. These can be determined by short-circuit test.

Total Cu losses, $P_c = I_1^2 R_1 + I_2^2 R_2$

It is clear that copper losses vary as the square of load current Thus if copper losses are 400 W at a load current of 10 A, then they will be (1/2)2 × 400 = 100W at a load current of 5A.

Total losses in a transformer = P_1 + Pc= Constant losses + Variable losses

It may be noted that in a transformer, copper losses account for about 90% of the total losses.

Transformer Efficiency

$$\text{Transformer } \eta = \frac{V_2 I_2 \cos\phi_2}{V_2 I_2 \cos\phi_2 + P_i + I_2^2 R_{02}}$$

Transformer Voltage Regulation $V.R = \frac{E_2 - V_2}{E_2}$.

Methods of Starting 3-Phase Induction Motors

The method to be employed in starting a given induction motor depends upon the size of the motor and the type of the motor. The common methods used to start induction motors are:

(i) Direct-on-line starting
(ii) Stator resistance starting
(iii) Autotransformer starting
(iv) Star-delta starting
(v) Rotor resistance starting

Methods (i) to (iv) are applicable to both squirrel-cage and slip ring motors. However, method (v) is applicable only to slip ring motors. In practice, any one of the first four methods is used for starting squirrel cage motors, depending upon, the size of the motor. But slip ring motors are invariably started by rotor resistance starting

UNIT III

1.2 WORKING OF PN JUNCTION DIODE

The working of a *pn* junction diode can be explained under two different heads

(a) Forward Bias
(b) Reverse Bias

1.2.1 FORWARD BIASED P-N JUNCTION DIODE

When external voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow, it is called forward biasing.

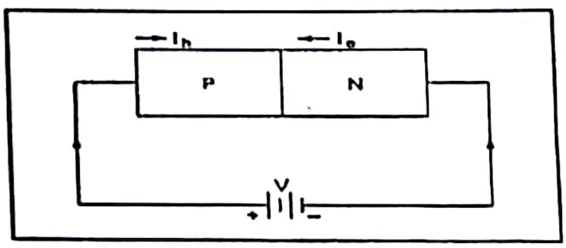


FIGURE 1.3 : Forward Biased p-n Juntion

Suppose positive battery terminal is connected to *p*-region of a semi-conductor and the negative battery terminal to the *n*-region as shown in Fig. 1.3 is called forward bias. Forward bias permits easy flow of current across the junction. The current flow may be explained as the following ways.

1. As soon as battery connections are made, holes are repelled by the positive battery terminal and electrons are repelled by the negative battery terminal with the result that both the elections and the holes are driven towards the junction. This movement of electrons and holes constitutes a large current flow through the semiconductor. The diode offers low resistance in forward direction.
2. The applied forward voltage reduced the height of potential barrier at the junction. It allows more carriers cross the junction, more current to flow across the junction. Forward bias reduced the thickness of depletion layer.

1.2.2 REVERSE BIASED P-N JUNCTION DIODE

When the external voltage applied to the junction is in such a direction that potential barrier is increased, it is called reverse biasing.

Suppose a negative terminal of the battery is connected to *p*-region of the diode and the positive battery terminal the *n*-region as shown in Fig. 1.4. is called reveres bias. In this case holes are attracted by the negative battery terminal and electrons by the positive terminal so that both holes and electrons move away from the junction. Since there is no current flows and the junction offers high resistance. The applied reverse voltage V increases the potential barrier thereby blocking the flow of majority carriers. The reverse bias increase the thickness of depletion layer.

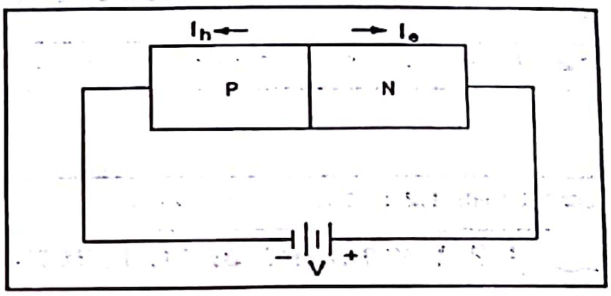


FIGURE 1.4 : Reverse Biased p-n Junction

Although under reveres bias condition, there is practically no current due to majority carriers, yet there is a small amount of current due to flow of minority carriers. This current is called reverse saturation current I_o. Since minority carriers are thermally generated I_o is extremely temperature dependent. I_o is found to double for every 10° C rise in germanium and for every 6°C rise in silicon. I_o is in order of μA for germanium and nA for silicon.

If reverse voltage is increased continuously the kinetic energy of minority electrons may become high enough to knockout electrons from the semiconductor atom. At this stage breakdown of the junction occurs, characterized by a sudden rise of reveres current and a sudden fall of the resistance of barrier region. This may destroy the junction permanently.

The relation between voltage and current is given by

$$I = I_o \left(e^{V/\eta V_T} - 1\right)$$

Where V_T = Volt equivalent to temperature = $\dfrac{T(k)}{11{,}600}$

I_o = reverse saturation current

V = applied voltage

η = 1 for germanium 2 for silicon.

6b) **Full wave rectifier circuit diagram :**

any diagram 3M

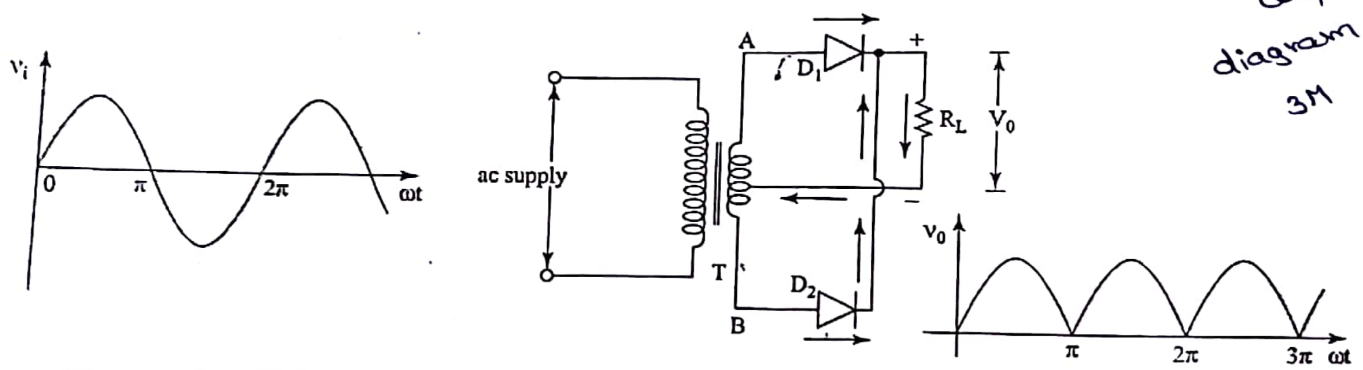


Figure 15.5 *Full-wave rectifier using two diodes and a centre-tapped transformer*

as

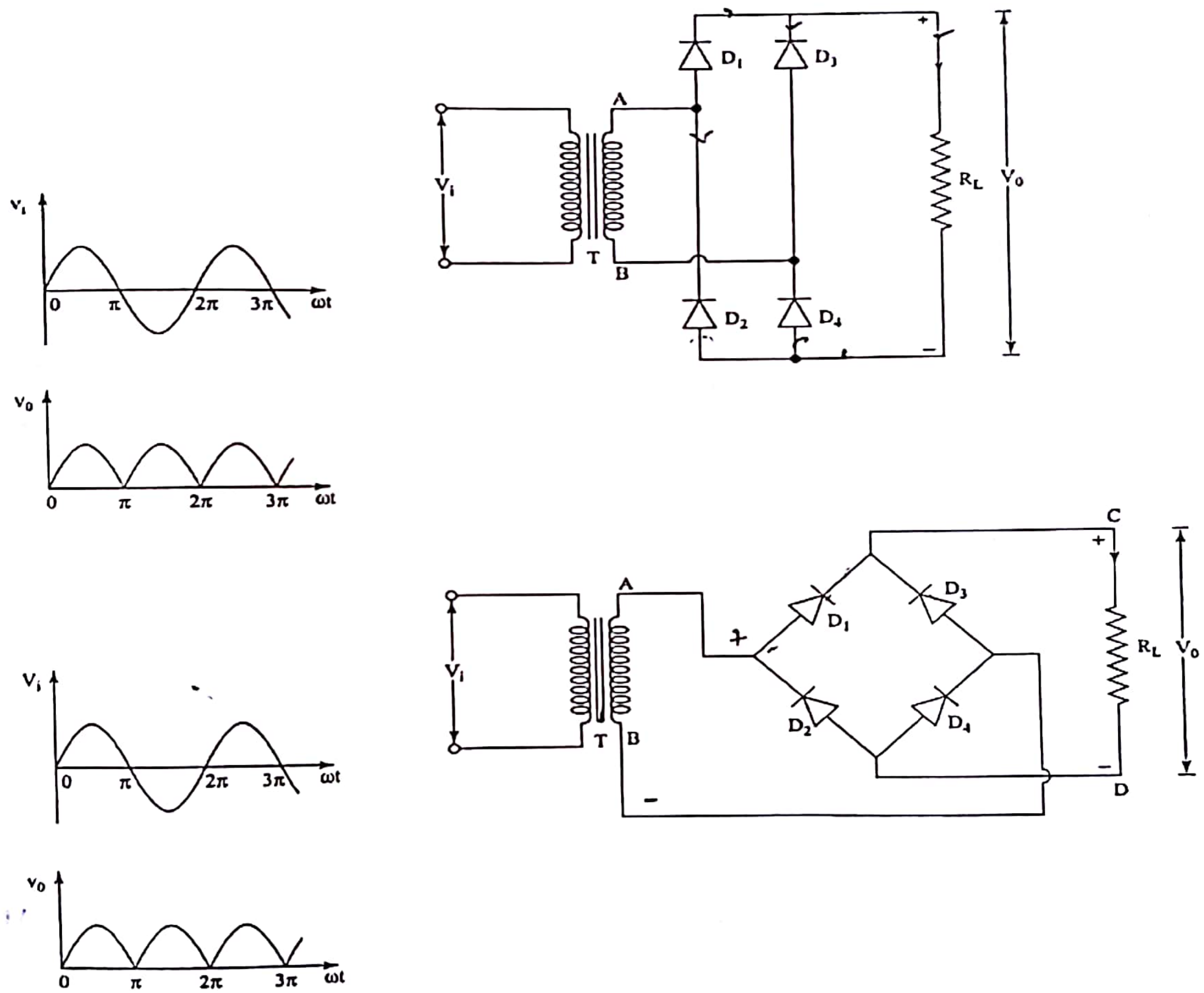


Figure 15.6 *A bridge rectifier circuit for full-wave rectification using four diodes and a transformer*

Ripple Factor

$$\text{Ripple factor, } r = \frac{\text{RMS value of ac component}}{\text{dc component}}$$

$$= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$ 2M

Substituting, $I_{rms} = \frac{I_m}{\sqrt{2}} =$ and $I_{dc} = \frac{2I_m}{\pi}$

$$r = \sqrt{\left(\frac{I_m \pi}{\sqrt{2}\, 2\, I_m}\right)^2 - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1}$$

$$= 0.48$$

7a) The emitter current I_E is the largest current. 3M

The Base Current I_B is the smallest current.

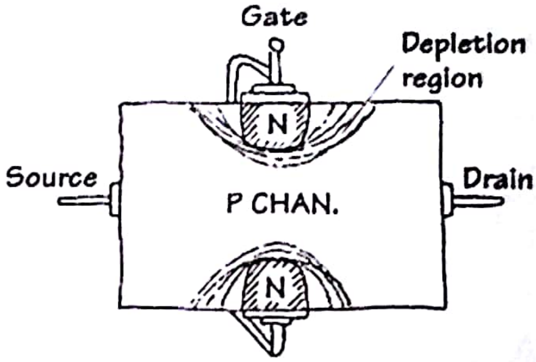
The collector current I_C is approximately equal to the emmitter current I_E $I_C = \alpha I_E$ $\alpha < 1.0$;

- The ratio $I_C / I_B = \beta$ is large, hence I_C is greater than I_B. 2M

7b) Given $\alpha = 0.998$, $I_E = 4mA$ 5M

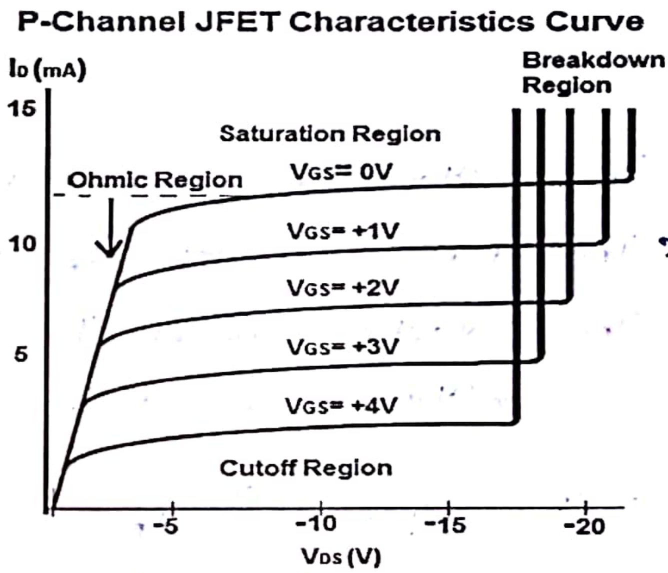
$I_C = \alpha I_E = 0.998 * 4m = 3.992mA$.

8a) A P-Channel JFET is composed of a gate, a source and a drain terminal.

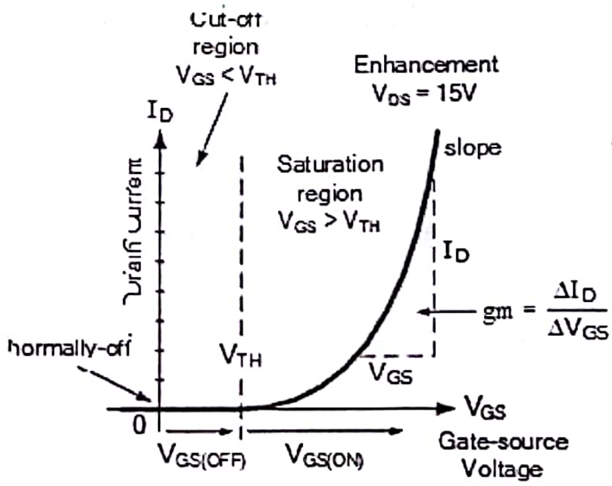


It is made with an p-type silicon channel that contains 2 n-type silicon terminals placed on either side. The gate lead is connected to the N-type terminals, while the drain and source leads are connected to either ends of the P-type channel.

When no voltage is applied to the gate of a P-Channel JFET, current (holes) flows freely through the central P-channel. This is why JFETs are referred to as "normally on" devices. Even without any voltage, they conduct current across from source to drain.



8b) Depletion mode MOSFETS are also available in which the gate extends the full width of the channel (from source to drain). In this case it is also possible to operate the transistor in enhancement mode. This is done by making the gate positive instead of negative. The positive voltage on the gate attracts more free electrons into the conducing channel, while at the same time repelling holes down into the P type substrate. The more positive the gate potential, the deeper, and lower resistance is the channel. Increasing positive bias therefore increases current flow. This useful depletion/enhancement version has the disadvantage that, as the gate area is increased, the gate capacitance is also larger than true depletion types. This can present difficulties at higher frequencies.



9b)

(i) ***The Inverting Amplifier***

2M

One of the more popular circuit configurations of the op-amp, because of its simplicity, is the so-called inverting amplifier, shown in Figure 12.5. The input signal be amplified is connected to the inverting terminal, while the noninverting terminalis grounded. It will now be shown how it is possible to choose an (almost) arbitrary gain for this amplifier by selecting the ratio of two resistors. The analysis is begun by noting that at the inverting input node, KCL requires that

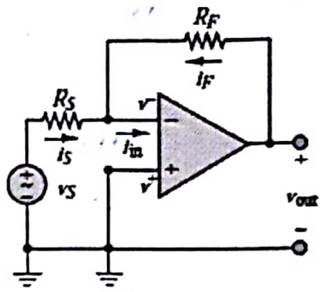


Figure 12.5 Inverting amplifier

$$i_S + i_F = i_{in}$$

The current i_F, which flows back to the inverting terminal from the output, is appropriately termed **feedback current,** because it represents an input to the amplifier that is "fed back" from the output. Applying Ohm's law, we may determine each of the three currents.

$$v_{out} = -\frac{R_F}{R_S} v_S \quad \text{Inverting amplifier closed-loop gain}$$

(ii) **The Ideal Integrator**

Consider the circuit of Figure 12.30, where $v_S(t)$ is an arbitrary function of time (e.g., a pulse train, a triangular wave, or a square wave). The op-amp circuit shown provides an output that is proportional to the integral of $v_S(t)$. The analysis of the integrator circuit is, as always, based on the observation that

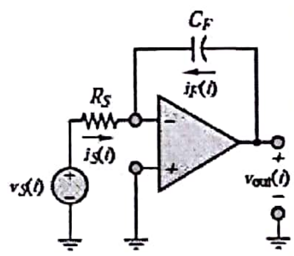


Figure 12.30 Op-amp integrator

$$i_S(t) = -i_F(t) \tag{12.63}$$

where

$$i_S(t) = \frac{v_S(t)}{R_S} \tag{12.64}$$

It is also known that

$$i_F(t) = C_F \frac{dv_{out}(t)}{dt} \tag{12.65}$$

from the fundamental definition of the capacitor. The source voltage can then be expressed as a function of the derivative of the output voltage:

3M

$$\frac{1}{R_S C_F} v_S(t) = -\frac{dv_{out}(t)}{dt} \tag{12.66}$$

By integrating both sides of equation 12.66, we obtain the following result:

$$v_{out}(t) = -\frac{1}{R_S C_F} \int_{-\infty}^{t} v_S(t')\,dt' \tag{12.67}$$

This equation states that the output voltage is the integral of the input voltage.

There are numerous applications of the op-amp integrator, most notably the analog computer, which will be discussed in Section 12.5. The following example illustrates the operation of the op-amp integrator.

9 a) CMRR in dB = $20\log_{10} A_d/A_c$

$A_d = \frac{V_o}{V_d} = \frac{120}{1m}$ 2M

$A_c = \frac{V_o}{V_c} = 20\mu/1m$ 2M

$\frac{A_d}{A_c} = \frac{120}{1m} \times \frac{1m}{20\mu} = 6M$

1M

CMRR = $20\log_{10}(6M) = 135.56 dB$.

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