# III/IV B.Tech (Regular) DEGREE EXAMINATION

Month & year: November, 2019

Semester: Fifth Semester

Subject code: 14EC501

Subject Name: Linear Integrated circuits & Applications

**SCHEME of EVALUATION**
**&**
**Answers**

**Prepared by**


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**14EC/EI 501**
**EC/EE/EI 311**

**Hall Ticket Number:**

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**III/IV B.Tech(Regular/Supplementary) DEGREE EXAMINATION**

**November, 2019**

**Fifth Semester**

**Common to ECE, EEE & EIE**

**Linear Integrated Circuits & Applications**

**Time:** Three Hours

**Maximum :** 60 Marks

*Answer Question No.1 compulsorily.* (1X12 = 12 Marks)

*Answer ONE question from each unit.* (4X12 = 48 Marks)

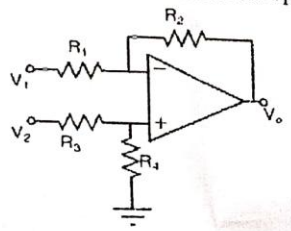
**1.** Answer all questions (1X12 = 12 Marks)

a. If the CMRR for a differential amplifier is 70dB and the differential gain is 50. What is the Ac.
b. What are the techniques to improve the frequency response of Op-Amps.
c. Sketch the transfer characteristics of differential amplifier.
d. What is a quadrature oscillator?
e. Give the expression for frequency of oscillations of the Triangular waveform generator?
f. Draw the pin diagram of Voltage Controlled Oscillator?
g. What are the disadvantages of weighted resistor DAC?
h. Give the working principle of S/H circuit?
i. What factors decide the speed of conversion of an ADC?
j. What is the use of control pin in IC 555?
k. Define Capture range and Lock range of PLL?
l. Differentiate between the narrow band pass and wide band pass filters?

**UNIT I**

2.a Explain the following op-amp parameters: (i) Input Offset voltage (ii) Output offset voltage (iii) CMRR and (iv) PSRR 6M

2.b If the differential input ($V_d$) and common mode input (Vcm) to the circuit below is 10mv and 0.5mv respectively, find the output voltage $V_o$ , Differential gain $A_d$ and Common mode gain (Acm). Given $R_1 = R_3 = 5K\Omega$, $R_2 = R_4 = 10K\Omega$. Assume the op-amp to be ideal. 6M




**(OR)**

3.a What is the importance of instrumentation amplifier? Draw the circuit diagram and derive the output expression for an op-amp Instrumentation amplifier with gain adjustability. 6M

3.b Define Slew Rate and derive an expression for the SR. What are the factors that influence the slew rate? 6M

**UNIT II**

4.a Explain the principle of Wien Bridge oscillator with a circuit diagram and derive the expression for frequency of oscillation. 6M

4.b Discuss how an op-amp is used as a comparator. What are the limitations of the op-amp as a comparator? 6M

**(OR)**

5.a Define VCO. Explain any two applications of VCO. 6M

5.b Explain the principle of RC Phase Shift oscillator with a circuit diagram and derive the expression for frequency of oscillation. 6M

**UNIT III**

6.a What are the drawbacks of flash type A/D converter? With a neat circuit diagram explain the operation of counter type A/D converter. 6M

6.b Explain the concept of R-2R ladder DAC with any two possible combinations. 6M

**(OR)**

7.a Name the circuit that is used to detect the peak value of the non-sinusoidal waveforms. Draw the circuit diagram and explain its operation with neat waveforms. 6M

7.b What is the use of voltage limiter compared to comparator? Draw the circuit of voltage limiters and explain its operation. 6M

**UNIT IV**

8.a Draw the circuit of a Monostable multivibrator using IC555 and explain its operation with necessary analysis. 6M

8.b Describe the functional block diagram of 555 Timer. 6M

**(OR)**

9.a Explain the operating principles of a 565 .PLL with a block diagram. Derive the expression for capture range. 6M

9.b What are the limitations of three terminal-voltage regulators? How current boosting is achieved in a IC723? 6M

1. Answer all Questions (12x1=12M)

2. a) i) Input offset voltage (4x1.5 = 6M)
ii) Output offset voltage
iii) CMRR
iv) PSRR
2. b) Problem (6M)

3. a) Instrumentation Amplifier (Importance-1M, Diagram-1M, Explanation-2M, Derivation-2M)
3. b) Slew Rate (Definition-2M, Causes-2M, Derivation-2M)

4. a) Wein bridge oscillator (Explanation-2M, Diagram-2M, Derivation-2M)
4. b) Comparator (Explanation-4M, Limitations-2M)

5. a) Voltage Controlled oscillator (Definition-1M, Explanation-2M, Application-3M)
5. b) RC Phase Shift Oscillator (Explanation-2M, Diagram-2M, Derivation-2M)

6. a) (Drawback of Flash ADC-1M, Counter Type Diagram-2M, Explanation-3M )
6. b) R-2R ladder (Diagram-2M, Explanation-2M, Any possible Combination-1M)

7. a) Peak detector (Explanation-3M, Diagram-2M, Waveform-1M)
7. b) Voltage Limiter (Definition-1M, Explanation-3M, Diagram-2M)

8. a) Monostable Multivibrator using 555(Working-3M, Circuit Diagramp-3M)
8. b) Functional Diagram of 555 Timer (Diagram-3M, Pin Descryption-3M)

9. a) Phase Locked Loop (Explanation-2M, Diagram-2M, Derivation-2M)
9. b) Limitations of Three terminal voltage regulators
(Limitations-2M, Explanation-2M, Diagram-2M)

**1.** **(12x1=12M)**

**a)** CMRR = 70db

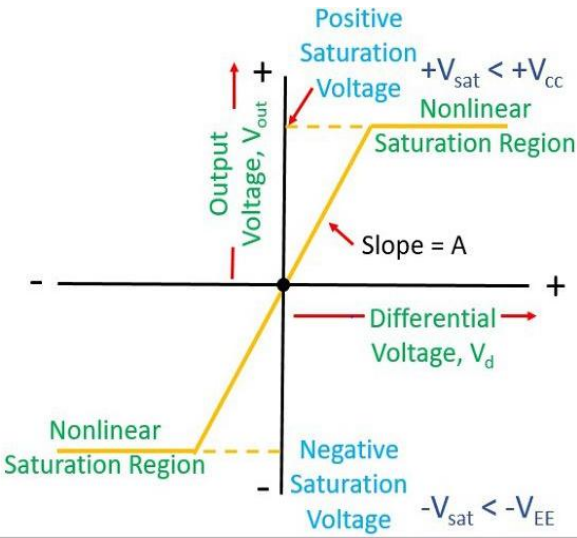
Ad = 50

CMRR = 20 log (Ad/Ac), Ac (db) = 15.82

**b)**

- Dominant pole
- pole zero

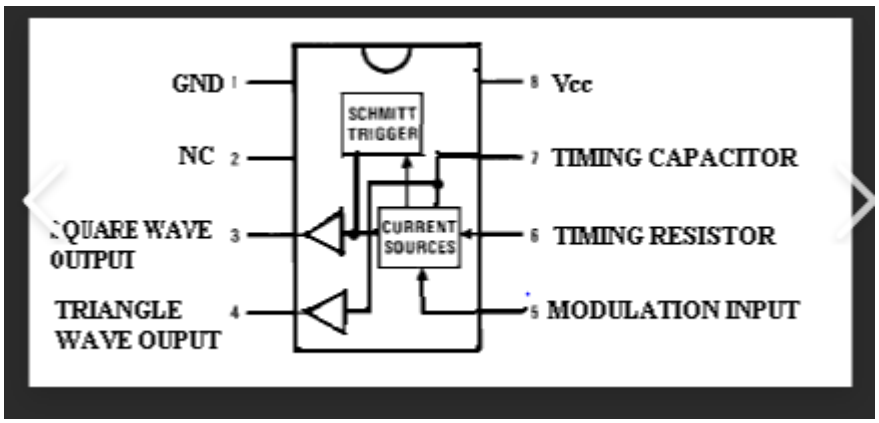
**c)**




**d)** It generates signals that are of same frequency and have a phase shift of 90 degrees with respect to each other.

**e)** $f = R3/4R1C1R2$

**f)**




**g)** More number of registers are required for designing weighted resistor DAC.

**h)** Samples an input signal and holds on to its last sampled value until the input is sampled again.

**i)**

- Conversion time
- Resolution

**j)** Control access to the internal voltage divider (by default, 2/3 $V_{CC}$)

**k) Capture range:**

The range of frequencies over which the PLL can acquire lock

**Lock range:**

The range of frequencies over which the PLL can maintain lock

**l)** For wideband (Q<10)

For Narrowband (Q>10)

**UNIT-I**

**2.a)**

**i) Input Offset voltage** **(4x1.5 = 6M)**

An ideal op-amp amplifies the differential input; if this input difference is 0 volts (i.e. both inputs are at the same voltage), the output should be zero. However, due to manufacturing process, the differential input transistors of real op-amps may not be exactly matched. This causes the output to be zero at a non-zero value of differential input, called the input offset voltage.

**ii) Output offset voltage**

The dc voltage between two output terminals (or the output terminal and ground for circuits with one output) when the input terminals are grounded. (It is due to the inherent mismatch of the input transistors and components during fabrication.)

**iii) CMRR**

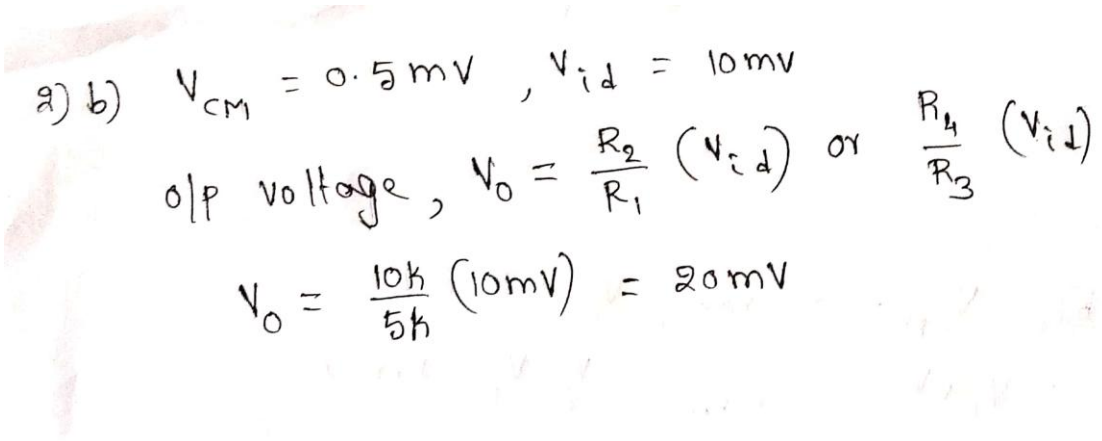
It is the ability of an op amp to reject the common mode signals and amplifies the differential signals.

$$CMRR = Ad/Acm$$

**iv) PSRR**

Power supply rejection ratio (PSRR)is a term widely used to describe the capability of an electronic circuit to suppress any power supply variations to its output signal.

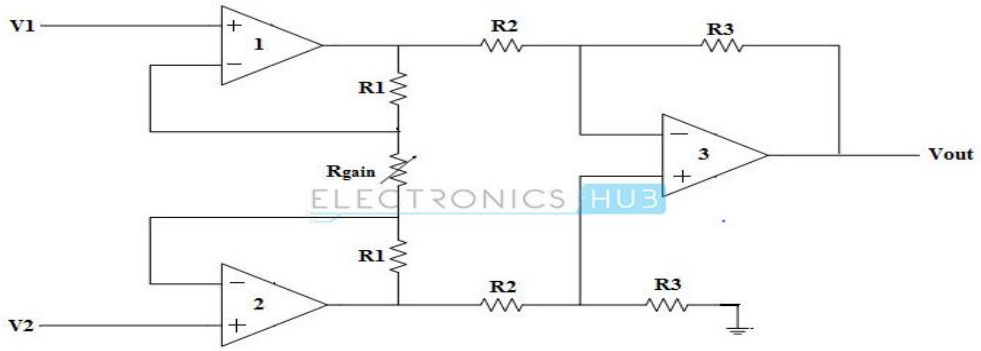
**2. b)** **(6M)**




**3.a) Instrumentation Amplifier:** **(Importance-1M, Diagram-1M, Explanation-2M, Derivation-2M)**

The important features are

- High gain accuracy
- High CMRR
- Low DC offset
- Low output impedance




**The output voltage expression is**

$$Vo = R2/R1\ (1+2(R^1/R))(V1-V2)$$

**3. b) Slew Rate:** **(Definition-2M, Causes-2M, Derivation-2M)**

- It is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/µsec.
- Explanation

**Causes for slew rate:**

There is usually a capacitor within or outside an op-amp to prevent oscillation. It is this capacitor which prevents the output voltage from responding immediately to a fast changing input.

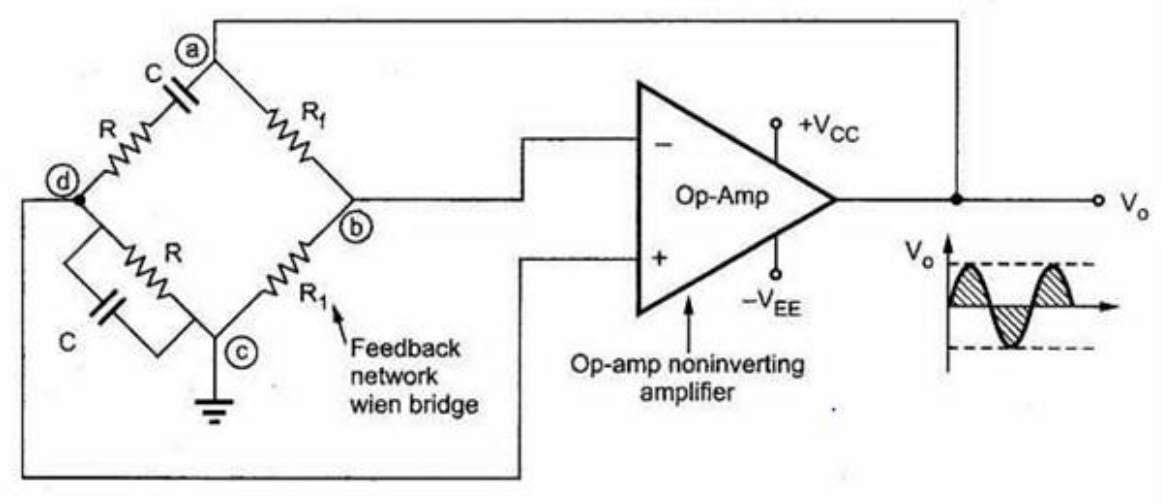
The slew rate can be expressed as

$$SR = dvc/dt/max = I/C = 0.5V/\mu s$$

## UNIT-II

**4. a) Wein bridge oscillator:** **(Explanation-2M, Diagram-2M, Derivation-2M)**

The most commonly used sine wave oscillators for audio frequencies. The frequency of oscillation depends upon RC components.



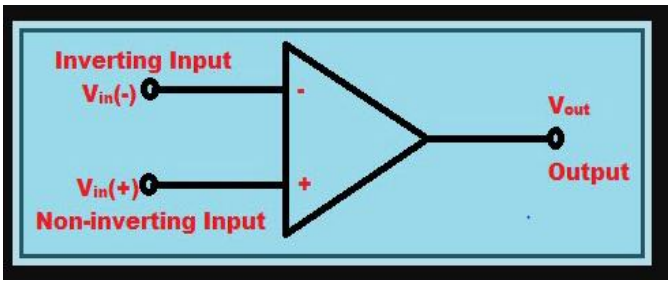
The frequency of oscillation

$f0 = 1/2\pi RC$

$Rf = 2R3$

**4. b) Comparator: (Explanation-4M, Limitations-2M)**

A Comparator is a circuit which compares a signal voltage applied at one input of an op amp with a known reference voltage at the other input. it is basically an open loop op amp with output +/- Vsat.




It can be classified as

- Non inverting Comparator
- Inverting Comparator

**Limitations:**

There are some limitations

- These op amp comparator circuits are typically used in applications where low performance is acceptable.
- Op amps takes more time to recover from saturation, as these are designed to operate in linear mode with negative feedback.
- An external hysteresis is always required for slow moving inputs, op amps doesn't have any internal hysteresis.
- There will be diodes connected back to back between inputs of many op amps, that may cause unpredicted current at inputs.

**5. a) Voltage Controlled oscillator: (Definition-1M, Explanation-2M, Application-3M)**

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage.

The various applications of VCO are:

1. Frequency Modulation.
2. Signal Generation (Triangular or Square Wave)
3. Function Generation.
4. Frequency Shift keying i.e. FSK demodulator.

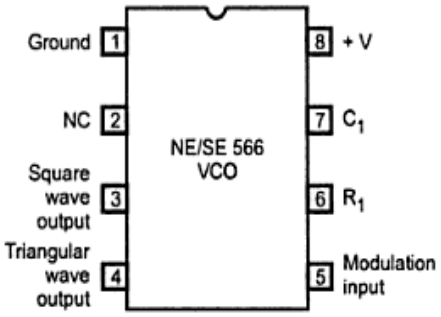



Fig. Pin diagram of IC 566 VCO

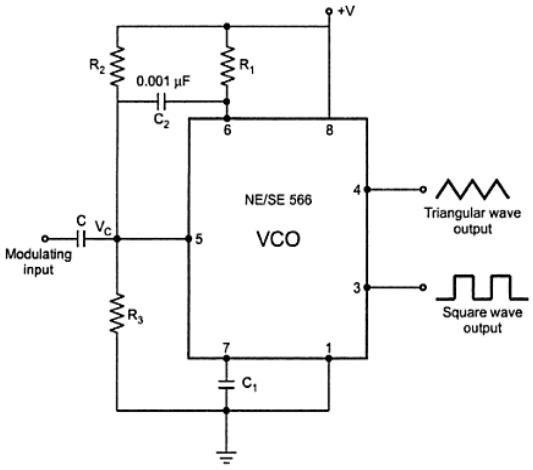


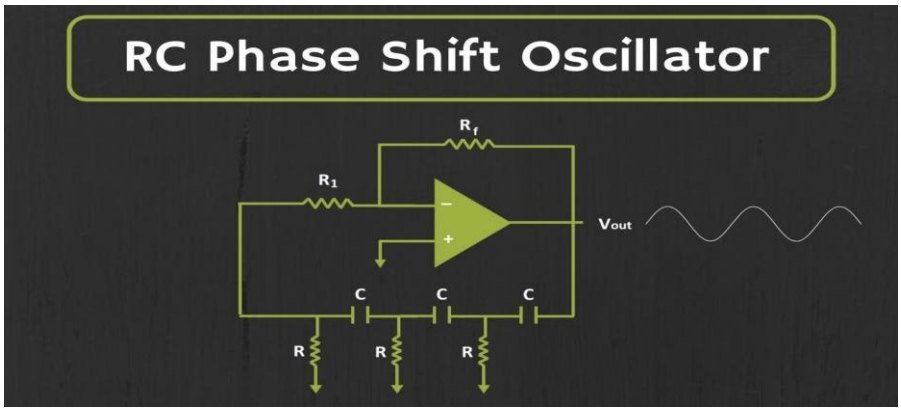

Fig. Typical connection diagram of 566 VCO

## Features of 566 VCO

1. Wide supply voltage range 10 V to 24 V.
2. Very linear modulation characteristics.
3. High temperature stability.
4. Excellent power supply rejection.
5. 10 to 1 frequency range with fixed $C_1$.
6. The frequency can be controlled by means of current, voltage, resistor, or capacitor.

**5. b) RC Phase Shift Oscillator: (Explanation-2M, Diagram-2M, Derivation-2M)**

The op amp is used in the inverting mode and it provides 180 degree phase shift. The additional phase shift of 180 is provided by the RC feedback network to obtain a total phase shift of 360 degrees.




**The frequency of oscillation is**

$$f = 1/2\pi RC\sqrt{6}$$

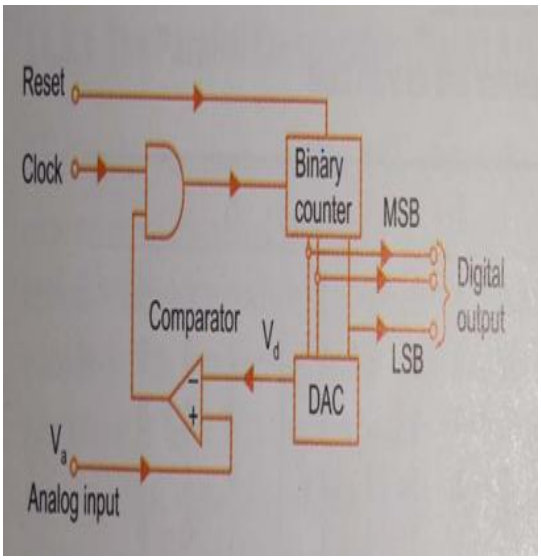
## UNIT-III

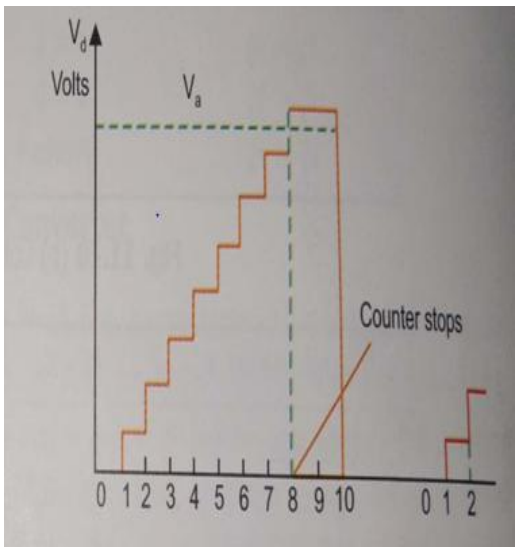
**6. a) Drawbacks of Flash type ADC:**

- The number of comparators are doubled as one bit increases.

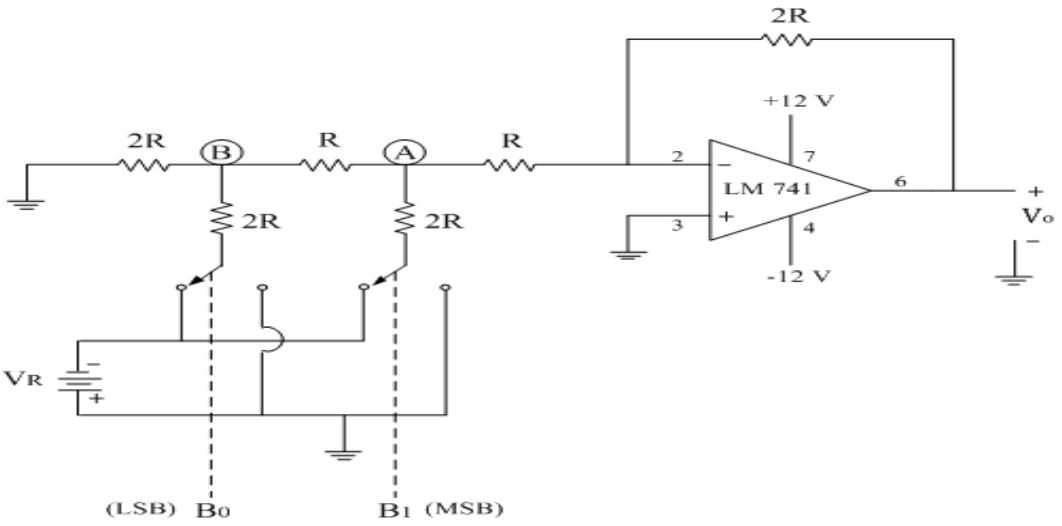
**(Drawback of Flash ADC-1M, Counter Type Diagram-2M, Explanation-3M )**

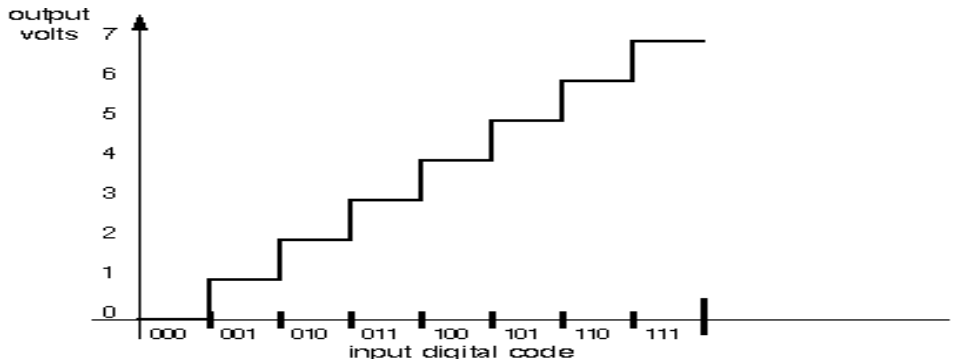
**Counter Type ADC:**



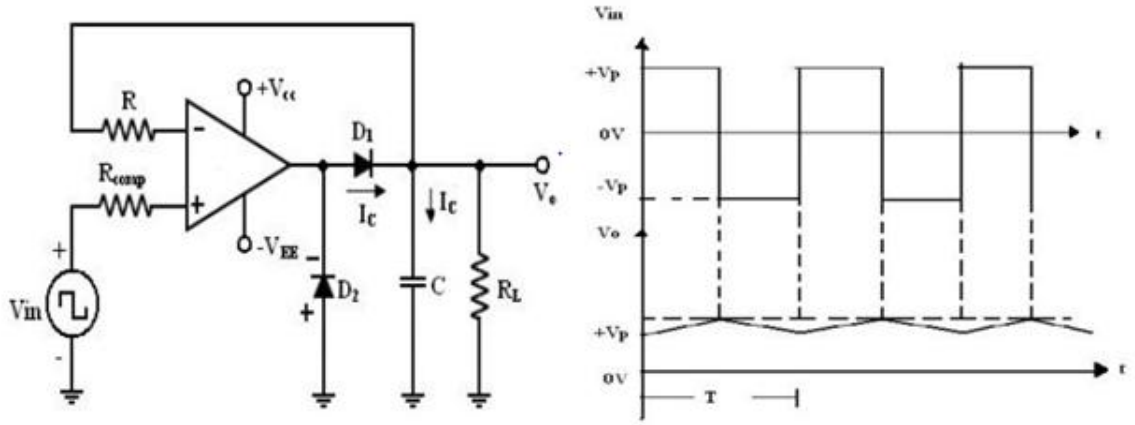

**6. b) R-2R ladder : (Diagram-2M, Explanation-2M, Any possible Combination-1M)**





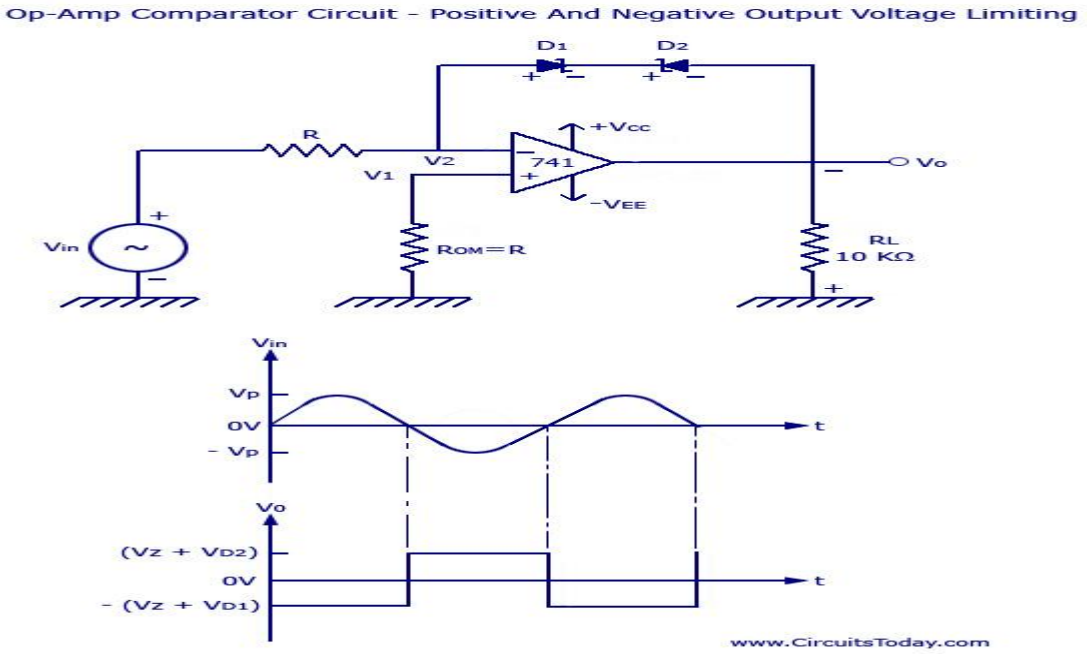

**7. a) Peak detector: (Explanation-3M, Diagram-2M, Waveform-1M)**

- To detect the peak of the waveform using op-amp.




**7. b) Voltage Limiter: (Definition-1M, Explanation-3M, Diagram-2M)**

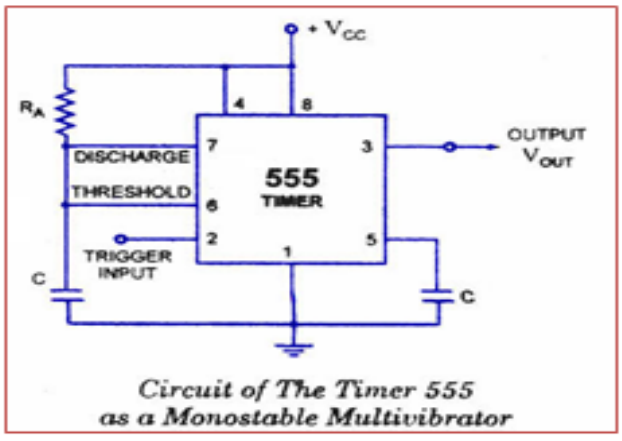
Voltage limiters are used to limit or clip the wave form upto required value by Normal diodes or Zener diodes.




**UNIT-IV**

**8. a)** **(Working-3M, Circuit Diagramp-3M)**

# 555 Timer as Monostable Multivibrator




*Circuit of The Timer 555 as a Monostable Multivibrator*

**Description:**

- In the standby state, FF holds transistor $Q_1$ ON, thus clamping the external timing capacitor C to ground. The output remains at ground potential. i.e. Low.
- As the trigger passes through $V_{cc}/3$, the FF is set, i.e. Q bar=0, then the transistor $Q_1$ OFF and the short circuit across the timing capacitor C is released. As Q bar is low , output goes HIGH.

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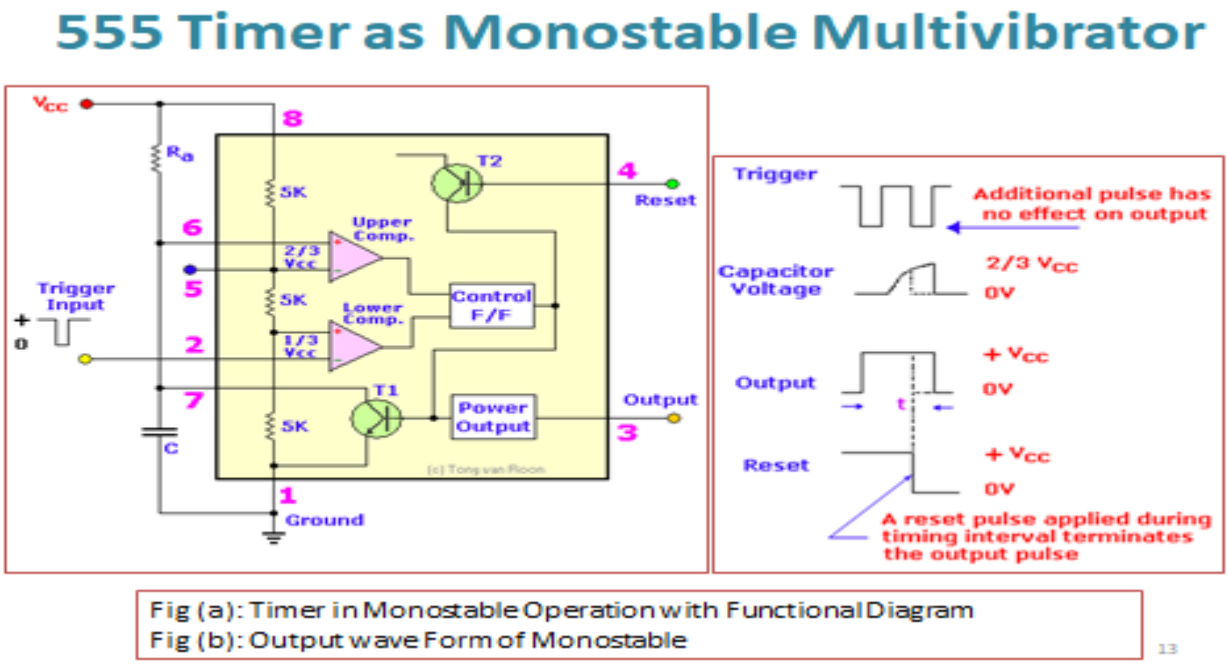
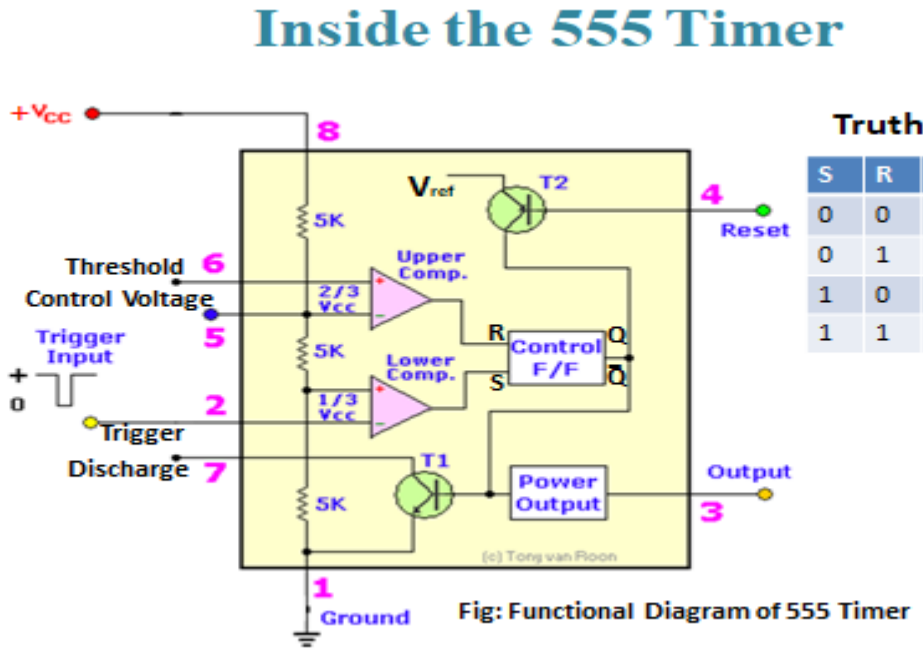



Fig (a): Timer in Monostable Operation with Functional Diagram
Fig (b): Output wave Form of Monostable

13

**8. b) Functional Diagram of 555 Timer:** **(Diagram-3M, Pin Descryption-3M)**



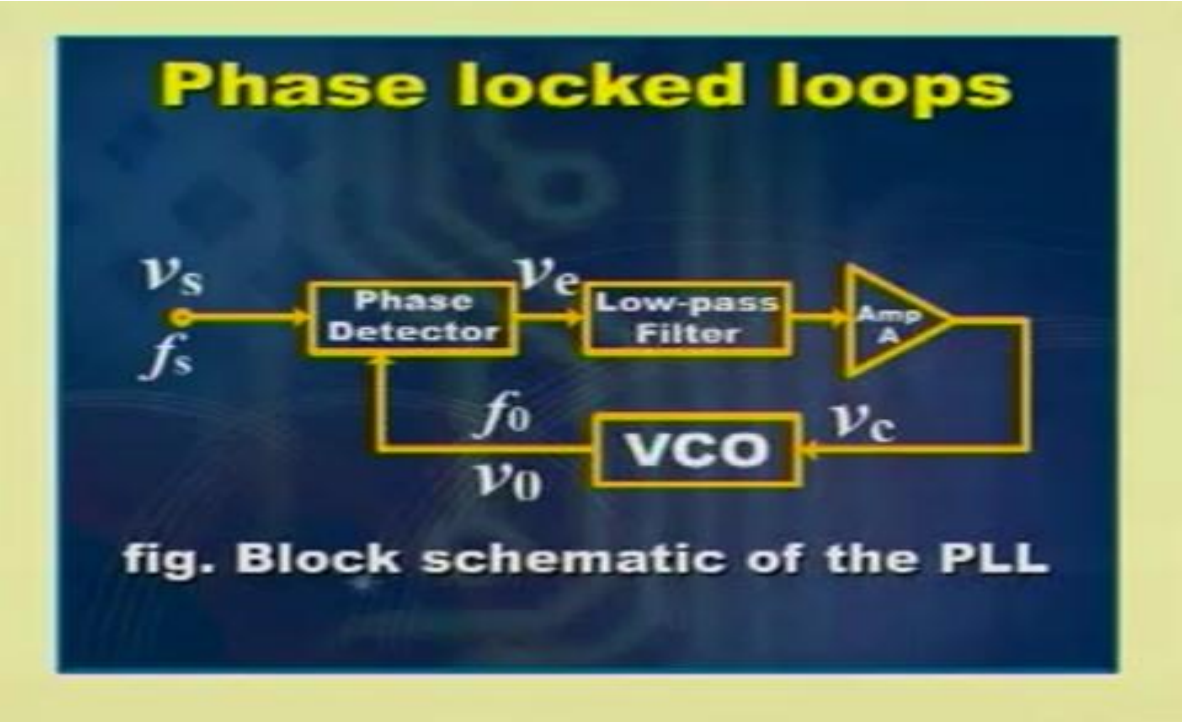

**Truth Table**

| S | R | Q | Q |
|---|---|---|---|
| 0 | 0 | No Change | |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | X | X |

**Fig: Functional Diagram of 555 Timer**

6

**9. a) Phase Locked Loop:** **(Explanation-2M, Diagram-2M, Derivation-2M)**




Phase locked loop construction and operation:

- The PLL consists of i) Phase detector ii) LPF iii) VCO. The phase detector or comparator compares the input frequency fIN with feedback frequency fOUT.
- The output of the phase detector is proportional to the phase difference between fIN & fOUT. The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage.
- The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO.
- The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.
- PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

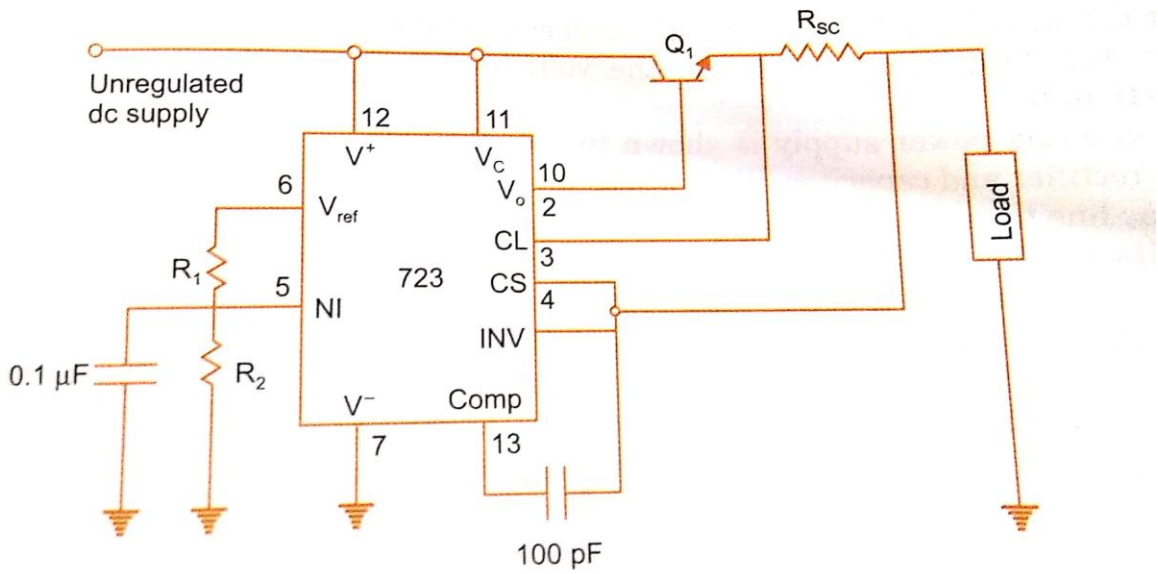
**9. b) Limitations of Three terminal voltage regulators:**

**(Limitations-2M, Explanation-2M, Diagram-2M)**

- No Short circuit protection
- It has fixed positive and negative voltage

**Current Boosting:**

The maximum current that 723 IC regulator can provide is 140mA. For many applications, this is not sufficient. It is possible to boost the current level simply by adding a boost transistor Q1 to the voltage regulator. The collector current of the pass transistor Q1 comes from the unregulated dc supply.


Unregulated
dc supply
12
11
V+
VC
10
Vo
2
6
Vref
CL
3
R1
5
723
CS
4
NI
INV
0.1 μF
R2
V−
Comp
7
13
100 pF
Q1
Rsc
Load