

Hall Ticket Number:

--	--	--	--	--	--	--	--	--	--

III/IV B.Tech (Regular\Supplementary) DEGREE EXAMINATION

Electrical and Electronics Engineering
Linear IC's and Applications

November, 2019

Fifth Semester

Time: Three Hours

Maximum : 60 Marks

Answer Question No.1 compulsorily.

(1X12 = 12 Marks)

Answer ONE question from each unit.

(4X12=48 Marks)

(1X12=12 Marks)

1 Answer all questions

- Define input offset voltage
- List out linear and non linear applications of OP-AMP
- What is the need of level translator in Op-Amp?
- List out the differences between Wien bridge and RC phase shift oscillator.
- Why practical integrator circuit is called Lossy integrator
- List out the limitations of voltage limiters
- What are the advantages and disadvantages of Successive Approximation A/D converter?
- Which is the more accurate A to D converter and why?
- What is meant by peak detector
- What is the purpose of reset pin in a 555 timer IC?
- Draw the block diagram of PLL.
- What are the advantages of active filters over passive filters?

UNIT I

- Explain the instrumentation amplifier with neat sketch and mention its applications 6M
- A square wave of peak to peak amplitude of 500mV has to be amplified to a peak to peak amplitude of 3 volts, with a rise time of 4 μ s or less, Can a 741 be used? 6M

(OR)

- List and explain the function of all the basic building blocks of an OP-AMP 6M
- Draw the circuit of a full wave rectifier and explain how it gives the average value. 6M

UNIT II

- With the help of a circuit diagram explain the functioning of triangular wave generator. 6M
- Schmitt trigger with the upper threshold level $V_{UT} = 0V$ and hysteresis width $V_H = 0.4V$ converts a 2KHz sine wave of amplitude $4V_{PP}$ in to a square wave. Calculate the time duration of the Negative and positive portion of the output wave form. 6M

(OR)

- Design a Wien bridge oscillator to oscillate at 5000Hz 6M
- Explain frequency response of Differentiator circuit. 6M

UNIT III

- Draw the circuit of weighted resistor DAC and derive expression for output analog voltage. 6M
- Draw and explain the circuit of a clipper which will clip the input signal below a reference voltage 6M

(OR)

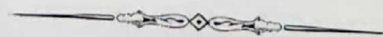
- Draw a sample and hold circuit. Explain its operation and indicate its uses 6M
- With a neat block diagram explain the data conversion procedure for dual slope ADC. 6M

UNIT IV

- With the help of a neat circuit diagram explain the working of an narrow band stop filter 6M
- Draw the block diagram of Monostable multivibrator using 555 timer and derive an expression for its frequency of oscillation. 6M

(OR)

- With the help of a neat circuit diagram explain the working of wide Band-pass filters. 6M
- What is frequency translation and explain FSK demodulation using 565 PLL 6M



- 1.
- a) Input offset voltage is the voltage that must be applied between two i/p terminals of op-amp to null the output
 - b) Linear applications include Inverting amplifiers, non-inverting amplifiers, voltage follower, v-I, I-v converter etc
Non-linear applications include zero crossing detector, Schmitt trigger, multivibrator, Precision rectifier etc.
 - c) Level translator (shifting) ckt is used to shift the dc level at the output of the intermediate stage downward to zero volts w.r. to ground
 - d)

<p>Wein bridge oscillator</p> <ul style="list-style-type: none">① Feedback network provides no phase shift② op-amp is used in non-inverting mode③ op-amp does not introduce phase shift	<p>RC phase shift oscillator</p> <ul style="list-style-type: none">Feedback network provides 180° phase shiftinverting modeop-amp introduces 180° phase shift
---	---
 - e) To avoid saturation problem, the feedback network capacitor (C_f) shunted by resistor (R_f). The combination of both behaves like practical capacitor which dissipates power. For this reason practical integrator is called lossy integrator

f) To keep O/P voltage swing between low values of voltage suitable for TTL logic other components like Zener diode are added onto ckt. Such circuits with specified o/p swing are called voltage limiters

g) adv. of successive appr. ADC

1. speed high compared to counter ADC
2. Good ratio of speed to power

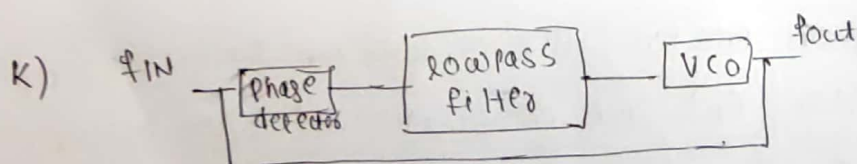
Drawbacks

1. cost is high bec of SAR
2. complexity in design

h) Dual slope ADC is relatively more accurate because it integrate (averages) the noise

i) peak detector measures the positive peak values of square wave i/p. (or) peak detector measures the peak values of non-sinusoidal waveforms

j) The reset pin i.e. pin 4 of 555 IC timer is used to restart the timing operation



- 1) gain and frequency adjustment flexibility
2. no loading problem
3. low cost

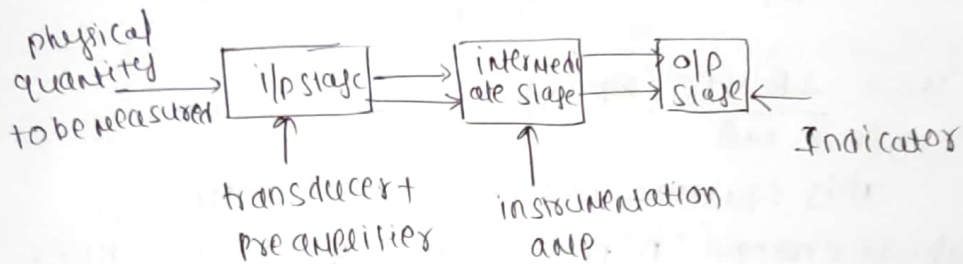
UNIT-1

Q.
a.

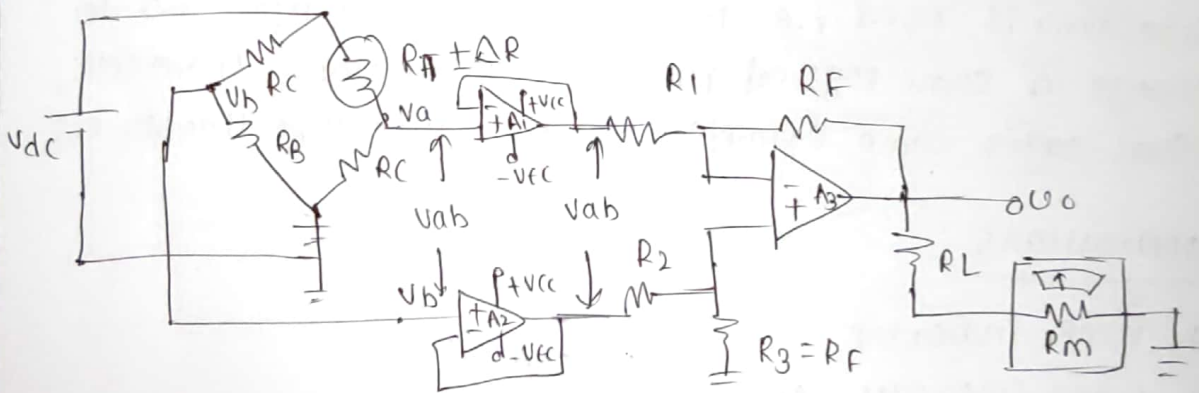
Many industrial and consumer applications measurement and control of physical conditions are important. Transducer is device used to convert physical to electrical quantity vice versa.

Diagram - 2M
Theory - 1M
Derivation - 2M
Applications - 1M

Instrumentation system is used to measure o/p signal produced by transducer. Below figure shows block diagram



Below figure shows differential instrumentation amplifier using a transducer bridge.



when bridge is balanced

$$V_a = V_b$$

$$\frac{R_B(V_{dc})}{R_B + R_C} = \frac{R_A(V_{dc})}{R_A + R_T} \rightarrow \frac{R_C}{R_B} = \frac{R_T}{R_A}$$

The bridge is balanced at a desired ref. value. As the physical quantity to be measured changes, the resi. of transducer also changes which causes the bridge to unbalance. The o/p voltage of the bridge can be expressed as fn. of change in resistance of transducer

$$V_a = V_{dc} \left(\frac{R_A}{R_A + R_T + \Delta R} \right)$$

$$V_b = \frac{R_B (V_{dc})}{R_B + R_C}$$

$$\text{if } R_B = R_A = R_C = R_T = R$$

$$V_{ab} = V_a - V_b = \frac{-\Delta R V_{dc}}{2(2R + \Delta R)}$$

The V_{ab} applied to differential instrumentation amplifier composed of three op-amps. now V_o is

$$V_o = \left(-\frac{R_F}{R_1} \right) V_{ab} = \frac{(\Delta R) V_{dc}}{2(2R + \Delta R)} \cdot \frac{R_F}{R_1}$$

$$V_o = \frac{\Delta R \cdot V_{dc}}{4R} \cdot \left(\frac{R_F}{R_1} \right)$$

This equation indicates V_o is directly proportional to change in resistance ΔR of transducer. since change in resistance is caused by change in physical energy, a meter connected at the o/p can be calibrated in terms of units of physical energy. Here resistive type transducer is used i.e. resistance of this changes w.d to change in some physical quantity. thermistors, photo cells, Strai gages some examples of resistive type transducers

applications

1. Temp. indicator
2. light intensity meter
3. Temp. controller
4. Measurement of flow and thermal conductivity

2.
b.

since op has peak amplitude greater than 1 volt, the slew rate is the limiting factor

$$\text{slew rate } \frac{\Delta V}{\Delta t}$$

rise time is change in the op voltage ΔV in 4 μs (or) less equal to

$$(0.9 - 0.1) 3V = 2.4V$$

$$\begin{aligned} \text{Slew rate} &= \frac{2.4V}{4 \times 10^{-6}} = 0.6 \times 10^6 \text{ V/s} \\ &= 0.6 \text{ V}/\mu\text{s} \end{aligned}$$

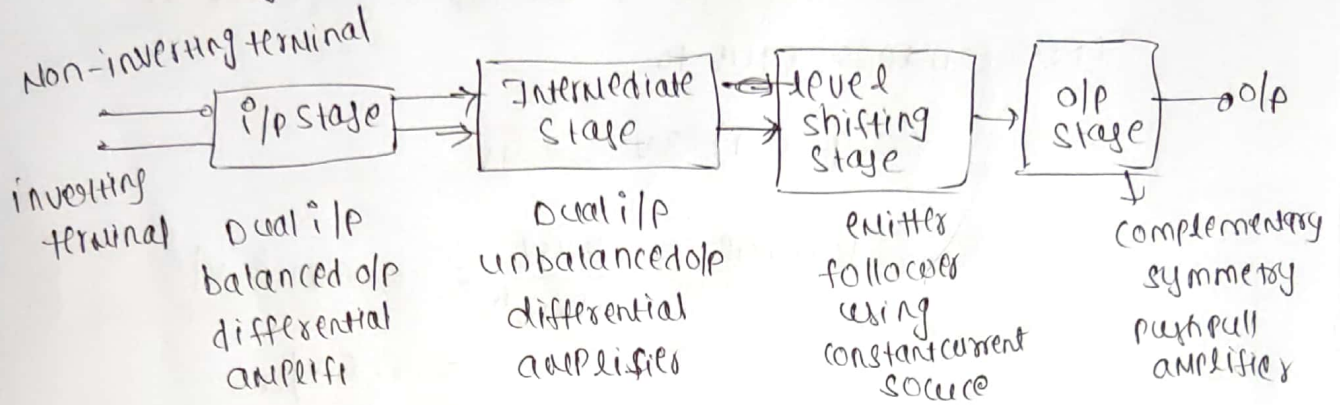
since slew rate of op-amp is $0.5 \text{ V}/\mu\text{s}$ it is too slow so IC 741 cannot be used.

slew rate formula - 2V
Procedure - 3M
conclusion - 1M

3
9.

Operational amplifier is direct coupled high gain amplifier usually consists of one or more differential amplifiers and usually followed by level translator and output stage. The output stage is generally push pull complementary symmetry pair.

Block diag-2M
each block - 1M
4x1 → 4M



i/p stage :- dual i/p balanced o/p differential amplifiers. This provides most of gain of amplifier and also establishes i/p resi of op-amp.

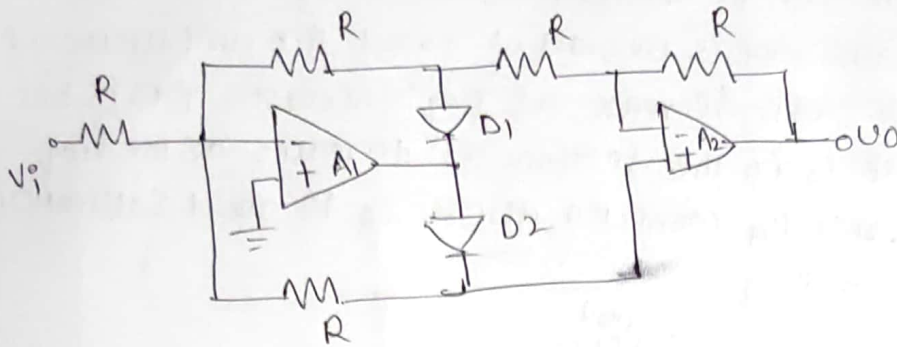
Intermediate stage :- This is another differential amplifier which is driven by o/p of first stage. In most cases this is dual i/p balanced (single-ended) o/p. Bec. of direct coupling is used dc voltage of this is well above the ground potential.

level shifting stage :- after 2nd stage level translator is used to shift dc level at the o/p of 2nd stage downward to zero potential bec. of direct coupling.

o/p stage :- This uses push-pull complementary amplifiers. This stage increases o/p voltage swing and raises the current supplying capability of op-amp. Well designed o/p stage provides low o/p resistance.

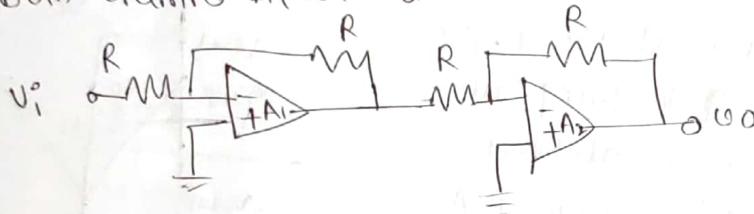
3.
b.

A full wave rectifier (or) absolute value ckt gives average value. It uses two op-amps and diodes, resistors.



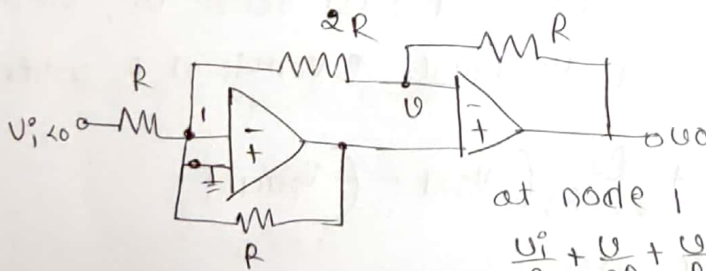
- ① for +ve i/p $V_i > 0$ diode D_1 is ON \rightarrow short ckt
diode D_2 is OFF \rightarrow open ckt

both opamps A_1 and A_2 act as inverters



②

- for -ve i/p $V_i < 0$ diode D_1 off \rightarrow open ckt
 D_2 on \rightarrow short circuit



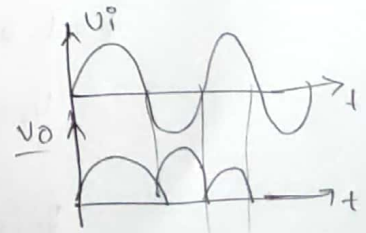
at node 1

$$\frac{V_i}{R} + \frac{V}{2R} + \frac{V}{R} = 0$$

$$V_i = -3/2 V \rightarrow V = -2/3 V_i$$

$$V_o = (1 + R/2R) \left(-2/3\right) V_i = -2 V_i$$

here $V_i < 0$ so $V_o = +V_i$

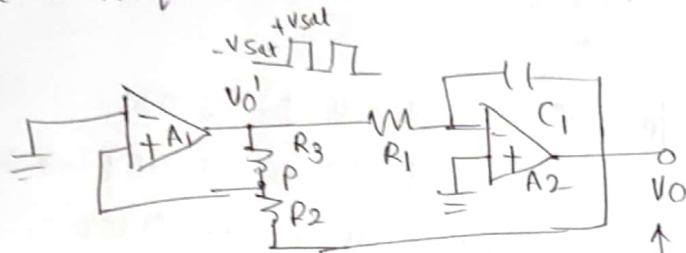


ckt diagram - 2M
case 1 - 2M
case 2 - 2M

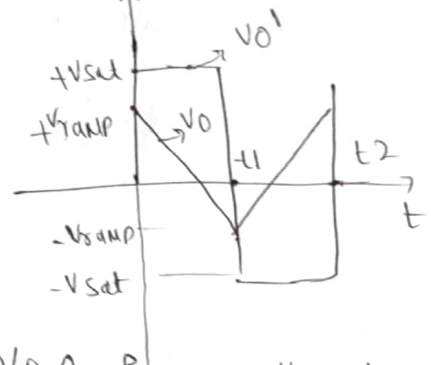
UNIT-11

4
a.

Triangular wave can be obtained by integrating square wave. amplitude of square wave is constant at $\pm V_{sat}$ the amplitude of triangular wave will decrease as freq increases. This is because of reactance of cap C_2 in the feedback ckt decreases as the freq increases. the resi R_4 connected across C_2 to avoid saturation problem at low freq.



Initially o/p of A_1 is at $+V_{sat}$. The o/p of A_2 will be $-ve$ going ramp. thus one end of $R_2 R_3$ is at $+V_{sat}$ and other at $-ve$ going ramp of A_2 .



at $t = t_1$ the effective voltage at P slightly less than zero. This switches o/p A_1 from $+V_{sat}$ to $-V_{sat}$. At $t = t_2$ the voltage at P just above 0V, switch o/p of A_1 from $-V_{sat}$ to $+V_{sat}$. • Voltage at P when A_1 at $+V_{sat}$ is

$$-V_{ramp} + \frac{R_2}{R_2 + R_3} (V_{sat} - (-V_{ramp}))$$

$$\text{At } t = t_1 \quad V_p = 0$$

$$-V_{ramp} = -\frac{R_2}{R_3} (+V_{sat})$$

$t = t_2$, when o/p of A_1 switches from $-V_{sat}$ to $+V_{sat}$

$$V_{ramp} = -\frac{R_2}{R_3} (-V_{sat}) = \frac{R_2}{R_3} (V_{sat})$$

$$V_o(p-p) = V_{ramp} - (-V_{ramp}) = \frac{2R_2}{R_3} V_{sat}$$

o/p switches from $-V_{ramp}$ to $+V_{ramp}$ in half period $T/2$.

$$V_o = -\frac{1}{RC} \int v_i dt$$

$$V_o(p-p) = -\frac{1}{R_1 C_1} \int_0^{T/2} (-V_{sat}) dt$$

$$V_o(p-p) = \frac{V_{sat}}{R_1 C_1} \left(\frac{T}{2}\right)$$

$$T = 2 R_1 C_1 \frac{V_o(p-p)}{V_{sat}}$$

$$T = \frac{4 R_1 C_1 R_2}{R_3}$$

$$f = \frac{1}{T} = \frac{R_3}{4 R_1 C_1 R_2}$$

diag - 1M
 waveform - 1M
 theory - 2M
 derivation - 2M

H
 b.

$$V_{UT} = 0V$$

$$V_{HT} = 0.4V$$

$$f = 2KHz$$

$$V = HV_{p-p}$$

waveform - 1M
 formula - 2M
 procedure - 3M

$$V_{HT} = V_{UT} - V_{LT} = 0 - V_{LT}$$

$$V_{LT} = -0.4V$$

$$-0.4 = V_m \sin(\pi + \theta)$$

$$= -V_m \sin \theta$$

$$0.4 = -V_m \sin \theta$$

$$0.4 = -a \sin \theta$$

$$\theta = 0.1 \text{ radian}$$

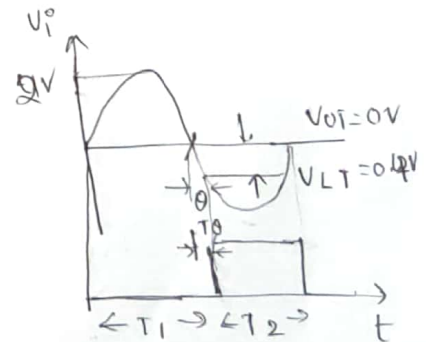
$$T = \frac{1}{f} = \frac{1}{1000} = 1ms$$

$$\omega T \theta = 2\pi (1000) \theta = 0.1$$

$$T \theta = \frac{0.1}{2\pi} = 0.016ms$$

$$T_1 = T/2 + T \theta = 0.516ms$$

$$T_2 = T/2 - T \theta = 0.48ms$$



5
a.

$$f_0 = 5 \text{ kHz}$$

$$\text{Let } C = 0.05 \mu\text{F}$$

$$f_0 = \frac{1}{2\pi RC} = \frac{0.159}{RC}$$

$$f_0 = \frac{0.159}{R \times 0.05 \times 10^{-6}}$$

$$5 \text{ kHz} = \frac{0.159}{R \times 0.05 \times 10^{-6}}$$

$$5 \times 10^3 = \frac{0.159}{R \times 0.05}$$

$$R = \frac{0.159}{25 \times 10^{-5}} = \frac{15900}{25} = 636 \Omega$$

$$\text{let } R_1 = 12 \text{ k}\Omega$$

$$1 + \frac{R_F}{R_1} = 3$$

$$\frac{R_F}{R_1} = 2$$

$$R_F = 2 \times 12 \text{ k}\Omega = 24 \text{ k}\Omega$$

USE $R_F = 50 \text{ k}\Omega$ potentiometer

Formula - 2M

$R_{cal} = 1M$

$R_1 = 1M$

$R_F = 2M$

5
b.

Differentiator:-

this circuit performs the mathematical operation of differentiation i.e. op waveform is the derivative of the ip waveform. It may be constructed from basic inverting amplifier if an ip resistor R_1 is replaced by capacitor C_1

$$i_c = i_B + i_f$$

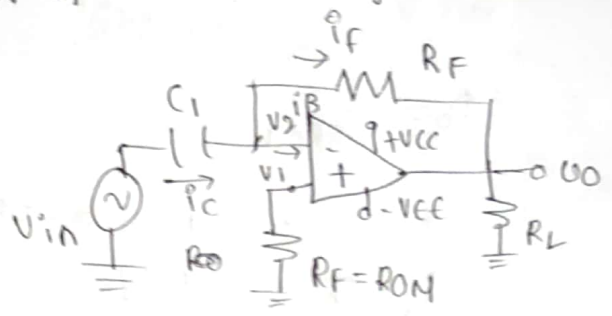
$$i_c = i_f$$

$$C_1 \frac{d(V_{in} - V_o)}{dt} = \frac{V_o - V_o}{R_f}$$

$V_1 = V_2 = 0$, bec. A is very large

$$C_1 \frac{dV_{in}}{dt} = -\frac{V_o}{R_f}$$

$$V_o = -R_f C_1 \frac{dV_{in}}{dt}$$



$$V_o = -R_f C_1 \frac{dV_{in}}{dt}$$

thus op is equal to $R_f C_1$ times the -ve instantaneous rate of change of ip input voltage V_{in} with time.

$$V_o(s) = -R_f C_1 s U_i(s)$$

$$|A| = |V_o/V_i| = |-j\omega R_f C_1| = \omega R_f C_1$$

$$|A| = f/f_a \quad f_a = 1/2\pi R_f C_1$$

$f < f_a \rightarrow |A| \rightarrow$ ~~increases~~ increases

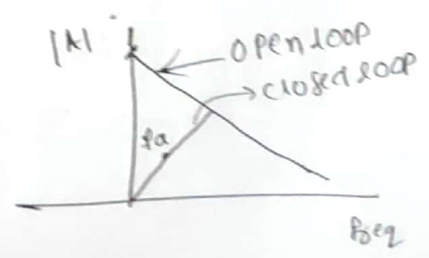
$f = f_a \rightarrow |A| = 1$

$f > f_a \rightarrow |A| \rightarrow$ ~~decreases~~ decreases

at high freq. differentiator unstable break into oscillations.

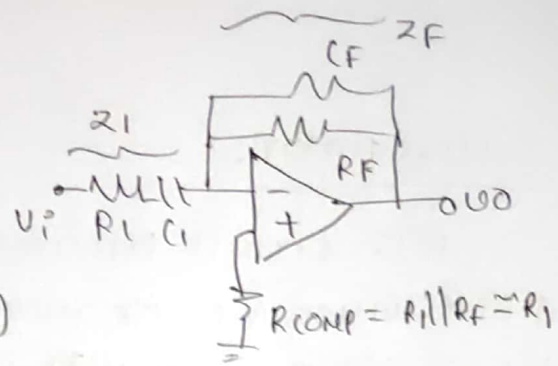
the ip impedance ($1/\omega C_1$) decreases with increasing in freq. there by making the circuit sensitive to high frequency noise.

practical differentiator eliminates the problem of instability and high frequency noise.



$$\frac{V_{OC}(s)}{V_i(s)} = -\frac{Z_F}{Z_I}$$

$$= -\frac{S R_F C_I}{(1 + S R_F C_F)(1 + S C_I R_I)}$$



$$\frac{V_{OC}(s)}{V_i(s)} = -\frac{S R_F C_I}{(1 + S R_F C_I)} = -\frac{S R_F C_I}{(1 + j f / f_b)}$$

$$f_b = \frac{1}{2\pi R_F C_I}$$

$f < f_b \rightarrow A_F = \text{increases}$

$f = f_b \rightarrow A / \sqrt{2}$

$f > f_b \rightarrow \text{decreases}$

$$V_O = -R_F C_I \frac{dV_i}{dt}$$

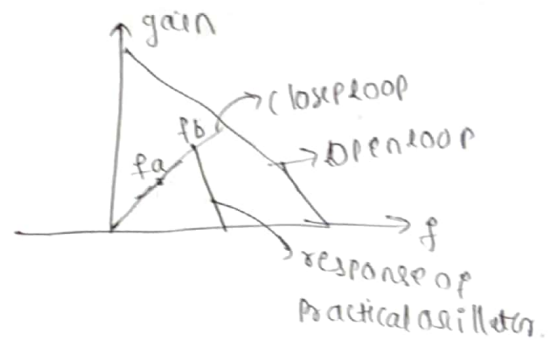


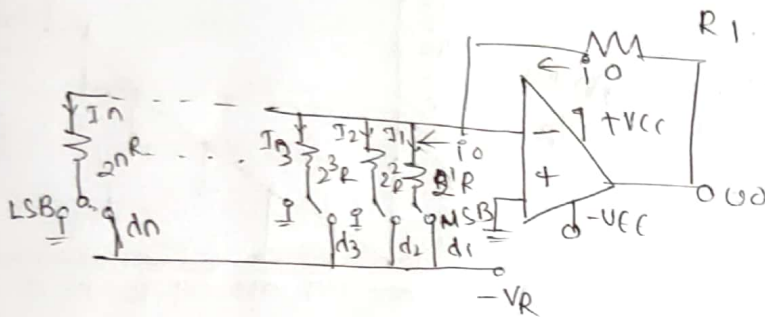
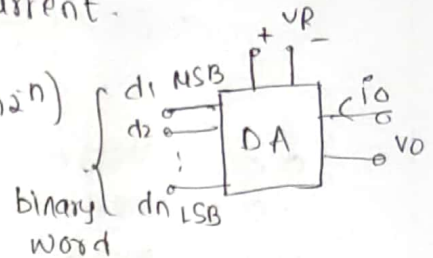
diagram - 2M
 freq resp - 1M
 derivation and
 theory - 3M

6

a. weighted resistor DAC

The i/p to the n-bit binary word D and is combined with ref. voltage V_R to give an analog o/p signal. The o/p of DAC can be either voltage or current.

$$V_O = K V_{FS} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n})$$



One of simplest DAC uses summing amplifiers with a binary weighted resistors. n electronic switches d_1, d_2, \dots, d_n controlled by binary word, the binary i/p to particular switch is 1, it connects the resistance to ref voltage $-V_R$ and if the input bit is 0, the switch connects the resistor to ground.

$$I_O = I_1 + I_2 + \dots + I_n$$

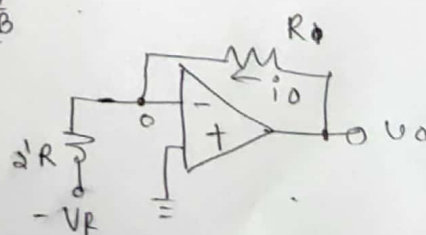
$$= \frac{V_R d_1}{2R} + \frac{V_R d_2}{2^2 R} + \dots + \frac{V_R d_n}{2^n R}$$

$$= \frac{V_R}{R} \left[d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n} \right]$$

$$V_O = I_O R_F = \frac{V_R \cdot R_F}{R} \left[d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n} \right]$$

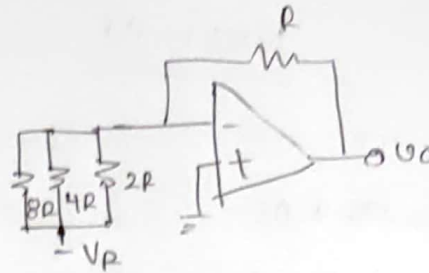
if i/p binary word is 1000

Switch d_1 connected to $-V_R$ and other switches are grounded



$$\frac{-V_R - 0}{2R} = \frac{-V_O}{R} \rightarrow V_O = V_R / 2$$

if i/p is 111



$$-\frac{V_R}{8R} - \frac{V_R}{4R} - \frac{V_R}{2R} = -\frac{V_{OO}}{R}$$

$$V_{OO} = \left(\frac{1}{8} + \frac{1}{4} + \frac{1}{2}\right) V_R = \left(\frac{1+2+4}{8}\right) V_R = \frac{7V_R}{8}$$

000	\$V_R/8\$ 0
001	\$V_R/8\$
010	\$2V_R/8\$
011	\$3V_R/8\$
100	\$4V_R/8 \rightarrow V_R/2\$
101	\$5V_R/8\$
110	\$6V_R/8\$
111	\$7V_R/8\$

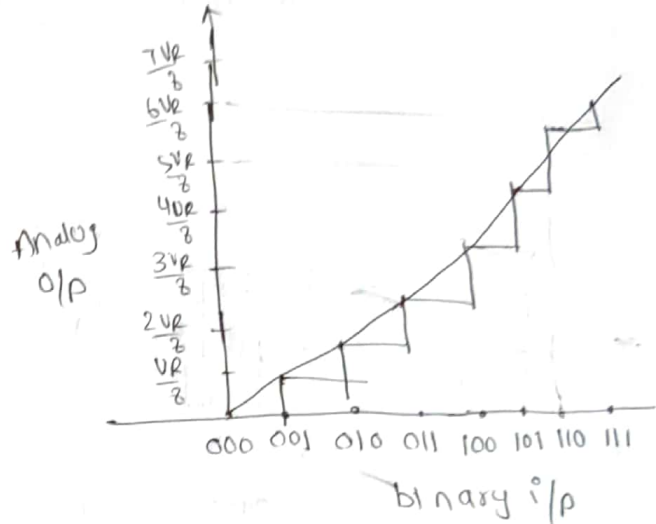


diagram - 1M
 calculation - 3M
 theory - 2M
 graph - 1M
 table

6

b Negative clipper circuit with $V_{ref} = +1V$

wave shaping tech. includes limiting, clipping, clamping
OP-AMP clipper ckt uses a rectifier diode to remove certain portion of i/p signal to obtain desired o/p waveform.

Negative clipper, a circuit which negative part of i/p signal can be formed by using an op-amp with rectifier diode. Additionally the clipping level is determined reference voltage.

$$V_{id} = V_1 - V_2$$

Case 1 :- when $V_{in} = +ve$ $V_o' = +ve$

$$V_{in} < V_{ref}$$

if i/p voltage less than reference voltage

diode D is reverse biased i.e. D=OFF acts as open ckt

$$V_o = V_{ref}$$

$V_{in} > V_{ref} \rightarrow$ D is forward biased D=ON acts as short ckt
so ckt acts as voltage follower o/p follows i/p

$$\underline{V_o = V_{in}}$$

Case 2 :- when $V_{in} = -ve$ $V_o' = -ve$

when input is -ve whatever the values of -ve voltage D is reverse biased (D=OFF) acts as open circuit

$$V_o = V_{ref}$$

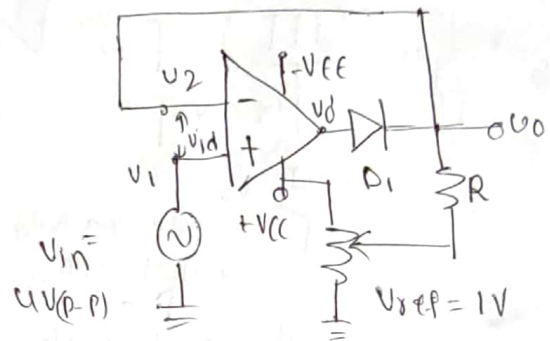
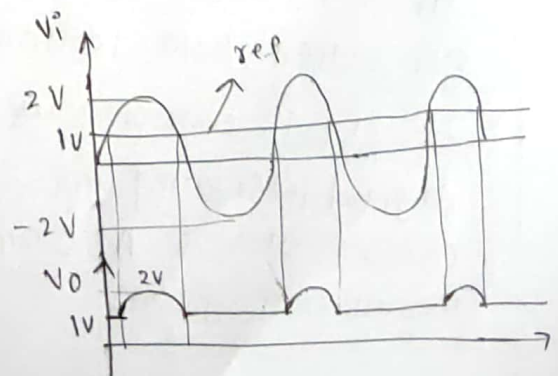
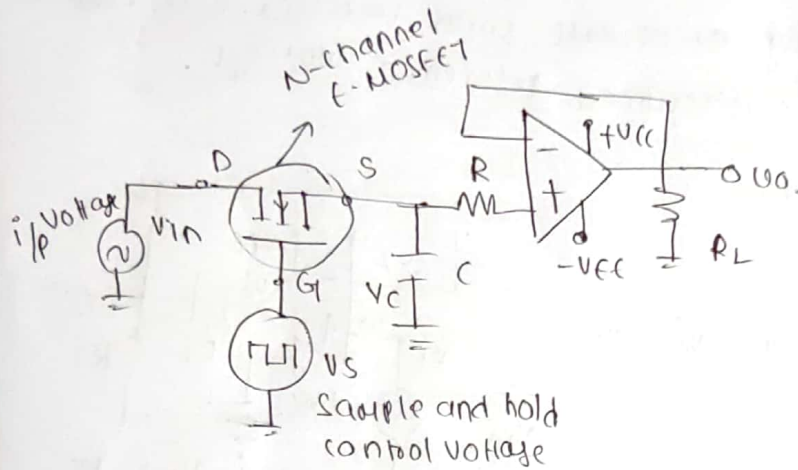


diagram - 2M
theory - 2M
waveform - 2M



7
a.

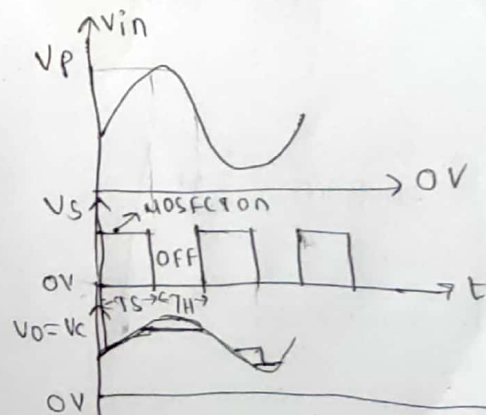
The sample and hold circuit samples the i/p signal and hold on to its last sampled value until the i/p signal is sampled again. uses op-amp and E-MOSFET. In this circuit E-MOSFET acts as switch that is controlled by the sample and hold control voltage V_S and capacitor C serves as a storage element.



diag-2M
theory-2M
waveform-2M

The analog i/p signal which to be sampled V_{in} is applied to drain, and the sample and hold control voltage V_S applied to gate of E-MOSFET. during the positive portion of V_S the E-MOSFET conducts and acts as closed switch. This allows i/p voltage to charge capacitor C , which in turn at output. On otherhand when V_S is zero E-MOSFET off and acts as open switch. capacitor starts discharge through op-amp. However the i/p resistance of op-amp voltage follower is very high hence the voltage across C retained. The time period T_S of sample and hold control voltage V_S during which the voltage across capacitor equal to input voltage is called sampling period. The time period T_H of V_S during which voltage across capacitor is constant are called hold periods.

It is commonly used in digital interfacing and communications such as ADC and pulse modulation systems.

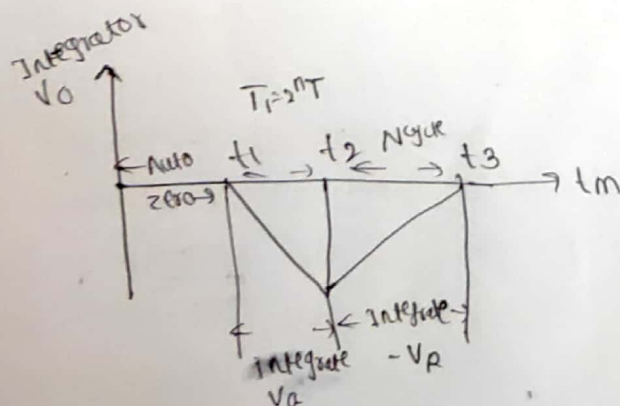
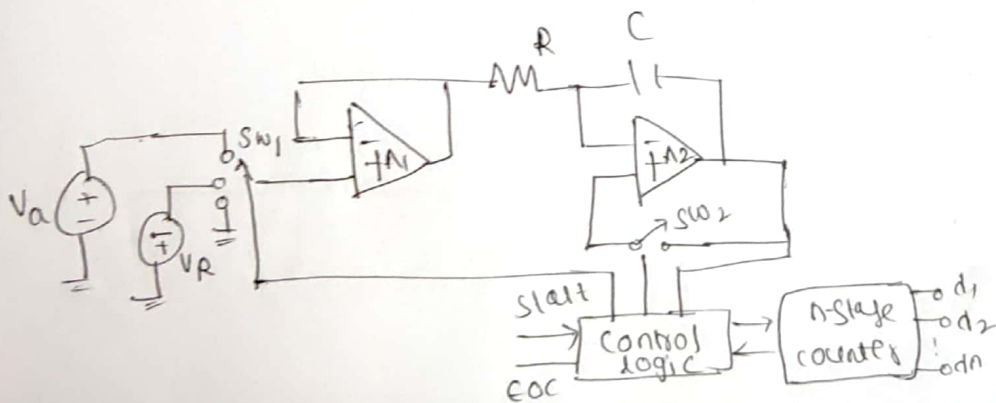


7.
b.

dual slope ADC

The analog part of CRT consists of high z_i buffer A_1 , precision integrator A_2 and voltage comparator. The converter first integrates the analog i/p signal V_a for fixed duration of an clock period. Then integrates an interval ref. voltage V_R of opposite polarity until integrator o/p is zero. The number N of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period. Hence N represents the desired output code.

At the arrival of start command at $t=t_1$ control logic opens SW_2 and connects SW_1 to V_a and enables the counter starting from zero. The circuit uses an n -stage ripple counter and therefore the counter resets to zero after counting 2^n pulses. The analog i/p V_a is integrated for fixed no. of 2^n counts of clock pulses after which the counter resets to zero. If the clock period is T , the integration takes place for a time $T_1 = 2^n \times T$ and o/p is ramp going downwards



diag - 2N
waveform - 1N
theory - 3N
and derivation

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}}$$

$$t_3 - t_2 = \frac{\text{digital count} \times 1}{\text{clock rate}}$$

$$V_0 = -\frac{1}{RC} V \Delta t$$

$$V_1 = (-1/RC) V_a (t_2 - t_1)$$

$$V_1 = (-1/RC) (-V_R) (t_2 - t_3)$$

$$V_a (t_2 - t_1) = V_R (t_3 - t_2)$$

$$V_a 2^n = V_R (N)$$

$$V_a = V_R (N/2^n)$$

advantages

- ① analog voltage V_a proportional to count reading
- ② integrates input signal for fixed time hence it provides excellent noise rejection of ac signals whose periods are integral multiples of integration time T_1 .

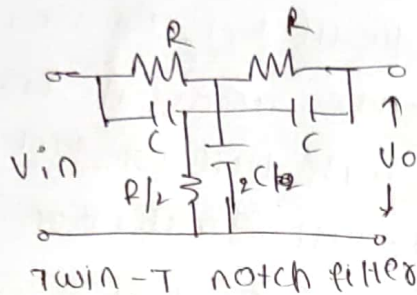
main disadvantage is long conversion time.

These converters particularly suitable for accurate measurement of slowly varying signals such as thermocouples and weighing scales

8
a.

Narrow band reject filter

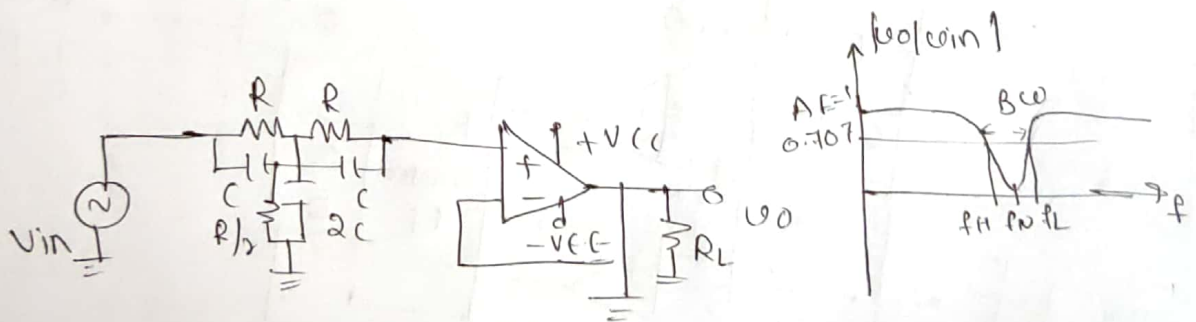
Band reject (or) band stop (or) band elimination filters are those frequencies are attenuated in stop band and passed outside this band. These filters are commonly called as notch filters. Bec. of higher $Q (>10)$ BW of this filter is very small



diag - 2M
theory - 3M
waveform - 1M

it is commonly used for the rejection of single frequency such as 60Hz power line frequency hum. The most commonly used notch filter is twin-T now. one is made up of 2 resistors and one capacitor while other uses two capacitors and a resistor. the notchout freq. is the freq at which maximum attenuation occurs given by

$$f_N = \frac{1}{2\pi RC}$$

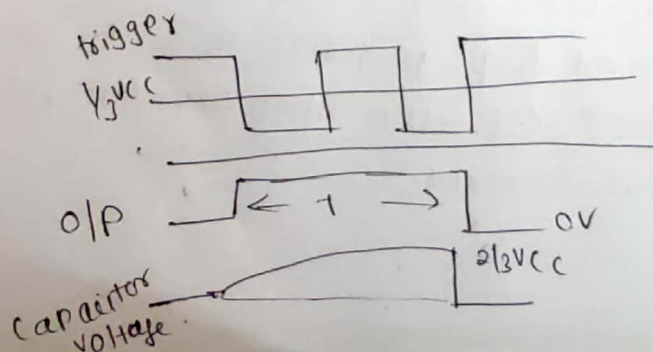
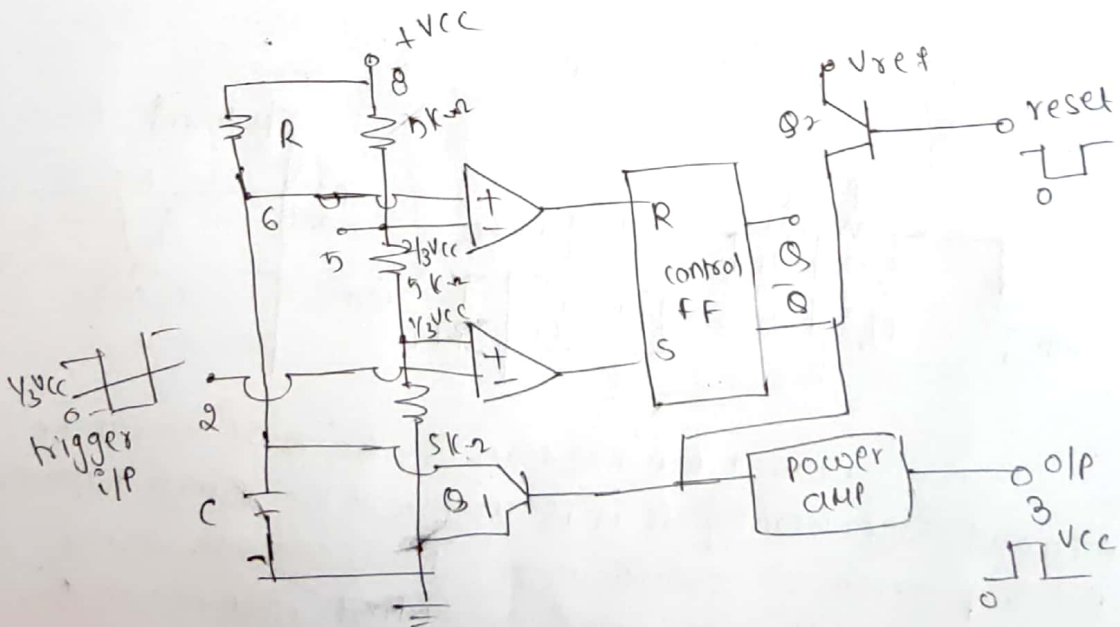


Twin-T now has low Q . the Q of now can be increased significantly if it is used with the voltage follower. the freq. response shown above. most common use of filter is communications and biomedical instruments for eliminating undesired freq. to design this for specific f_N chose the value of cap $<1\mu F$ then calculate required value of R using above formula.

8.
b.

Monostable multivibration using 555 timer

In standby state flipflop holds transistor Q_1 on thus clamping the external timing capacitor C to ground. The o/p remains at ground potential i.e. low. As the trigger passes through $V_{CC}/3$ the FF is set i.e. $Q=0$. This makes Q_1 off and short circuit across timing capacitor C released. As Q low, the o/p goes HIGH ($=V_{CC}$). The timing cycle now begins since C unclamped the voltage across it rises exponentially through R towards V_{CC} with time constant RC . The time period T , after the V_C just greater than $2/3 V_{CC}$ and the upper comparator resets the FF, that is $R=1, S=0$ (assuming very small trigger pulse). This makes $Q=1, Q_1$ goes on there by discharging capacitor C rapidly to ground. The o/p returns to standby state (o/s) ground potential.

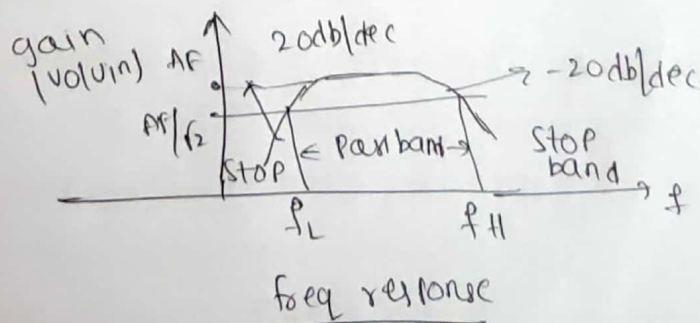
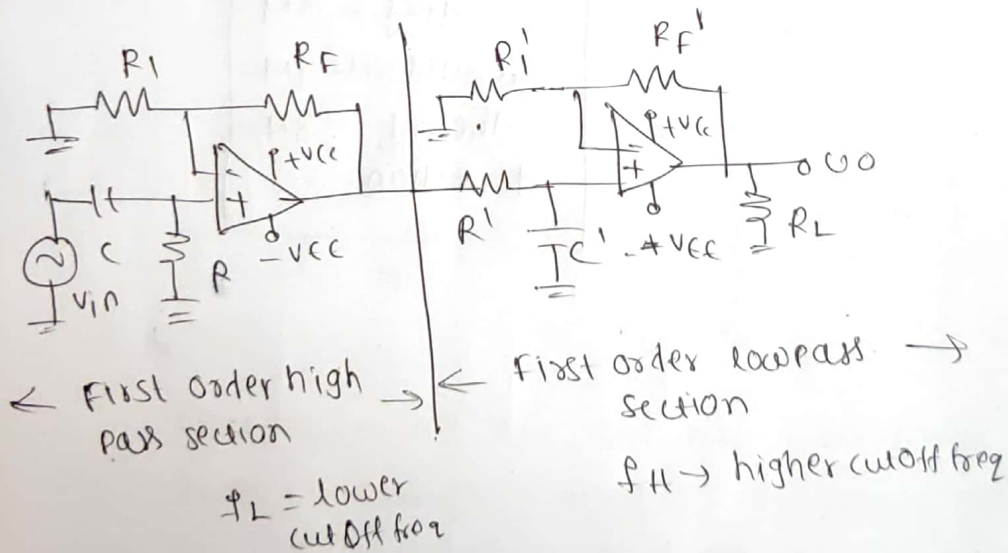


9
a.

wide band pass filter

Band pass filter has passband b/w two cutoff frequencies f_H and f_L such that $f_H \gg f_L$. Any i/p freq outside this band is attenuated. wide band pass filters have low Q (< 10) and Bw is high.

wide band pass filter can be formed by cascading high pass and low pass sections and generally the choice ~~of~~ for simplicity of design. To obtain $\pm 20\text{dB/dec}$ bandpass, first order high pass and low pass sections are cascaded. For $\pm 40\text{dB/dec}$ band pass filter second order high pass and low pass sections are cascaded. order of bandpass filter depends on order of high pass and low pass sections. To realize Bandpass filter response, f_H must be larger than f_L .



the voltage across cap

$$V_c = V_{CC} (1 - e^{-t/RC})$$

$$t = T \quad V_c = \frac{2}{3} V_{CC}$$

$$\frac{2}{3} V_{CC} = V_{CC} (1 - e^{-T/RC})$$

$$e^{-T/RC} = \frac{1}{3}$$

$$T = RC \ln(3)$$

$$T = 1.1 RC \text{ sec.}$$

monostable multivibrator can be used as missing pulse detector, linear ramp generator, freq divider, pulse width modulation

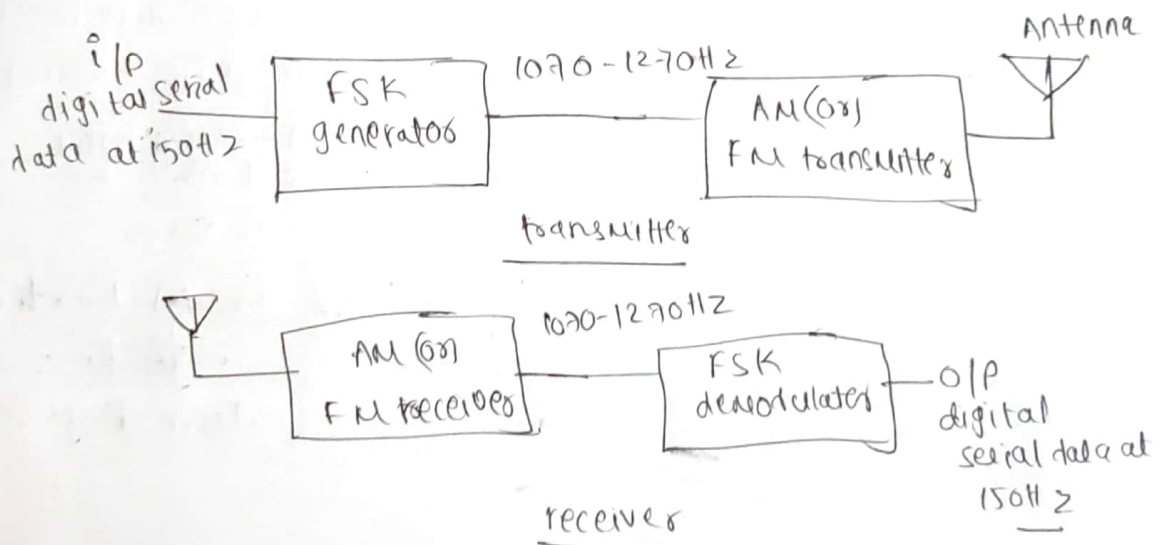
diag - 24
waveform - 14
theory, - 34
derivation

9
b.

frequency translation means the process of transferring a signal from one part of frequency axis to other is called frequency translation. It occurs frequently in the wireless communication system i.e. this is used to transfer the pass band signal to base band signal

FSK demodulator

In wireless communications the binary data (or code) is transmitted by means of carrier freq that is shifted b/w two preset frequencies. since carrier freq is shifted b/w two preset frequencies the data transmission is said to be FSK technique. a very useful application of SSS PLL is FSK demodulator.



block diagram of AM and FM transmitters and receivers. FSK generator is formed by using SSS as astable multivibrator whose freq is controlled by state of BJT Q_1 . The o/p frequency of FSK generator depends on logic state of digital data i/p. when i/p is logic 1, 0, off. under this ~~mode~~ ~~mode~~ works in its normal mode as astable multivibrator, cap charges through R_A and R_B to $2/3 V_{CC}$ and discharges through R_B to $1/3 V_{CC}$. capacitor charges and discharges alternatively b/w $2/3 V_{CC}$ and $1/3 V_{CC}$ as long as the input is at logic 1 state

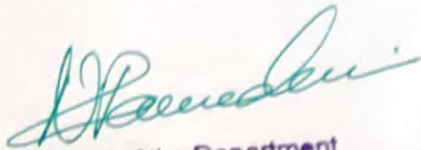
the frequency of o/p waveform is

$$f_0 = \frac{1.45}{(R_A + 2R_B)C} = 1070 \text{ Hz}$$

on other hand when i/p is logic 0, Q_1 on which in turn connects resistors R_C across R_A . this action reduces the charging time of cap. and increases o/p freq.

$$f_0 = \frac{1.45}{(R_A \parallel R_C + 2R_B)C} = 1270 \text{ Hz}$$

HOD Signature



Head of the Department
Electrical & Electronics Engg.
Bapatla Engineering College
BAPATLA - 522101.

Scheme prepared

by M. Nagendra

1. M. Nagendra

Asst. Professor

EEE department

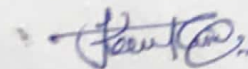
phone no. 8328079613

2. M. Suresh Babu

Asst. Professor

EEE Dept.

3. Dr. N. Karthik



Assoc. Professor.