18EI302

Hall Ticket Number:

II/IV B.Tech (Regular) DEGREE EXAMINATION

November, 2019
Third Semester
Time: Three Hours

Electronics & Instrumentation Engg.
Electronic Devices & Circuits
Maximum : 50 Marks

Answer Question No.1 compulsorily. (1X10 = 10 Marks)

Answer ONE question from each unit. (4X10=40 Marks)

1 Answer all questions (1X10=10 Marks)

a) What is doping?
b) What is drift current?
c) Write law of mass action.
d) Find the factor by which the reverse saturation current of silicon diode will get multiplied when the temperature is increased from 27°C to 47°C.
e) Which configuration of BJT has high input resistance?
f) In a BJT, write the relation between α and β.
g) Define threshold voltage of a MOSFET.
h) What is the relation between μ, g_m and r_d in a MOSFET.
i) What is the approximate voltage gain of source degenerated amplifier?
j) What is the advantage of using active load in an amplifier?

UNIT I

2 a) Derive the expressions for intrinsic carrier concentrations using energy band model. 5M

b) If the effective mass of an electron is equal to twice the effective mass of a hole, find the distance (in electron volts) of the Fermi level in an intrinsic semiconductor from the centre of the forbidden band at room temperature. 5M

(OR)

3 a) List basic equations that are useful for semiconductor device analysis and describe the variables. 5M

b) In a semiconductor, it is observed that three quarters of current is carried by electrons and one quarter by holes. If at this temperature, the drift speed of electrons is three times that of the holes, determine the ratio of electrons to holes in the semiconductor. 5M

UNIT II

4 a) Explain avalanche breakdown mechanism in a diode? 5M

b) The diode current is 0.6mA when the applied voltage is 400mV and 20mA when the applied voltage is 500mV. Determine η at room temperature. 5M

(OR)

5 a) Compare the three configurations of a Bipolar Junction Transistor 5M

b) Determine the quiescent currents and the collector to emitter voltage for a silicon transistor with $\beta = 50$ in the self biasing arrangement. The circuit component values are $V_{CC} = 20V$, $R_C = 2K$, $R_E = 0.1$ K, $R_1 = 100K$ and $R_2 = 5K$. 5M

UNIT III

6 a) Explain the operation of n-channel MOSFET with neat diagrams. 5M

b) Calculate the drain current of an nMOS transistor for $V_{GS} = 0V$, 1V and 2V with device parameters as $W = 5\mu m$, $L = 1\mu m$, $V_{DS} = 0.1V$, $V_{tn} = 1V$, $\mu_n C_{OX} = 25\mu A/V^2$. 5M

(OR)

7 a) Find the voltage gain of the common gate stage. 5M

b) Obtain the ON resistance of an nMOS transistor with $V_{GS} = 3V$, Vtn = 1V, $\mu_n C_{OX} = 25\mu A/V^2$, $W = 3\mu m$ and $L = 1\mu m$. 5M

UNIT-IV

8 .a) Explain the design of a basic current mirror. 5M

b) What is the need if biasing? Analyse a CS biasing circuit. 5M

(OR)

9. Analyse a different pair with small signal inputs and find the differential gain. 10M

Scheme of Evaluation

1. 10×1 – 10M

2. (a) Description of the three modes – 3M
   Carriers in the three to determine the concentration – 2M

   (b) n_0, p_0 → 1M
   expression for E_F – 2M
   value of E_F – 2M

3. (a) Five equations – 5×1 = 5M

   (b) equations of J_n and J_p – 2M
   finding the ratio $\frac{n}{p}$ – 3M

4. (a) Description of the breakdown mechanism – 5M

   (b) I–V relation in a diode – 1M
   $\frac{I_2}{I_1} = e^{(V_2 - V_1)/nV_T}$ – 2M
   value of n – 2M

5. (a) Simple circuits of three configurations – 2M
   Any three comparison – 3M

   (b) Circuit diagram – 1M
   quiescent current value – 2M
   V_{CEQ} – 2M

6. (a) Schematic diagram – 2M
   Description of the working principle – 3M

   (b) for $V_{GS} = 0V$ case → 1M
   for $V_{GS} = 1V$ case → 1M
   for $V_{GS} = 2V$ case → 3M

7. (a) Circuit diagram – 2M
   Small signal equivalent circuit along with the derivation of voltage gain – 3M (or) quantitative analysis of the large signal model to derive the voltage gain – 3M

   (b)

8. (a) Diagram showing the design concept – 1M
   Circuit diagram – 2M
   Description – 2M

8. (b) Need of biasing – 1M
   Circuit of CS biasing – 2M
   Explanation – 2M

9. Circuit of differential pair with small signal inputs – 2M
   Circuits for simplified analysis – 4M
   Derivation of the gain – 4M

Set

1. (a) Controlled addition of impurities to a crystal is called doping
(b) the transport of charges in a crystal as a result of under the influence of an electric field is called drift current.

(c) $P_{no} n_{no} = N_c N_v \exp\left(-\frac{E_g}{kT}\right) = n_i^2$

(d) 4

(e) Common Collector Configuration

(f) $\alpha = \frac{\beta}{1+\beta}$

(g) It is the minimum gate voltage at which the conduction just starts & the inversion region is formed.

(h) $\mu = g_m r_d$

(i) $-\frac{R_D}{R_S}$

(j) It provides a large resistance without changing the biasing value.

2 (a) the basic tenets of energy band model are
(i) Allowed energy states to electrons
(ii) Distribution of allowed states over energy ; $N(E)$
(iii) At any temperature T, under equilibrium only a fraction of allowed energy states are occupied. This fraction is given by $f(E,T)$, Fermi dirac function.

Allowed energy states to electrons

In the silicon crystal, as the atomic separation decreases, the $2N$ states of 3S orbital and $6N$ states of 3p orbital club together and split into two energy bands namely valence band ($4N$ states) and conduction band ($4N$ states).

The $4N$ electrons available occupy the valence band and the conduction band has empty states (at $T = 0K$).

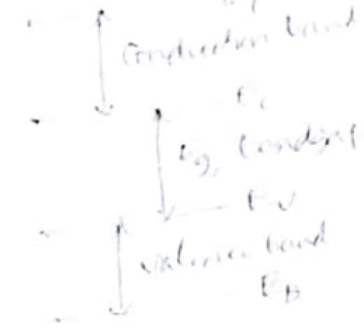
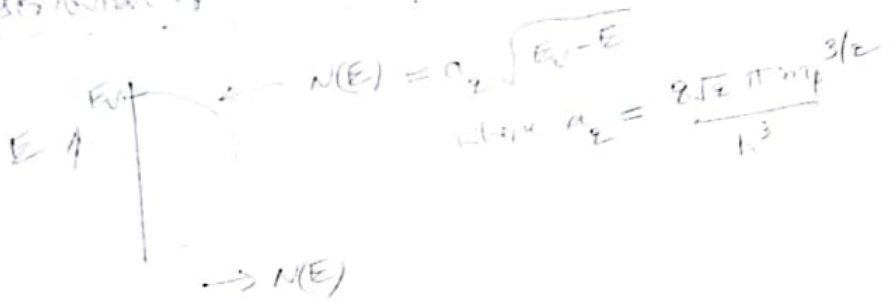
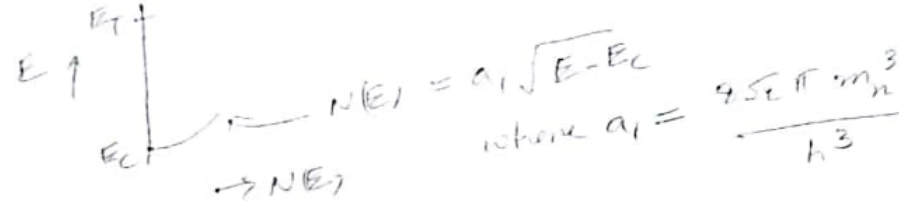


Fig. Energy band model of semiconductor

Distribution of allowed states over energy





Fermi Dirac function

$$f(E,T) = \frac{1}{1+\exp\left(\frac{E-E_f}{kT}\right)}$$ under equilibrium

where E_f = Fermi level

The information related to
- → allowed energy states
- → the density of states function
- → the fraction of occupied states at an energy E

Can be put together to derive an equation for the carrier concentration & intrinsic concentration.

$$n_i = \int_{E_c}^{E_T} N(E)\,dE\,f(E,T)$$

$$= \int_{E_c}^{E_T} a_1\sqrt{E - E_c}\left[\frac{1}{1+\exp\left(\frac{E-E_f}{kT}\right)}\right]dE$$

The approximations used to easily evaluate the above integral are (i) $E_T \to \infty$ (ii) Boltzmann approximation (iii) parabolic density of states approximation.

After integration

$$n_i = 2\left[\frac{2\pi m_n kT}{h^2}\right]^{3/2} \exp\left(\frac{E_f - E_c}{kT}\right)$$

$$= N_c \exp\left(\frac{E_f - E_c}{kT}\right)$$

The number of holes in the valence band at any temperature is given by

$$p_i = \int_{E_B}^{E_V} N(E)\,dE\,[1 - f(E,T)]$$

$$= \int_{E_B}^{E_V} a_2\sqrt{E_V - E}\left[1 - \frac{1}{1+\exp\left(\frac{E - E_f}{kT}\right)}\right] dE$$

The approximations used to easily calculate the above integral are (i) $E_B \to 0$ (ii) Boltzmann approximation (iii) parabolic density of states approximation

After integration

$$p_i = 2\left[\frac{2\pi m_p kT}{h^2}\right]^{3/2} \exp\left(\frac{E_f - E_V}{kT}\right)$$

$$= N_V \exp\left(\frac{E_f - E_V}{kT}\right)$$

2 (b) Given $n_i = p_i$ and $m_n = m_p$

$$n_i = p_i$$

$$2\left[\frac{2\pi m_n kT}{h^2}\right]^{3/2} \exp\left(\frac{E_c - E_f}{kT}\right) = 2\left[\frac{2\pi m_p kT}{h^2}\right]^{3/2} \exp\left(\frac{E_f - E_v}{kT}\right)$$

As $m_n = m_p$ that gives

$$2^{3/2} \exp\left(\frac{E_c - E_f}{kT}\right) = \exp\left(\frac{E_f - E_v}{kT}\right)$$

$$\exp\frac{2E_f - (E_c + E_v)}{kT} = 2^{-3/2}$$

$$\frac{2E_f - (E_c + E_v)}{kT} = \ln 2^{-3/2}$$

$$E_f = \frac{E_c + E_v}{2} - \frac{3}{4} kT \ln 2$$

$$= \frac{E_c + E_v}{2} - 0.0135 \text{ eV}$$

Fermi level E_f is below the centre of bandgap by 0.0135 eV.

3 (a)

Equation		Transport equation	
Carrier flux	Electrons	$J_n = q n \mu_n E + q D_n \frac{\partial n}{\partial x}$	$\frac{\partial}{\partial t}(\delta n) = \frac{1}{q}\frac{\partial J_n}{\partial x} + G' - \frac{\delta n}{\tau}$
	Holes	$J_p = q p \mu_p E - q D_p \frac{\partial p}{\partial x}$	$\frac{\partial}{\partial t}(\delta p) = -\frac{1}{q}\frac{\partial J_p}{\partial x} + G' - \frac{\delta p}{\tau}$
Electric flux		$E = -\frac{\partial \psi}{\partial x}$	$\frac{\partial E}{\partial x} = \frac{\rho}{\epsilon}$

3(b) J = total current density

$$J_n = \frac{3}{4} J$$

$$J_p = \frac{1}{4} J$$

$$v_n = 3 v_p$$

$$J_n = q n v_n$$

$$J_p = q p \cdot v_p$$

$$J = J_n + J_p$$

$$\frac{J_n}{J_p} = \frac{q n v_n}{q p v_p}$$

$$\frac{\left(\frac{3}{4} J\right)}{\left(\frac{1}{4} J\right)} = \frac{q n 3 v_p}{q p v_p}$$

$$3 = \frac{n}{p}(3)$$

$$n = p$$

$$\frac{n}{p} = 1.$$

4 (a) Avalanche breakdown

If the applied reverse bias increases, the field across the junction increases correspondingly.

Thermally generated carriers while traversing the junction acquire a large amount of kinetic energy from this field. As a result, the velocity of these carriers increase.

These electrons disrupt covalent bond by colliding with immobile ions and create new electron hole pairs.

These new carriers again acquire sufficient energy from the field and collide with other immobile ions thereby generating further electron hole pairs.

This process is cumulative in nature and results in generation of avalanche of charge carriers within a short time.

This mechanism of carrier generation is known as avalanche multiplication. This process results in flow of large amount of current at the same value of reverse bias.

4 (b) The current equation in a diode is

$$I = I_0 \left(e^{V/\eta V_T} - 1\right)$$

$$\simeq I_0 e^{V/\eta V_T} \quad \text{for } V > 3V_T$$

$$\therefore I_1 = I_0 e^{V_1/\eta V_T}$$

$$I_2 = I_0 e^{V_2/\eta V_T}$$

$$\frac{I_2}{I_1} = e^{(V_2 - V_1)/\eta V_T}$$

$$\ln\left(\frac{I_2}{I_1}\right) = \frac{V_2 - V_1}{\eta V_T}$$

$$\ln\left(\frac{20\times10^{-3}}{0.6\times10^{-3}}\right) = \frac{(500-400)10^{-3}}{\eta\,(26\times10^{-3})} \Rightarrow \eta = 1.097$$

Comparison of Transistor Configurations

Fig: Common base Configuration

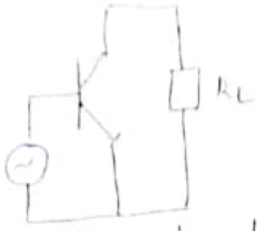


Fig: CE Configuration

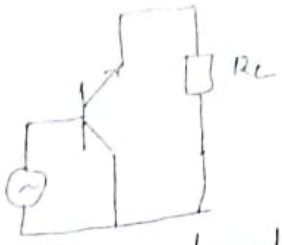
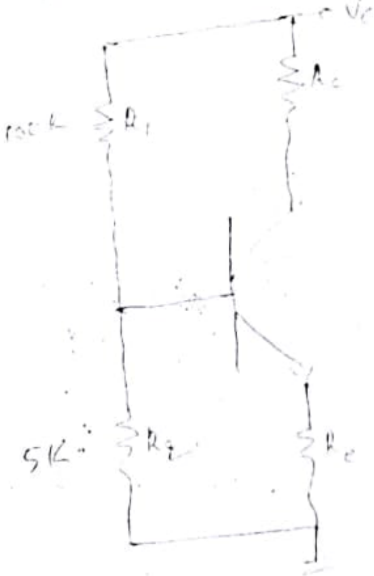


Fig: CC Configuration.

Parameter	CB Configuration	CE Configuration	CC Configuration
Input dynamic resistance	Very low (20Ω)	high (600Ω)	Very high (1MΩ)
output dynamic resistance	Very high (1MΩ)	low (73.5k)	Very low (21.6Ω)
voltage gain	3330	−3330	1
Current gain	less than unity (0.99)	high (−50)	high(≅1)

when $R_L = \infty$

3(b) Determine the quiescent currents and the collector to emitter voltage for a silicon transistor with $\beta = 50$ in the self biasing arrangement. The circuit component values are $V_{CC} = 20V$, $R_C = 2\,k\Omega$, $R_E = 0.1\,k\Omega$, $R_1 = 100\,k\Omega$, $R_2 = 5\,k\Omega$



$$V = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$= \frac{5}{100+5}(20)$$

$$= 0.952 \text{ Volt}$$

$$R = R_1 \| R_2$$

$$= \frac{(5K)(100K)}{5K + 100K}$$

$$= 4.76k$$

$$I_E = I_C + I_B$$

$$= \beta I_B + I_B$$

$$= (\beta + 1) I_B$$

$$0.952 = 4.76(10^3) I_B + (0.1\times10^3)(51) I_B$$

$$= (4760 + 5100) I_B$$

$$I_B = 96\,\mu A$$

$$I_C = \beta I_B = (50)(96)10^{-6}$$

$$= 4.8\,mA$$

$$I_E = 4.896\,mA$$

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$20 = (4.8)(10^{-3})(2\times10^3) + V_{CE} + (4.896)10^{-3}(0.1\times10^3)$$

$$20 = 9.6 + V_{CE} + 0.489$$

$$V_{CE} = 20 - 10.089$$

$$= 9.911\,V$$

Enhancement
MOSFET (Metal Oxide Semiconductor Field Effect Transistor):-

The n-channel MOSFET consists of a lightly doped p-type substrate into which two highly doped n+ regions are diffused, as shown in the following fig

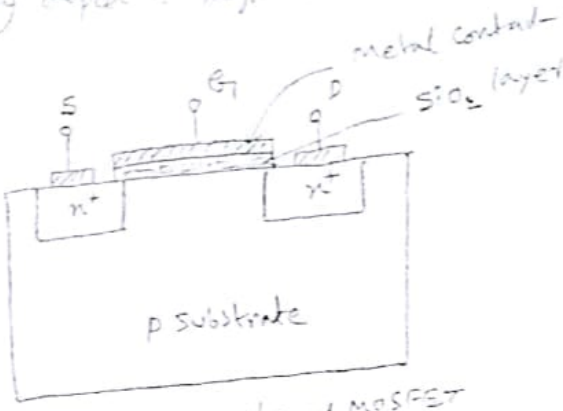


Fig: Enhancement n-channel MOSFET

The insulating layer of silicon dioxide is the reason why this device is called the insulated gate field effect transistor.

If a positive voltage is applied to the gate w.r.t the body of substrate, at the surface the material became like p type but small +ve voltage

If the gate voltage (+ve) is increased further, the surface first becomes space charge neutral and next it becomes negatively charged excessively, which means that the surface becomes n type for large values of gate voltage. Thus is called inversion of p-type material became n-type at the surface with the applied +ve gate voltage.

This is shown in the following diagram.

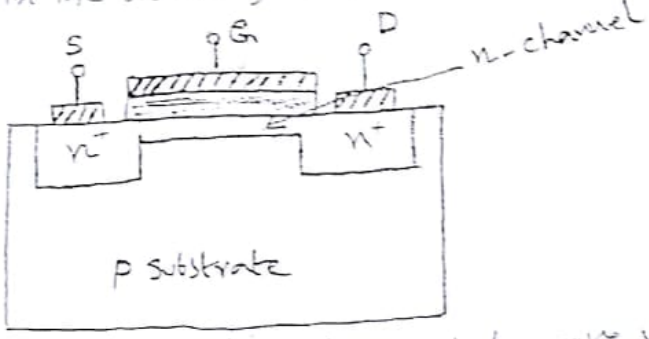


Fig: Schematic of MOSFET when gate is applied a +ve voltage w.r.t substrate.

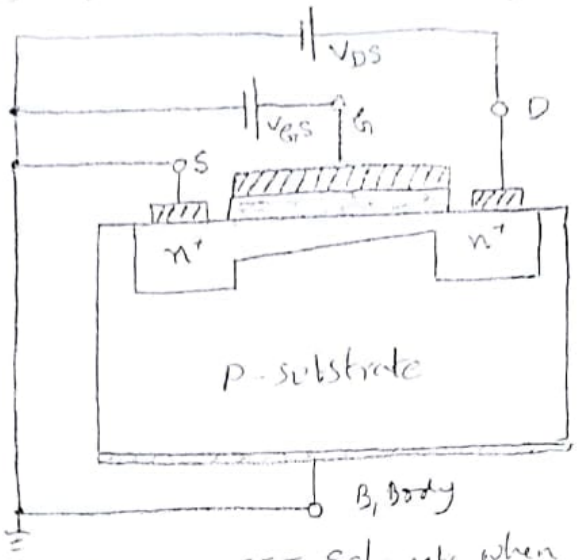
The depth of the conductive channel can be varied by varying the gate voltage.

The gate voltage that is necessary to make the surface of the semiconductor as conductive as the substrate or bulk or body is called threshold voltage (V_T).

(or)

Threshold voltage is that gate voltage that will permit a certain amount of current to flow from source to drain.

As the drain current is enhanced by the +ve gate voltage, this device is called an enhancement type MOSFET.



$V_{GD} = V_{GS} - V_{DS}$

Fig: MOSFET Schematic when $V_{DS} = V_{GS} - V_T$

When only the threshold voltage is applied, the channel gets formulated. The channel depth is dependent upon the excess voltage over and above V_T.

Initially the depth of the channel is dependent on $V_{GS} - V_T$. If V_{DS} is increased from zero, the depth of the channel at the drain end decreases. This is shown in the above fig.

If V_{DS} is increased to a value $V_{GS} - V_T$ then the channel gets closed at the drain end & the channel is pinched off at the drain end.

The characteristics of MOSFET are shown below.

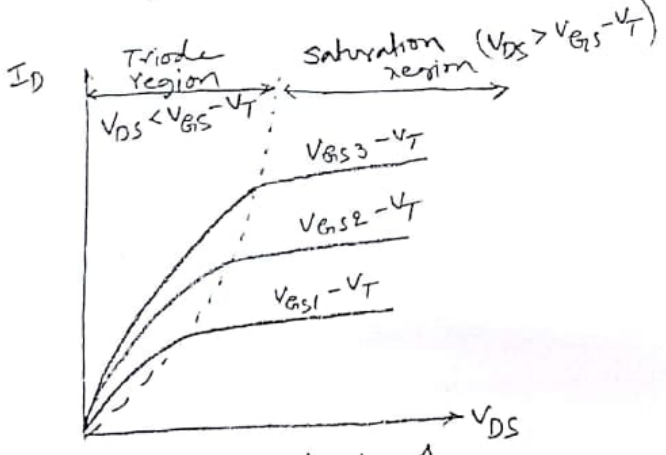


Fig: Drain characteristics of MOSFET

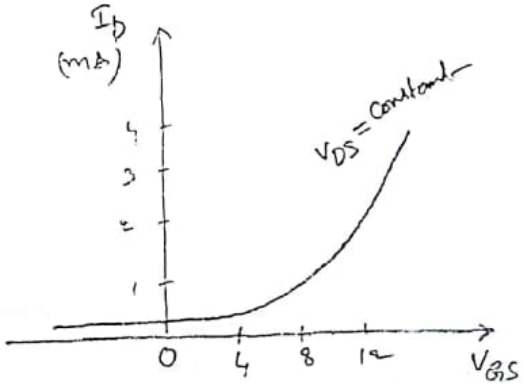


Fig: Transfer characteristic.

In the Saturation region, $I_D = K(V_{GS} - V_T)^2$ where K = Constant

In the triode region, $I_D = 2K\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$

6 (b)

For $V_{GS} = 0V < V_{th} = 1V$, channel does not form, $I_D = 0$

For $V_{GS} = 1V = V_{th}$, channel does not form, $I_D = 0$

For $V_{GS} = 2V > V_{th} = 1V$, channel form and its equation of I_D is

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$= 25 \times 10^{-6} \frac{5}{1} \left[(2-1)(0.1) - \frac{(0.1)^2}{2} \right]$$

$$= 11.875 \mu A$$

7(a)

Voltage gain of a Common gate stage

(a) (b)

Fig: (a) Common gate stage with direct coupling at input
(b) CG stage with capacitive coupling at input

A Common gate stage senses the input at the source and produces the output at the drain.

The gate is connected to a dc voltage to establish proper operating condition.

First consider the large signal behavior of the circuit shown in fig a.

For simplicity, assume that V_{in} decreases from a large positive value. Also $\lambda = 0$.

For $V_{in} \geq V_b - V_{TH}$, M_1 is OFF and $V_{out} = V_{DD}$

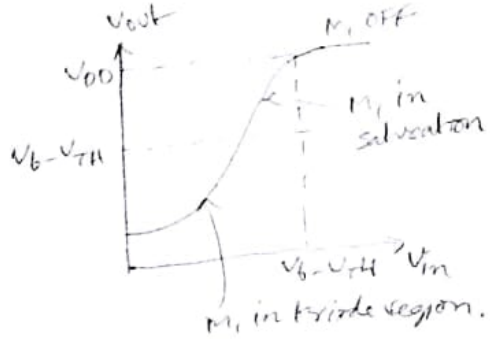


Fig: Common gate input-output characteristic

For lower values of V_{in},

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 \quad \text{if } M_1 \text{ is in saturation}$$

As V_{in} decreases, so does V_{out}, eventually driving M_1 into the triode region if

$$V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D = V_b - V_{TH}$$

The input-output relation is shown in the above fig, illustrating the case in which M_1 enters the triode region as V_{in} decreases.

In the region where M_1 is saturated,

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D$$

obtaining a small signal gain of

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})\left(-1 - \frac{\partial V_{TH}}{\partial V_{in}}\right)R_D$$

Since $\frac{\partial V_{TH}}{\partial V_{in}} = \frac{\partial V_{TH}}{\partial V_{SB}} = \eta$, we have $\frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox}\frac{W}{L}R_D(V_b - V_{in} - V_{TH})(1+\eta)$

$$= g_m(1+\eta)R_D$$

Interestingly, the body effect increases the equivalent transconductance of the stage.

Q4.)

Given NMOS Transistor

$V_{GS} = 3V$,

$V_{th} = 1V$

$\mu_n C_{ox} = 25 \mu A/V^2$

$W = 3\mu m$

$L = 1\mu m$

$$\frac{\partial I_D}{\partial V_{DS}} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th}) - V_{DS}\right]$$

$$\left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{DS} \to 0} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})$$

$$r_{H,ON} = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th})}$$

$$= \frac{1}{25 \times 10^{-6}\left(\frac{3}{1}\right)(3-1) \cdot \frac{A}{V^2} \frac{\mu m}{\mu m} V}$$

$$= 6.67 K\Omega$$

2(a)

Design of a basic current mirror:

The design of current sources in analog circuits is based on "copying" currents from a reference, with the assumption that an already defined current source is already available.

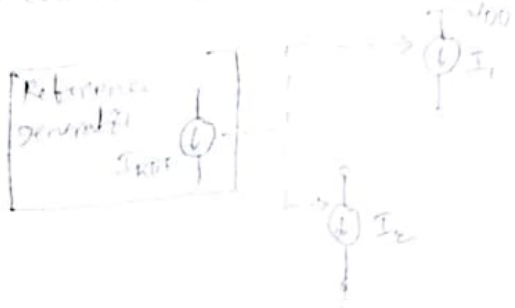


Fig: Use of a reference to generate various currents

Two identical MOS devices that have equal gate source voltages and operate in saturation carry equal currents (if $\lambda = 0$)

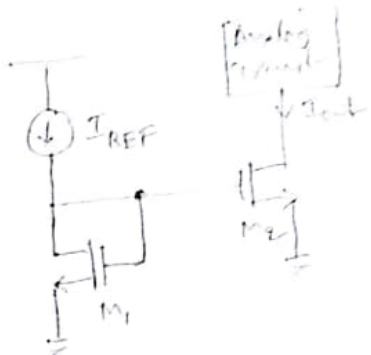


Fig: Basic current mirror

The structure consisting of M_1 and M_2 in the above fig is called a "current mirror". In the general case, the transistors need not be identical. Neglecting the channel length modulation, we can write

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2$$

obtaining $$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

Kits

Need of biasing

All amplifier stages must be properly biased so that, in the absence of the input signal, each transistor carries the required current and establishes the necessary terminal voltages.

The current establishes the transconductance and output resistance of the transistor while the terminal voltages determine the headroom and hence the allowable voltage swings.

CS biasing: Simple CS stage

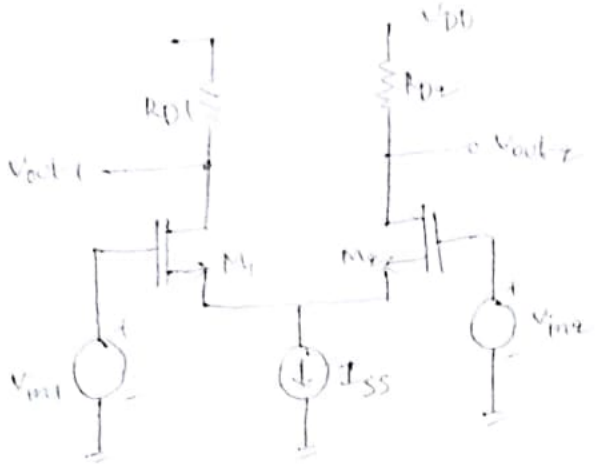
Fig: CS biasing: simple CS stage

V_{in} is coupled capacitively to establish a high impedance at V_B so that X has the same dc voltage as V_B and the same signal voltage as V_{in}

Note that C_B and R_B form a high pass filter, select $\frac{1}{2\pi R_B C_B}$ lower than the lowest input frequency so that the ac gain from V_{in} to V_x is near unity in the frequency range of interest.

9.

Analysis of a differential pair with small signal inputs to find the differential gain

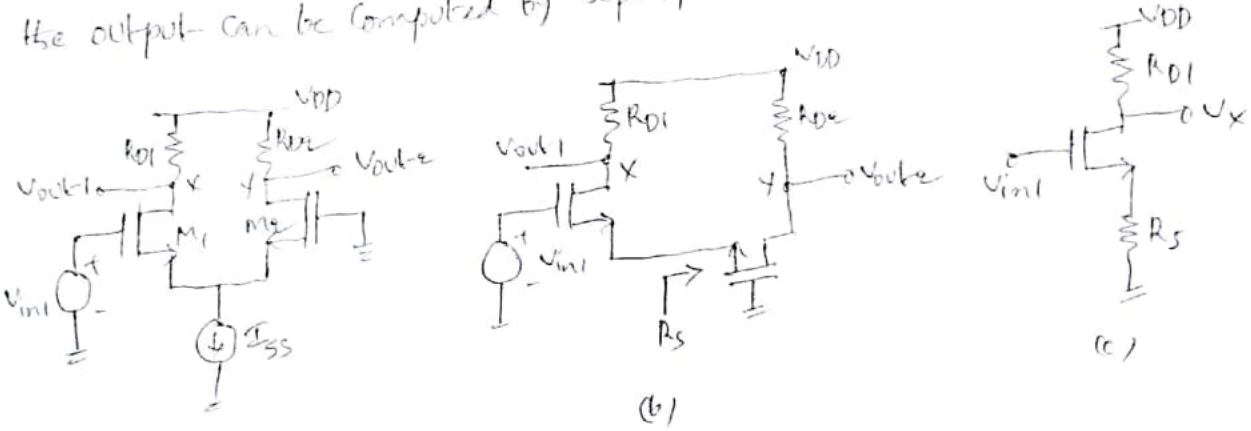


First Differential pair with small signal inputs

Assume that M_1 and M_2 are saturated

Assume that $R_{D1} = R_{D2} = R_D$

The above circuit is driven by two independent signals. Thus, the output can be computed by superposition.



(a) (b) (c)

Fig 2(a) Differential pair sensing one input signal

(b) circuit of (a) viewed as a CS stage degenerated by M_2

(c) equivalent of circuit (b).

Let us set V_{in2} to zero and find the effect of V_{in1} at X and Y (Fig 2(a)).

To obtain V_X, note that M_1 forms a common source stage with a degeneration resistance equal to the impedance seen looking into the source of M_2 (Fig 2(b)).

Neglecting the channel length modulation and body effect, $R_S = \frac{1}{g_{m2}}$ (Fig 2(c)) and

$$\frac{V_Y}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

To calculate V_Y, note that M_1 drives M_2 as a source follower and replace V_{in1} and M_1 by a thevenin equivalent (bias)

Fig 3: Replacing M_1 by a thevenin equivalent

the thevenin voltage $V_T = V_{in1}$ and

the resistance $R_T = \frac{1}{g_{m1}}$

Hence M_2 operates as a common gate stage, exhibiting a gain of

$$\frac{V_Y}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$

If follows from the earlier two equations that the overall voltage gain for V_{in1} is

$$(V_X - V_Y)\Big|_{\text{due to } V_{in1}} = \frac{-2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in1}$$

$$= -g_m R_D V_{in1} \quad \text{when } g_{m1} = g_{m2} = g_m$$

By virtue of symmetry, the effect of V_{in2} at X and Y is identical to that of V_{in1} except for a change in the polarities

$$(V_X - V_Y)\Big|_{\text{due to } V_{in2}} = g_m R_D V_{in2}$$

By superposition $\frac{(V_X - V_Y)_{tot}}{V_{in1} - V_{in2}} = -g_m R_D$