Set-2

Solutions

18EI 303

Digital Electronics.

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Set-II Solutions.

1 (a) Bubble OR Gate is nothing But NAND Gate.

Truth table.

A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

(b). $(25)_{10} = (\quad)_{Gray}$

16 8 4 2 1
1 1 0 0 1

Binary of $(25)_{10} = (11001)_2$

$(11001)_2 = (10101)_{Gray}$

(c) For each pair of elements x, y in Boolean Algebra.

(a) $\overline{(x+y)} = \bar{x}\cdot\bar{y}$ (b) $\overline{xy} = \bar{x}+\bar{y}$

(d) -17 in Signed 1's complement form.

16 8 4 2 1
1 0 0 0 1
0 1 1 1 0

1 01110

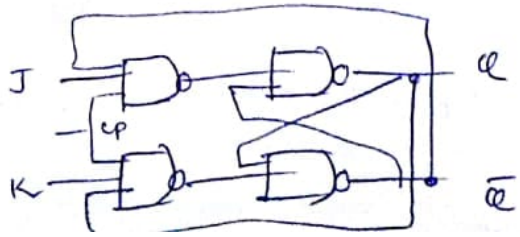
↓ sign bit, ~ magnitude

(e). $f(x,y,z) = \bar{x}\bar{y}z + xz + yz = z[\bar{x}\bar{y} + x + y]$

$= z[(x+y)+\bar{x}][x+y+\bar{y}] = z\cdot[(1+y)][1+x] = z.$

(f). minterms: product terms that have this property of all variables appearing exactly once are called min terms, Max terms: Sum terms that have this property of all variables appearing exactly once are called max terms.

(g)



JK flip flop

(h) $N < 2^{n_{min}}$

$10 < 2^{n_{min}} \Rightarrow$ $n_{min} = 4$

(i) In PLA both AND array & OR array are programmable

In PROM AND array is fixed OR array is programmable

(j) Synchronous Counters: In Synchronous Counters Clock pulses Common to the all the flip-flops

In Asynchronous Counters Output of one Flip-flop acts as Clock to the next flip-flop.

Unit-I

2 (a) (i) $(1256)_8 = (x)_2$

$x = (001\ 010\ 101\ 110)_2$

(ii) $(42)_5 = (x)_7$.

$\Rightarrow (x)_7 = 4 \times 5^1 + 2 \times 5^0 = 20 + 2 = (22)_{10}$

$(22)_{10} = (x)_7 = (31)_7$.

7 | 22
3 - 1

$\therefore x = 31$

(iii) $(10011.11)_2 = (x)_{16}$

$(0001\ 0011 . 1100)_2 = (x)_{16}$

$\therefore x = 13.C$

(b) $(295) = (100\ 100\ 11\ 1)$ Binary.

$(295) = (0010\ 1001\ 0101)$ BCD

$(295) = (0101\ 1100\ 1000)$ Excess-3

$(295) = (0110\ 1111\ 1011)_{8\,4\,-2\,-1}$

$(295) = (0010\ 1010\ 0101)_{7\,4\,2\,1}$

OR

3 (a). Given $x\bar{y} + \bar{x}y = z$, Show that $x\bar{z} + \bar{x}z = y$

$z = x \oplus y \qquad \bar{z} = x \odot y$

$\bar{x}(\bar{x}y + x\bar{y}) + x \cdot (xy + \bar{x}\bar{y})$

$= \bar{x}\cdot\bar{x}y + x\bar{x}\bar{y} + x\cdot xy + x\cdot\bar{x}\bar{y}$

$= \bar{x}y + 0 + xy + 0 = \bar{x}y + xy = y(x+\bar{x})$

$= y.$

(b). For any x in Boolean Algebra.

(a) $x+x = x$. (b) $x\cdot x = x$.

Proof: (a). $(x+x) = (x+x)\cdot 1$ by P-2(b)

$= (x+x)(x+\bar{x})$ by P-5(a)

$= x + x\bar{x}$ by P-4(b)

$= x + 0$ by P-5(b)

$= x$ by P-2(a).

(b). $x\cdot x = x\cdot x + 0$ by P-2(a)

$= xx + x\bar{x}$ by P-5(b)

$= x\cdot(x+\bar{x})$ by P-4(b)

$= x\cdot 1$ by P-5(a)

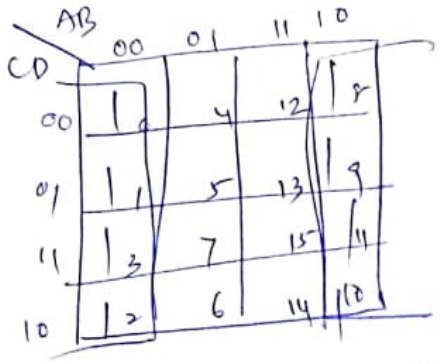
$= x$ by P-2(b)

Unit - II

4 (a).

K-Map:

$f(A,B,C,D) = \sum m\,(0,1,2,3,8,9,10,11)$.



One 8-Box Combination

Simplified Sop expression

$f(A,B,C,D) = \overline{B}$

4 (b) Design of 3-bit Binary - Gray code Converter

Step: 1 No. of i/p's: 3, No. of o/p's: 3.

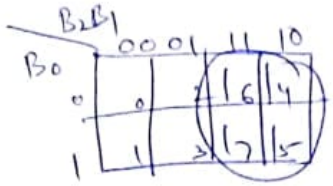
Step: 2 B_2, B_1, B_0 are i/p's G_2, G_1, G_0 are o/p's

Step: 3 Truth table

B_2	B_1	B_0	G_2	G_1	G_0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

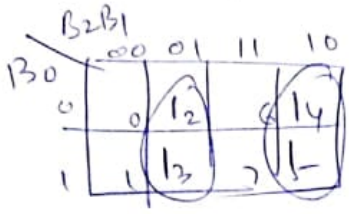
Step: 4

$G_2 = f(B_2, B_1, B_0) = \Sigma m(4,5,6,7)$



$G_2 = B_2$

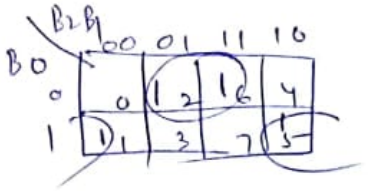
$G_1 = f(B_2, B_1, B_0) = \Sigma m(2,3,4,5)$



$\bar{B_2} B_1 + B_2 \bar{B_1}$

$G_1 = B_2 \oplus B_1$

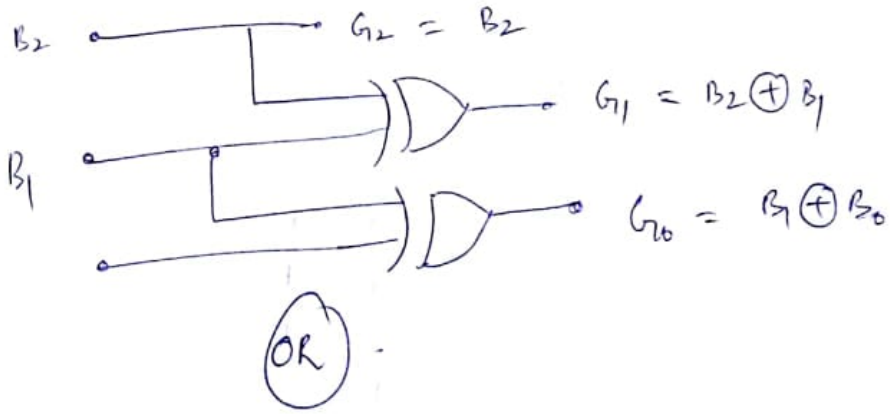
$G_0 = f(B_2, B_1, B_0) = \Sigma m(1,2,5,6).$



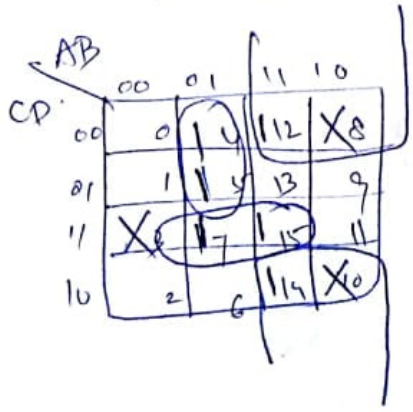
$G_1 = B_1 \bar{B_0} + \bar{B_1} B_0$

$= B_1 \oplus B_0$

Step: 5 Logic diagram:

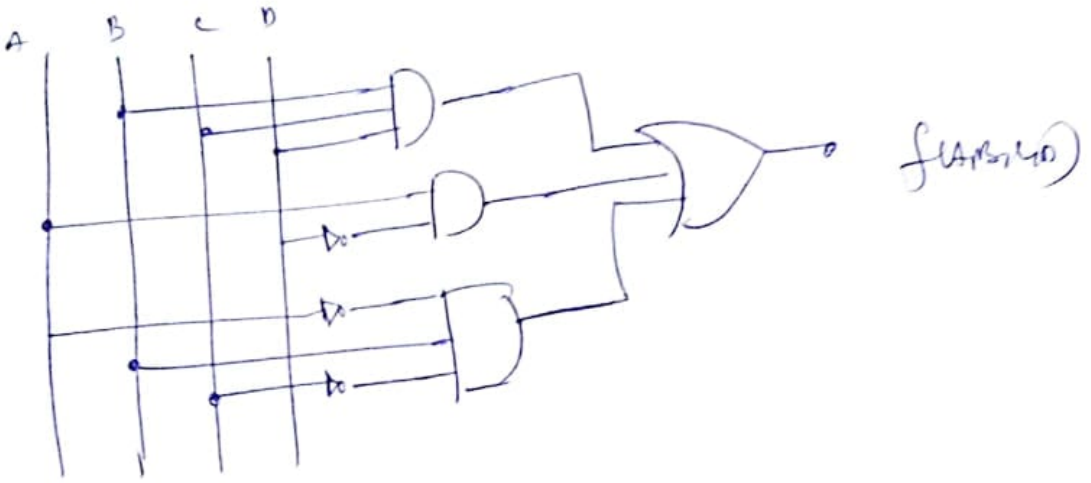


5(a). $f(A,B,C,D) = \Sigma m(4,5,7,12,14,15) + \Sigma d(3,8,10)$



SOP Expression: $A\bar{D} + BC + \bar{A}B\bar{C}$

~~5(b)~~ Logic diagram:



5(b) Design of Full-Subtractor ckt

Step:1 No. of inputs: 3. No. of o/p's: 2

Step:2 x, y, z are i/p s, c are o/p's

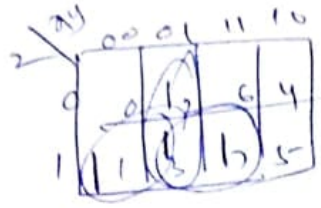
Step:3 Truth table

x	y	z	s	c
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Step:4 $S = f(x,y,z) = \Sigma m(1,2,4,7)$

$= x \oplus y \oplus z$.

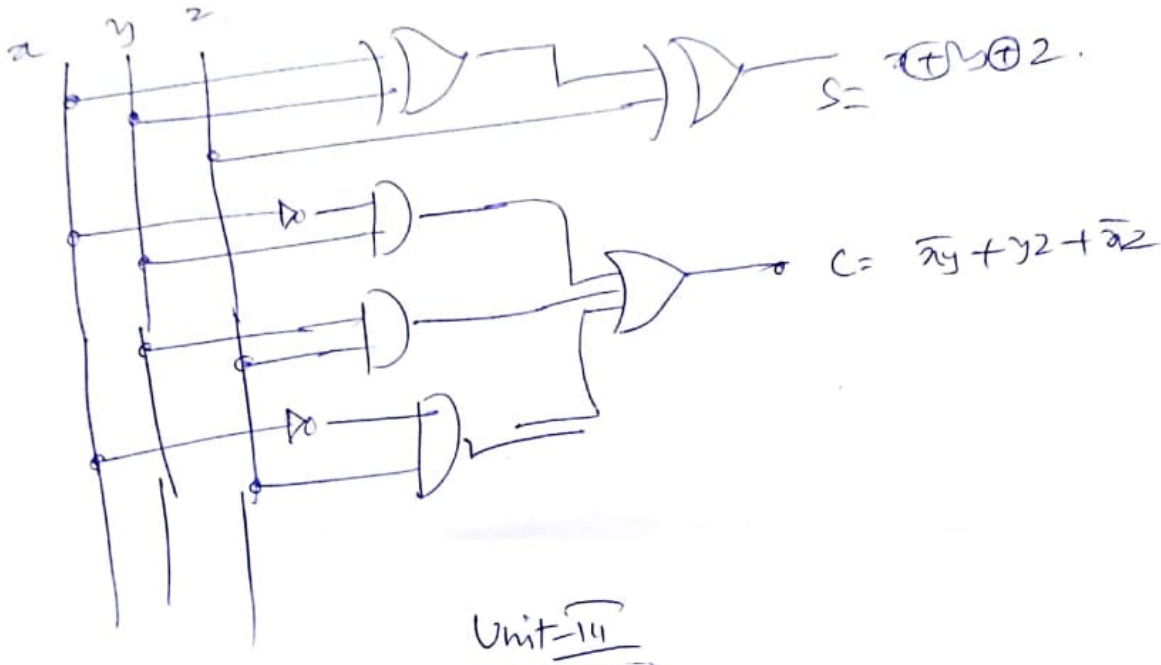
$C = f(x,y,z) = \Sigma m(1,2,3,7)$



$C = \bar{x}y + \bar{x}z + yz$

$= \bar{x}y + yz + \bar{x}z$

Step: 5 Logic diagram.



Unit-III

6 (a) Decoder: Combinational ckt, that converts Binary information from the n coded i/ps to a max of 2^n unique o/p's.

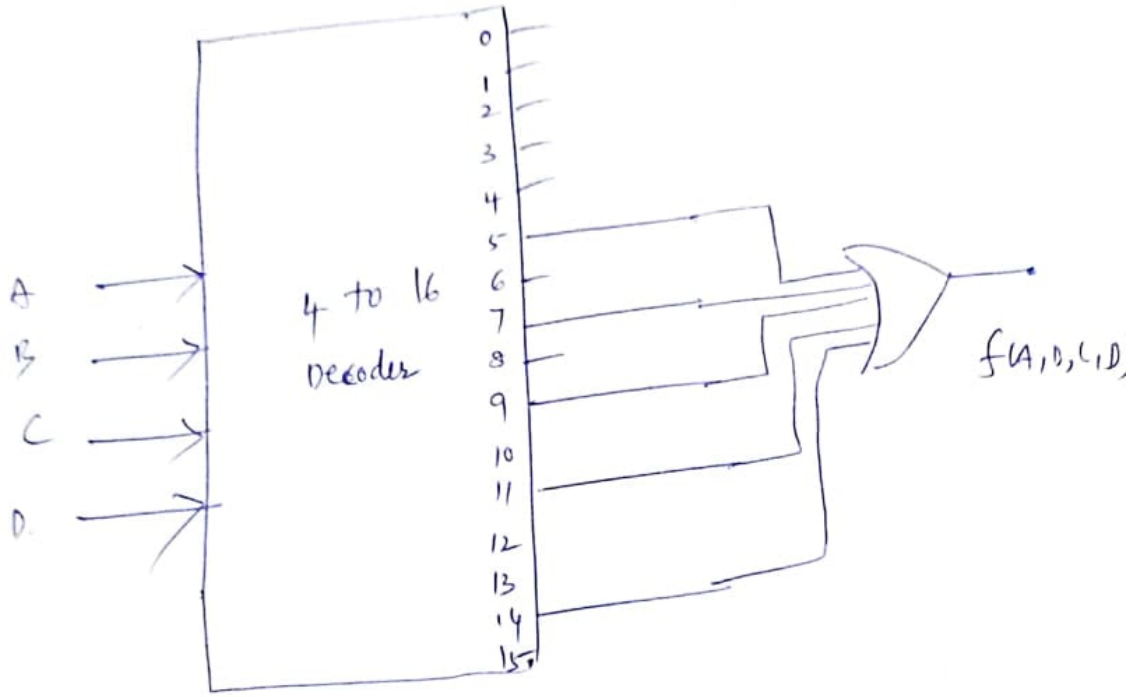
$f(A,B,C,D) = \bar{A}BD + A\bar{B}D + ABC\bar{D}$

$\bar{A}BXD$	$A\bar{B}XD$	$ABC\bar{D}$
0101	9 1001	14 1110
0111	11 1011	

$= \Sigma m(5,7,9,11,14)$

Boolean function implementation using Decoder

Required decoder 4 to 16 decoder



6

(5) Magnitude Comparator:

A magnitude Comparator is a Combinational Logic CKt that compares the two n-bit numbers A and B determines whether A>B, A=B or A<B.

Design of 2-bit Magnitude Comparator

A = $A_1 A_0$ B = $B_1 B_0$ are two 2-bit numbers.

Case-I. A=B Condition

A=B when $A_1=B_1$ and $A_0=B_0$.

∴ The o/p logic expression for A=B Condition

$E = E_1 E_0$.

E_1 = A_1, B_1 ⇒ D — E_1 E_0 = A_0, B_0 ⇒ D — E

Case-II

A>B Condition.

A > B when and only when

$A_1 > B_1$

(or)

$A_1 = B_1$, $A_0 > B_0$.

∴ O/P Expression for this condition.

$A_1\bar{B}_1 + E_1 \cdot A_0\bar{B}_0$

Case-III A<B Condition.

A<B when and only when.

$A_1 < B_1$

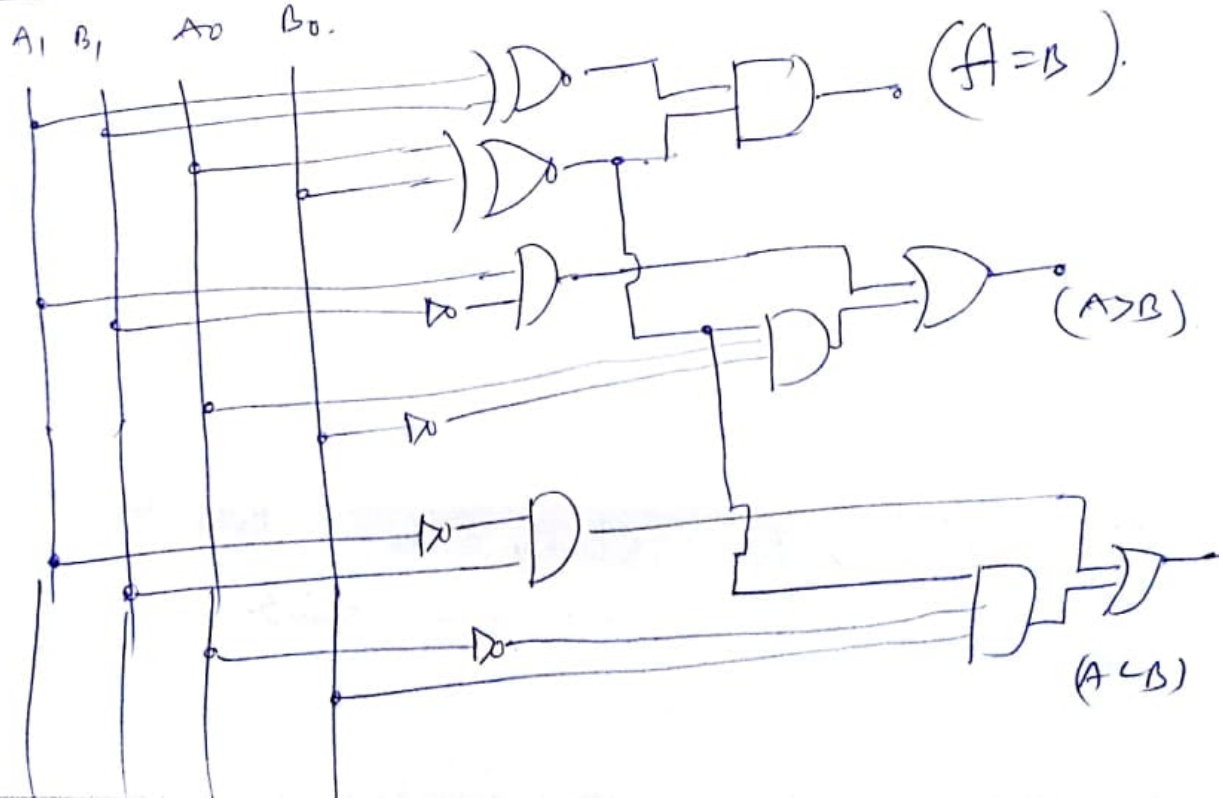
(or).

$A_1 = B_1$ and $A_0 < B_0$

∴ O/P expression for this condition.

$\bar{A}_1B_1 + E_1 \cdot \bar{A}_0B_0$.

Logic diagram.

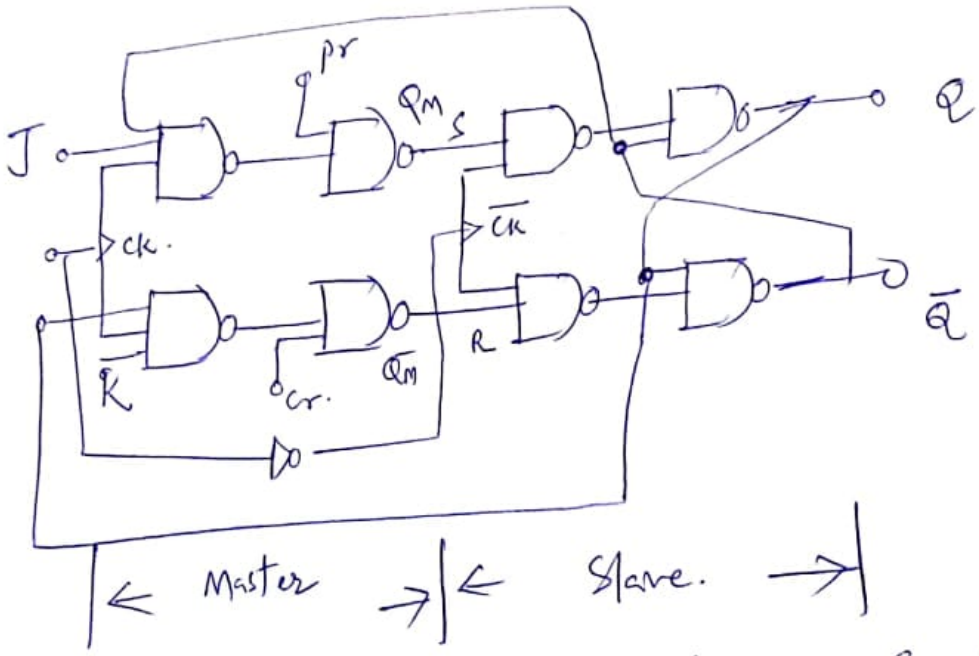


7(a)

Race-around Condition in J-K Flip-flop

In JK Flip-flop as long as Clock is high for the input conditions J & K equals to, the o/p changes or complements its from 1 → 0 and 0 → 1. This is called toggling o/p or Uncontrolled Changing (or) racing Condition

The above problem is eliminated using Master-Slave JK Flip-flop shown below



When pr=1 cr=1 CK=1 Master is enabled. and operation follows the JK F'F truth table

Further more CK=0, the Slave SR Flip-flop is inhibited, so that Q_n is invariant for the pulse duration t_p, Clearly the Race-around difficulty is circumvented with this.

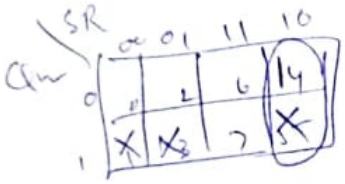
After the pulse passes $C_K = 0$, so that Master is inhibited and $\bar{C}K = 1$, which causes the Slave to be enabled. The Slave is SR flip-flop. If $S = Q_M = 1$ and $R = \bar{Q_M} = 0$ then $Q = 1$ and $\bar{Q} = 0$ Similarly $S = Q_M = 0$ and $R = \bar{Q_M} = 1$ then $Q = 0$ & $\bar{Q} = 1$.

7(b) Conversion of J-K Flip-flop into SR flip-flop.

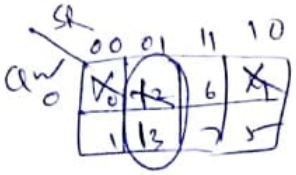
Q_n	Q_{n+1}	S	R	Q_n	J	K
0	0	0	X	0	0	X
0	1	1	0	0	1	X
1	0	0	1	1	X	1
1	1	X	0	1	X	0

$J = f(S, R, Q_n) = \Sigma m(4) + \Sigma d(3, 1, 5)$

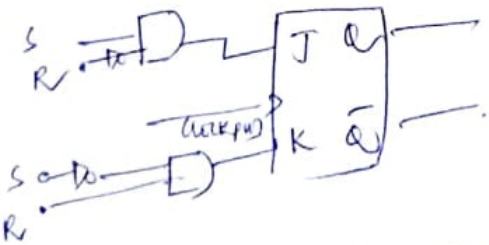
$K = f(S, R, Q_n) = \Sigma m(3) + \Sigma d(0, 2, 4)$.



$J = S\bar{R}$



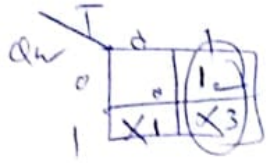
$K = \bar{S}R$



Conversion of J-K flip flop into T flip-flop

Q_n	Q_{n+1}	T	Q_n	J	K
0	0	0	0	0	X
0	1	1	0	1	X
1	0	1	1	X	1
1	1	0	1	X	0

$J = f(T, Q_N) = \Sigma m(2) + \Sigma d(1,3)$

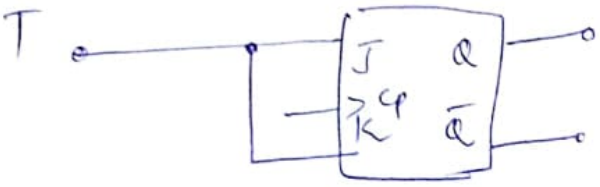


$J = T.$

$K = f(T, Q_N) = \Sigma m(3) + \Sigma d(0,2)$

$K = T.$

Logic diagram:



Unit - IV

8. Design of BCD Synchronous Counter

BCD counter means Mod-10 Counter

No. of flip-flops required

$N < 2^m$

$m_{min} = 4.$

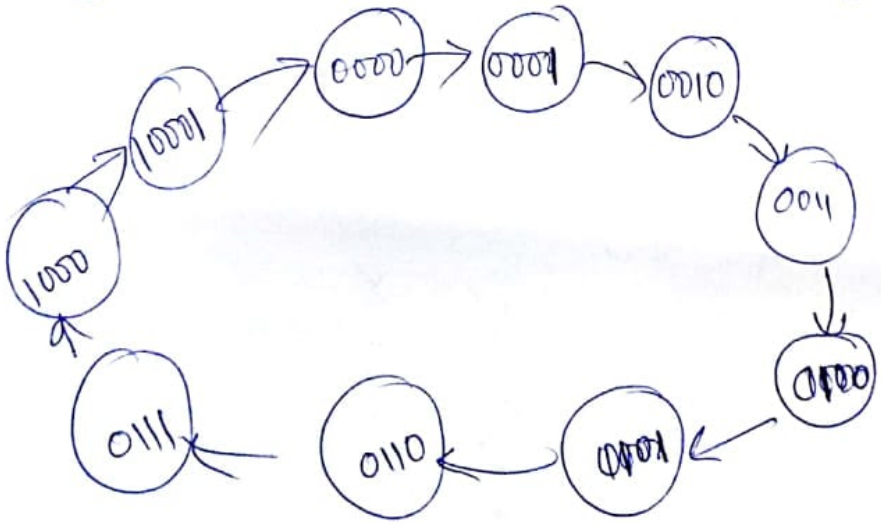
Type of flip-flop

JK

J_A, K_A, J_B, K_B, J_C

J_D K_D.

State diagram:



present state				Next state				J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

Permanent Don't Cares:

Unused states.

10, 11, 12, 13, 14, 15

$J_A = \Sigma m(7) + \Sigma d(8, 9, 10 \text{ to } 15)$

$J_B = \Sigma m(3) + \Sigma d(4, 5, 6, 7, 10 \text{ to } 15)$

$J_C = \Sigma m(1, 5) + \Sigma d(2, 3, 6, 7, 10 \text{ to } 15)$

$J_D = \Sigma m(0, 2, 4, 6, 8) + \Sigma d(1, 3, 5, 7, 9 \text{ \& } 10 \text{ to } 15)$

$K_A = \Sigma m(9) + \Sigma d(0 \text{ to } 7 \text{ \& } 10 \text{ to } 15)$.

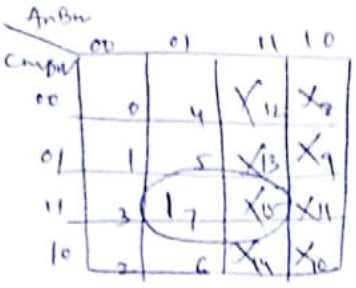
$K_B = \Sigma m(7) + \Sigma d(0, 1, 2, 3, 7, \text{ \& } 10 \text{ to } 15)$

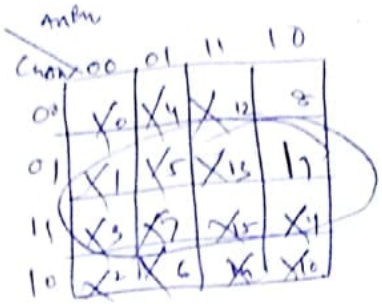
$K_C = \Sigma m(3, 7) + \Sigma d(0, 1, 4, 5, 8, 9 \text{ \& } 10 \text{ to } 15)$

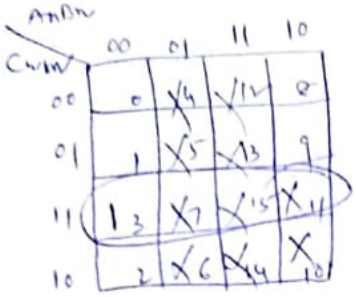
$K_D = \Sigma m(1, 3, 5, 7, 9) + \Sigma d(0, 2, 4, 6, 8 \text{ \& } 10 \text{ to } 15)$

$K_A = D_n$

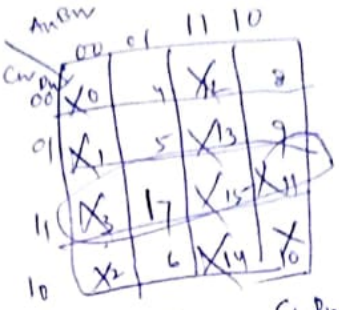
$J_A = B_n C_n D_n$



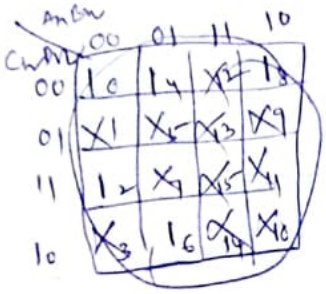




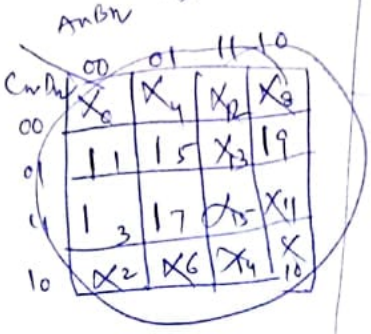
$J_B = C_n D_n$



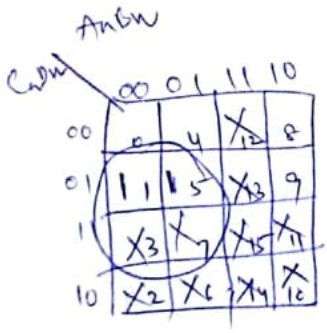
$K_B = C_n D_n$



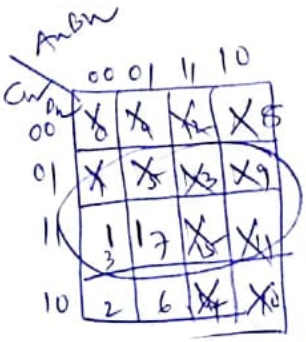
$J_D = 1$



K_D $K_D = 1$

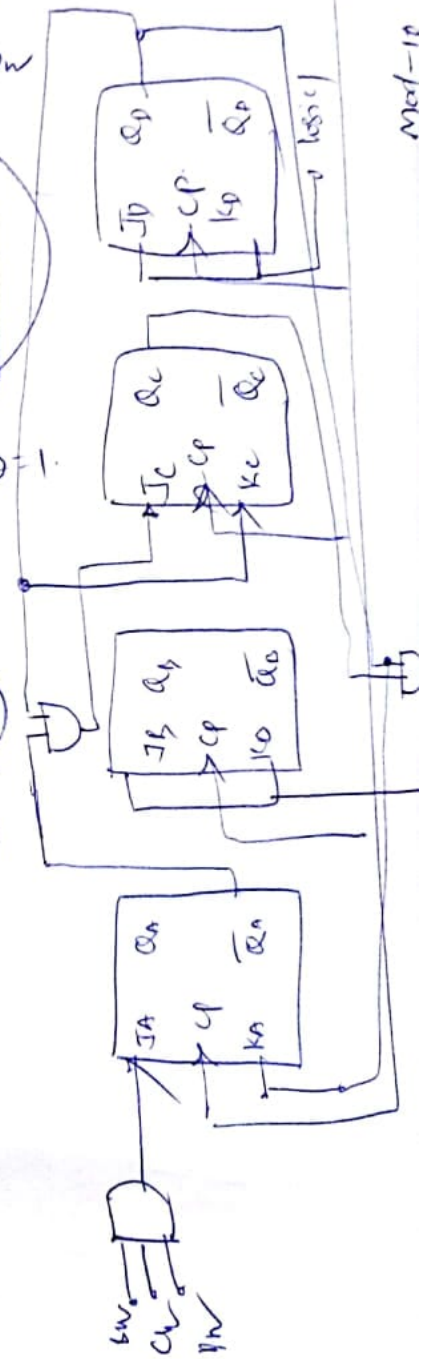


$J_C = \bar{A}_n D_n$



$K_C = D_n$

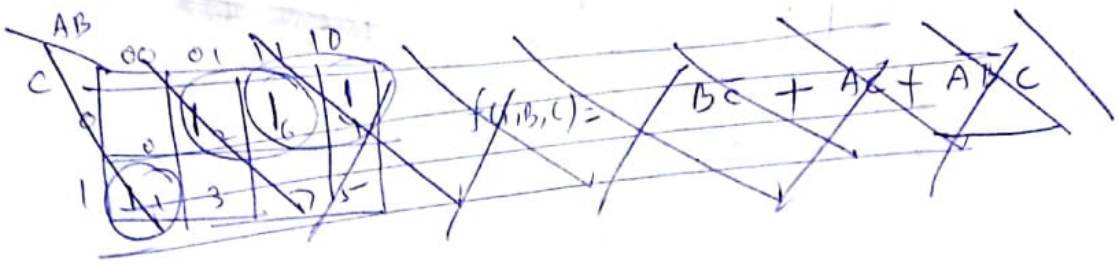
Draw the logic diagram:



9(a).

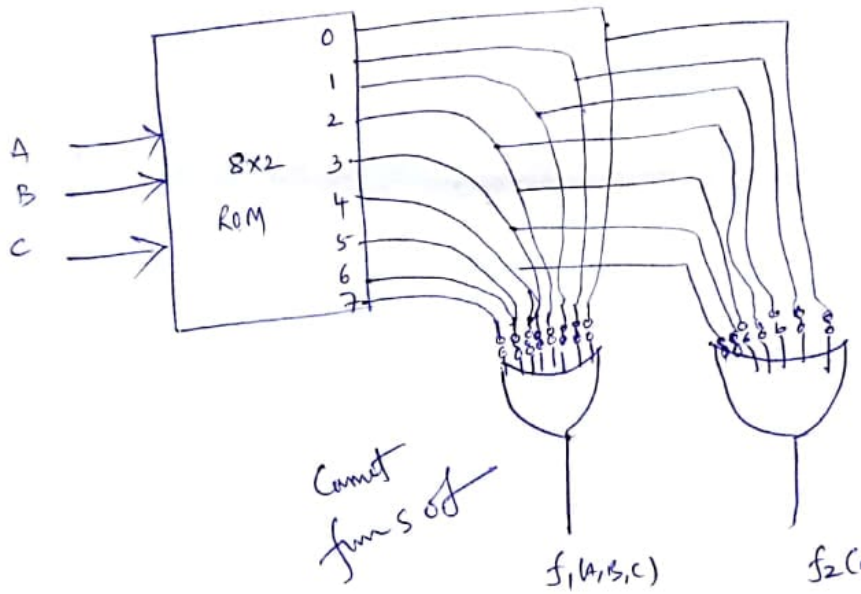
Implement Boolean function

$f(A,B,C) = \Sigma m(1,2,4,6)$. using PROM



Size of the ROM Here $n = 3$.

$2^n \times m$ $2^3 \times 2 =$ 8×2 ROM



Canonical forms of

$f_1(A,B,C)$ $f_2(A,B,C)$.

1, 2, 4, 6 0, 1, 6, 7

9(b)

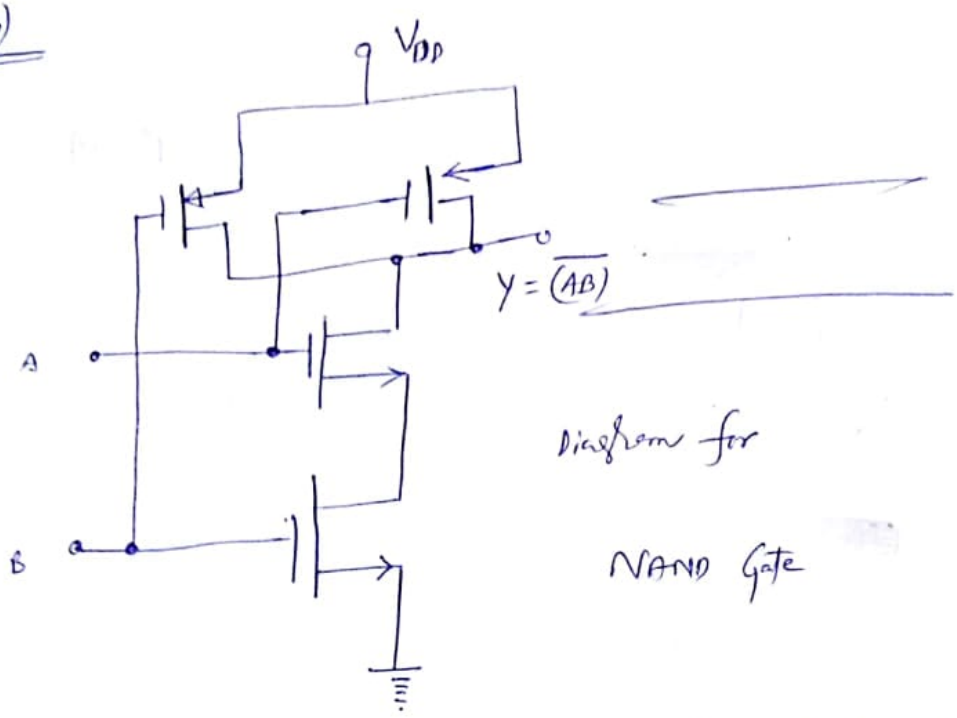


Diagram for NAND Gate

(1) A 2-i/p NAND Gate consists of two p-type units in parallel & 2 n-type units in series

(2) If all inputs are high, both p-Channel transistors turn off and both n-channel transistors turn on

(3) The o/p has a low impedance to ground and produces a low state

(4) If any input is low, the associated n-channel transistor is turned off and the associated p-Channel transistor is turned on.

(5) The o/p is coupled to the V_{DD} and goes to the high state