14IT502

Hall Ticket Number:

III/IV B.Tech (Regular/Supplementary) DEGREE EXAMINATION

November, 2019 **Information Technology**

Fifth Semester **Compiler Design**

Time: Three Hours **Maximum :** 60 Marks

Answer Question No.1 compulsorily. (1X12 = 12 Marks)

Answer ONE question from each unit. (4X12=48 Marks)

1 Answer all questions (1X12=12 Marks)

a) Define assembler.
b) Define symbol table.
c) Define lexeme.
d) List the possible actions can make in shift-reduce parsing.
e) Define reduce/reduce conflict.
f) Define syntax-directed definition.
g) Define control stack.
h) Define activation record.
i) Define call by reference.
j) Define register allocation.
k) Define basic block
l) Define flow graph.

UNIT I

2 a) Illustrate phases of compiler with an assignment statement a=(b+c)*(b+c)*2 8M

b) Find whether the following grammar is LL(1) or not 4M
S-> abSa|aaAb
A->baAb|b

(OR)

3 a) Find the predictive parser for the following grammar and parse the sentence id+id*id 8M
E→ E+T|T
T→ T*F|F
F→ (E)| id

b) Differentiate the lexical analysis with parsing. 4M

UNIT II

4 a) Construct the SLR parsing table for the grammar 8M
S->(L)|a
L->L,S|S

b) Construct Syntax tree for b + 5 - a 4M

(OR)

5 a) Construct the LALR parsing table for the grammar 8M
S->L=R|R
L->*R|id
R->L

b) Illustrate the construction of input/output translator with Yacc. 4M

UNIT III

6 a) Illustrate stack and heap storage allocation strategies for strings and records. 8M

b) Demonstrate the representing of scope information. 4M

(OR)

7 a) Explain register assignment and allocation with an example. 4M

b) Demonstrate different data structures to symbol tables 8M

UNIT IV

8 a) Describe simple target machine model. 6M

b) Demonstrate determining the liveness and next-use information for each statement in a basic block. 6M

(OR)

9 a) Illustrate back patching. 4M

b) Illustrate the issues in design of code generator 8M

Compiler design schema			
1	Answer all questions		(1X12=12 Marks)
	a)	Define assembler.	1M
	b)	Define symbol table.	1M
	c)	Define lexeme.	1M
	d)	List the possible actions can make in shift-reduce parsing.	1M
	e)	Define reduce/reduce conflict.	1M
	f)	Define syntax-directed definition.	1M
	g)	Define control stack.	1M
	h)	Define dynamic storage allocation.	1M
	i)	Define call by reference.	1M
	j)	Define register allocation.	1M
	k)	Define basic block	1M
	l)	Define CISC	1M
UNIT I			
2	a)	Illustrate phases of compiler with an assignment statement a=(b+c)*(b+c)*2	8M
Ans:		Diagram-2M Explanation-3M Example-3M	
2	b)	Find whether the following grammar is LL(1) or not S-> abSa|aaAb A->baAb|b	4M
Ans:		Procedure-2M Result-1M	
(OR)			
3	a)	Find the predictive parser for the following grammar and parse the sentence (a+b)*c E→ E+T|T T→ T*F|F F→ (E)| id	9M
Ans:		Procedure-3M Table-6M	
3	b)	Differentiate the lexical analysis with parsing.	3M
Ans:		Any 3 differences- 3M	
UNIT II			
4	a)	Construct the SLR parsing table for the grammar S->(L)|a L->L,S|S	8M
Ans:		Procedure-3M Table-5M	
4	b)	Construct Syntax tree for b + 5 – a	4M
Ans:		Tree -4M	
(OR)			
5	a)	Construct the LALR parsing table for the grammar S->L=R|R L->*R|id R->L	8M
Ans:		Procedure-3M Table-5M	
5	b)	Illustrate the construction of input/output translator with Yacc.	4M
Ans:		Diagram-2M Explanation-2M	
UNIT III			

6	a)	Illustrate stack and heap storage allocation strategies for strings and records.	7M
Ans:		Stack storage allocation-3M Heap storage allocation -4M	
6	b)	Demonstrate the representing of scope information.	5M
Ans:		Explanation-5M	
(OR)			
7	a)	Explain register assignment and allocation with an example.	5M
Ans:		Explanation -3M Example-2M	
7	b)	Demonstrate different data structures to symbol tables	7M
Ans:		Explanation-7M	
UNIT IV			
8	a)	Describe simple target machine model.	8M
Ans:		Expalanation-8M	
8	b)	Demonstrate determining the liveness and next-use information for each statement in a basic block.	4M
Ans:		Expalanation-4M	
(OR)			
9	a)	Illustrate back patching.	4M
Ans:		Expalanation-4M	
9	b)	Illustrate the issues in design of code generator	8M
Ans:		Expalanation-8M	