III/IV B.Tech Regular Degree Examination

Scheme of Evaluation

SET -3

Subject Name: Linear Integrated Circuits

Month & year: Feb, 2021

Subject code: 18EC501

Semester: Fifth

Department: ECE

Maximum: 50 Marks

Internal Faculty:

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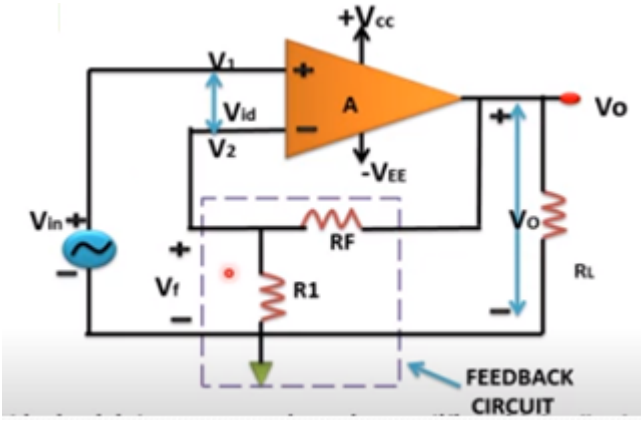
One Mark answers

1.a	Due to effect of input offset voltage, the total output offset voltage VooT as follows, In open loop op-amp, the total output offset voltage is equal to positive or negative saturation voltage. Total output offset voltage with feedback = (Total output offset voltage without feedback)/(1+AB)	1M
1.b	Input Impedance of an ideal op-amp is infinity. Output impedance of an ideal op-amp is zero.	1M
1.c	Slew Rate is defined as Maximum rate of change of output voltage per unit time.	1M
1.d	The ability of the oscillator circuit to oscillate at one exact frequency is called frequency stability.	1M
1.e	A comparator circuit compares two voltages and outputs either a 1 (the voltage at the plus side; VDD in the illustration) or a 0 (the voltage at the negative side) to indicate which is larger.	1M
1.f	List the Applications of VCO: • Phase Locked Loop • Modulation and Demodulation circuits • Frequency Synthesizers	1M
1.g	Clippers are used to reduce or clip some portion of waveforms where as Clampers are used to add some DC voltage to the waveforms.	1M
1.h	Flash type ADC	1M
1.i	The range of frequencies over which the PLL can acquire lock with an input signal.	1M
1.j	$H(s) = \frac{A_o}{s^2C^2R^2 + sCR(3 - A_o) + 1}$	1M

Essay answers

2.a **Explanation 1M+ Circuit 1M+Expressions 3M= 5M**

It is also called non-inverting voltage feedback circuit. With this type of feedback, the in signal drives the non-inverting input of an amplifier; a fraction of the output voltage is then back to the inverting input. The op-amp is represented by its symbol including its large sig voltage gain Ad or A, and the feedback circuit is composed of two resistors R1 and Rf.



Closed loop voltage gain:

$$\text{close loop voltage gain} = A_F \frac{V_o}{V_{in}}$$

$$\text{IN differential amplifier} = V_o = A v_{id} = A(V_1 - V_2)$$

$$V_2 = V_f = \frac{R1\ V_o}{R1 + RF}$$

$$V_1 = V_{in}$$

$$V_2 = V_f = \frac{R1\ V_o}{R1 + RF}$$

$$V_o = A\left[V_{in} - \frac{R1\ V_o}{R1 + RF}\right]$$

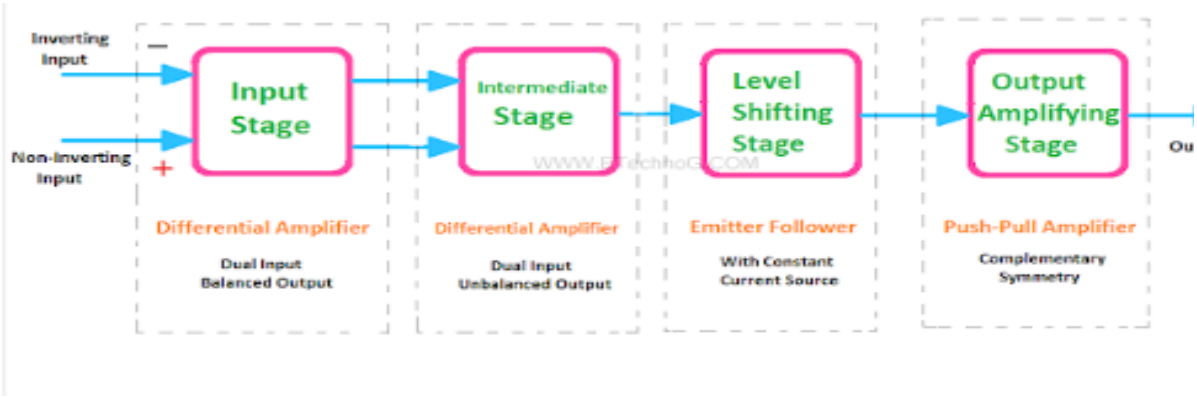
$$V_o = A\ V_{in} - \frac{AR1\ V_o}{R1 + RF}$$

$$V_o\left[1 + \frac{AR1\ V_o}{R1 + RF}\right] = AV_{in}$$

$$V_o = \frac{A(R1 + RF)\ V_{in}}{R1 + RF + AR1}$$

$$\frac{V_o}{V_{in}} = \frac{A(R1 + RF)}{R1 + RF + AR1} = AF$$

2.b **Diagram 3M + Explanation 2M = 5M**



Input Stage: It is a Dual input Balanced output Differential Amplifier

Increases the CMRR. High gain requirement is adjusted, Provides the input impedance very high.

Intermediate Stage: It is a Dual input unbalanced output Differential Amplifier

Driven by output of 1st stage, Adjusts the half gain of 1st stage ,Error voltage is cancelled in this stage.

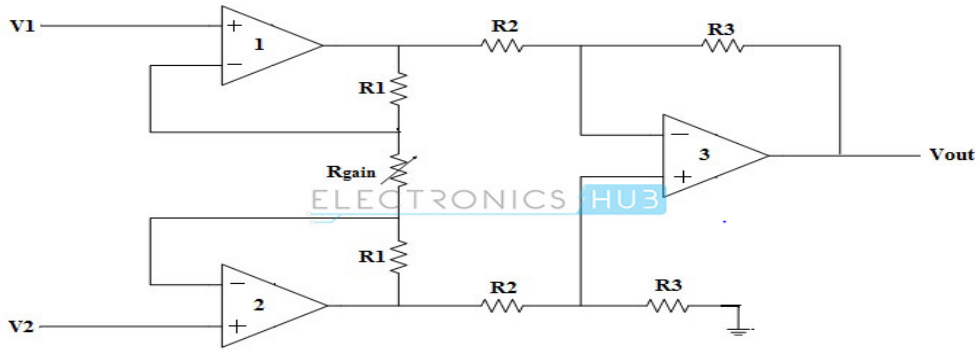
Level Shifting: Suppress the dc level downward to zero volt with respect to ground Consisting of current amplifiers as emitter followers. Also minimizes the error by suppressing dc level to ground.

Output Stage: This stage increases the output voltage swing and the current in supplying capability of the amplifiers. Provides low output impedance.

3.a **Explanation-2M+Circuit-2M+Expressions-1M=5M**

The important features are

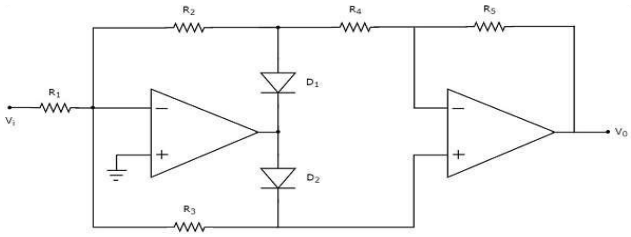
- High gain accuracy
- High CMRR
- Low DC offset
- Low output impedance



The output voltage expression is

$$Vo = R2/R1\ (1+2(R^1/R))(V1-V2)$$

3.b **Diagrams 2M + Expressions 3M = 5M**

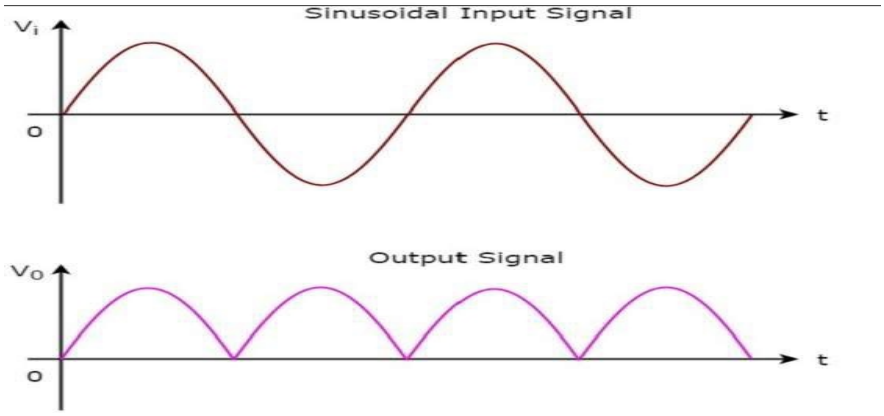


- The above circuit diagram consists of two op-amps, two diodes, D_1 & D_2 and five resistors, R_1 to R_5.

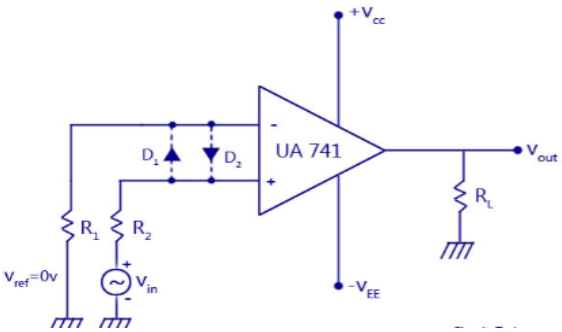
For the +v**e half cycle** of a sinusoidal input(V_i > o) the output of the first op-amp will be negative. Hence, diodes D_1 is forward biased and D_2 will be reverse biased.

- The ckt A_1 acts as Inv.amp , hence output voltage of the first op-amp will be , $V_{01} = (- R_2 /R_1) V_i$
- The ckt A_2 acts as another Inv.amp, with o/p given by $V_0 = (- R_5/ R_4) V_{01}$
- Total O/P Voltage ,$V_0 = (- R_2 /R_1)(-R_5 /R_4) V_i$
- When $R_2 = R_1 = R_5 = R_4 = R$
  Then $V_0 = V_i$
- For the **-ve half cycle** of a sinusoidal input (V_i < 0), the output of the first op-amp will be positive. Hence, diodes D_1 reverse biased and D_2 will be forward biased.
- Then ckt A_1 acts as Inv.amp, output voltage of the first op-amp will be $V_{01} = (-R_3 /R_1) V_i$
- The output of the first op-amp is directly connected to the non-inverting terminal of the second op-amp. Now, the second op-amp (ckt A_2) with resistors, R_4 and R_5 acts as a **non-inverting amplifier**.
- The output voltage of the second op-amp will be

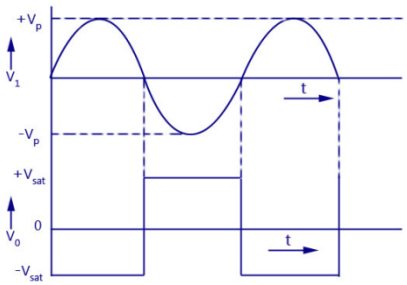
$$V_0 = \left(1 + \frac{R_5}{R_4}\right) V_{01}$$



4.a **diagram 3M+Explanation 2M = 5M**



- The zero crossing detector circuit is an important application of the op-amp comparator circuit.
- It can also be called as the sine to square wave converter. Anyone of the inverting or non-inverting comparators can be used as a zero-crossing detector. The only change to be brought in is the reference voltage with which the input voltage is to be compared, must be made zero (Vref = 0V). An input sine wave is given as Vin. These are shown in the circuit diagram and input and output waveforms of an inverting comparator with a 0V reference voltage.

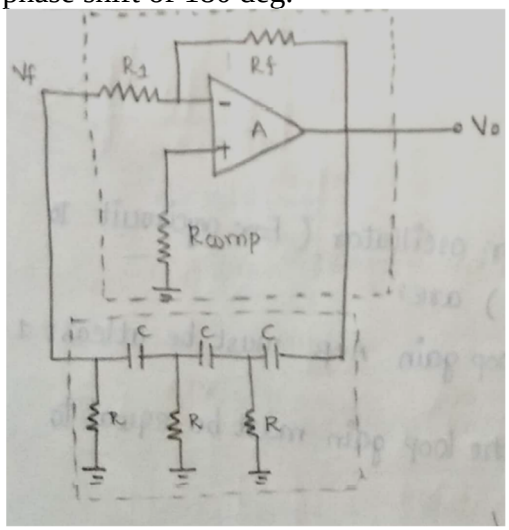


4.b **Diagram 1M + Expressions 4M= 5M**

RC Phase Shift Oscillator :

Op-Amp is used in the inverting mode and therefore provides 180 deg phase shift .

The additional phase of 180 deg is provided by RC cascaded feedback Circuit to obtain total phase shift of 180 deg.



Applying KVL to various loops we get,

$$I_1\left(R+\frac{1}{j\omega C}\right)-I_2 R = V_i$$

$$-I_1 R + I_2\left(2R+\frac{1}{j\omega C}\right)-I_3 R = 0$$

$$0 - I_2 R + I_3\left(2R+\frac{1}{j\omega C}\right) = 0$$

Replacing jω by s and writing the equations in the matrix form,

$$\begin{vmatrix} R+\frac{1}{sC} & -R & 0 \\ -R & 2R+\frac{1}{sC} & -R \\ 0 & -R & 2R+\frac{1}{sC} \end{vmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} V_i \\ 0 \\ 0 \end{bmatrix}$$

Using the Crammer's rule to obtain I_3

$$D = \begin{vmatrix} \frac{1+sRC}{sC} & -R & 0 \\ -R & \frac{1+2sRC}{sC} & -R \\ 0 & -R & \frac{1+2sRC}{sC} \end{vmatrix}$$

$$= \frac{(1+sRC)(1+2sRC)^2}{s^3C^3} - \frac{R^2(1+2sRC)}{sC} - \frac{R^2(1+sRC)}{sC}$$

$$= \frac{(1+sRC)(1+4sRC+4s^2C^2R^2) - R^2s^2C^2[1+2sRC+1+sRC]}{s^3C^3}$$

$$= \frac{1+5sRC+8s^2C^2R^2+4s^3C^3R^3-3s^3R^3C^3-2R^2s^2C^2}{s^3C^3}$$

$$= \frac{1+5sRC+6s^2C^2R^2+s^3C^3R^3}{s^3C^3} \qquad \ldots (19)$$

$$D_3 = \begin{vmatrix} \frac{1+sRC}{sC} & -R & V_i \\ -R & \frac{1+2sRC}{sC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= V_i R^2$$

$$\therefore \quad I_3 = \frac{D_3}{D} = \frac{V_i R^2 s^3 C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3}$$

Now $$V_o = V_f = I_3 R = \frac{V_i R^2 s^3 C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3}$$

$$\therefore \quad \beta = \frac{V_o}{V_i} = \frac{R^3 s^3 C^3}{1+5sCR+6s^2C^2R^2+s^3C^3R^3}$$

Replacing s by jω, s^2 by $-\omega^2$, s^3 by $-j\omega^3$

$$\therefore \quad \beta = \frac{-j\omega^3 R^3 C^3}{1+5j\omega CR-6\omega^2C^2R^2-j\omega^3C^3R^3}$$

Dividing numerator and denominator by $-j\omega^3R^3C^3$ and replacing $\frac{1}{\omega RC}$ by α we get,

$$\therefore \quad \beta = \frac{1}{1+6j\alpha-5\alpha^2-j\alpha^3}$$

$$\therefore \quad \boxed{\beta = \frac{1}{(1-5\alpha^2)+j\alpha(6-\alpha^2)}} \qquad \ldots (23)$$

To have phase shift of 180°, the imaginary part in the denominator must be zero.

$$\therefore \quad \alpha(6-\alpha^2) = 0$$

$$\therefore \quad \alpha^2 = 6 \qquad \text{neglecting zero value}$$

$$\boxed{\alpha = \sqrt{6}}$$

$$\therefore \quad \frac{1}{\omega RC} = \sqrt{6}$$

$$\boxed{f = \frac{1}{2\pi RC\sqrt{6}}}$$

This is the frequency with which circuit oscillates,

At this frequency,

$$\beta = \frac{1}{1-5\times(\sqrt{6})^2} = -\frac{1}{29}$$

The negative sign indicates a phase shift of **180°**

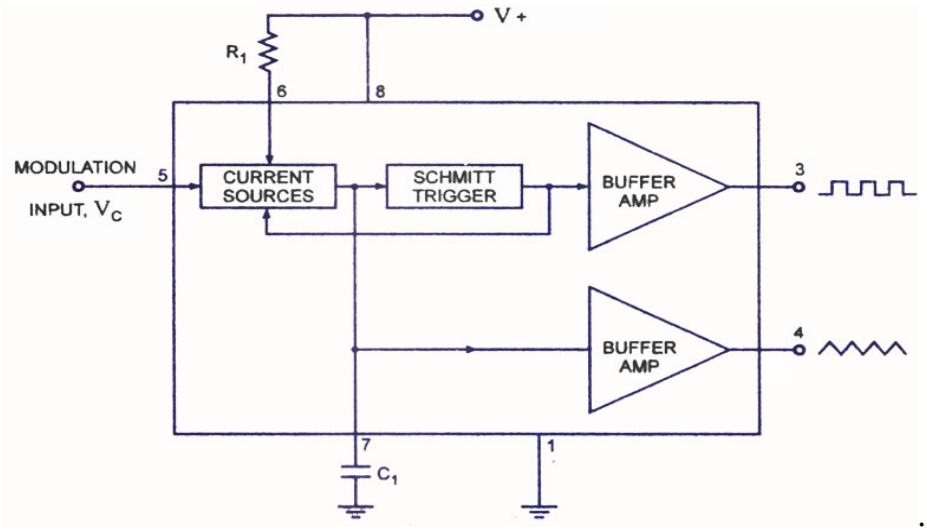
$$\therefore \quad \boxed{|\beta| = \frac{1}{29}}$$

Now to have the oscillations, $|A\beta| \geq 1$

$$\therefore \quad |A|\,|\beta| > 1$$

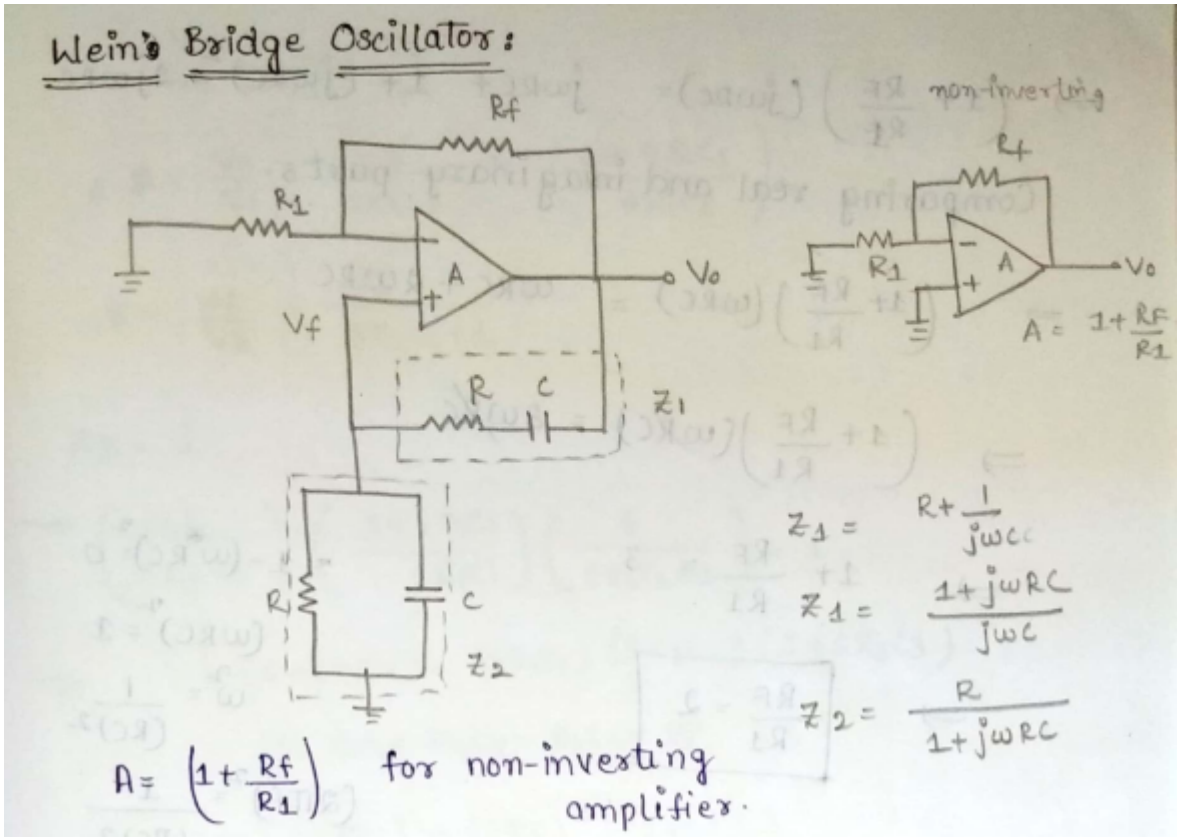
$$|A| \geq \frac{1}{|\beta|} \geq \frac{1}{\left(\frac{1}{29}\right)}$$

5.a **Explanation 2M + Circuit diagram 3M = 5M**

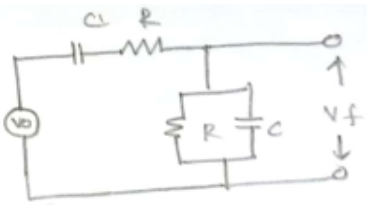


- The VCO block diagram consists of Current sources to charge and discharge an external capacitor at a rate set by external Resistor R and the modulating DC i/p voltage.
- Now the Triangular wave is generated by alternately charging the external capacitor by one current source and then linearly discharging it by another current source.
- The charge and discharge levels are determined by Schmitt trigger action.
- The schmitt Trigger also provides square wave at the o/p .
- Both the o/p waveforms are taken through Buffer amplifiers , so that the o/p impedance of each is 50 Ω .
- The VCO can be programmed over a 10 to 1 freq range by proper selection of external R,C and by control Voltage (V_c).
- The typical amplitude of triangular wave is 2.4 V and that of the square wave is 5.4 V pp.
- The free running frequency or centre operating freq is given by
  f_0 = (2 (+V - V_c))/ ((R1C1) +V) ,
  there is some limitations like
  1. 2kΩ <= R1 <= 20KΩ ,
  2. ¾ +V <= V_c <= +V
  3. f_0 < 1 MHz
  4. 10V <= +V <= 24V

5.b **Circuit diagram 1M + Expressions 4M = 5M**



$\beta = \frac{V_f}{V_o}$ $\quad V_f = V_o \cdot \frac{Z_2}{Z_1 + Z_2}$



$$\Rightarrow V_f = V_o \cdot \frac{\frac{R}{1+j\omega RC}}{\frac{1+j\omega RC}{j\omega C} + \frac{R}{1+j\omega RC}}$$

$$V_f = V_o \cdot \frac{R}{(1+j\omega RC)} \times \frac{(j\omega C)(1+j\omega RC)}{j\omega RC + (1+j\omega RC)^2}$$

$$V_f = V_o \cdot \frac{j\omega RC}{j\omega RC + (1+j\omega RC)^2}$$

$$\Rightarrow \frac{V_f}{V_o} = \frac{SRC}{SRC + (1+SRC)^2}$$

$A\beta = 1$

$$\Rightarrow \left[1 + \frac{R_f}{R_1}\right]\left[\frac{SRC}{SRC + (1+SRC)^2}\right] = 1$$

$$\Rightarrow \left(1 + \frac{R_F}{R_1}\right)(j\omega RC) = j\omega RC + (1 + j\omega RC)^2$$

$$\Rightarrow \left(1 + \frac{R_F}{R_1}\right)(j\omega RC) = j\omega RC + 1 + (j\omega RC)^2 + 2j\omega RC$$

Comparing real and imaginary parts.

$$\Rightarrow \left(1 + \frac{R_F}{R_1}\right)(\omega RC) = \omega RC + 2\omega RC$$

$$\Rightarrow \left(1 + \frac{R_F}{R_1}\right)(\omega RC) = 3\omega RC$$

$$\Rightarrow 1 + \frac{R_F}{R_1} = 3$$

$$\Rightarrow \boxed{\frac{R_F}{R_1} = 2}$$

$- 1 - (\omega RC)^2 = 0$

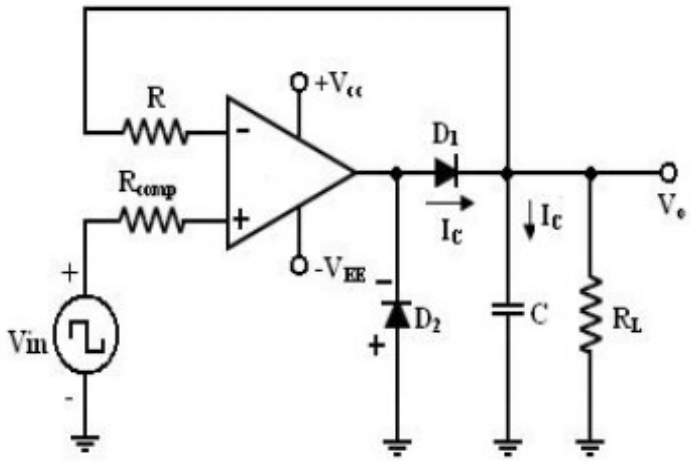
$(\omega RC)^2 = 1$

$\omega^2 = \frac{1}{(RC)^2}$

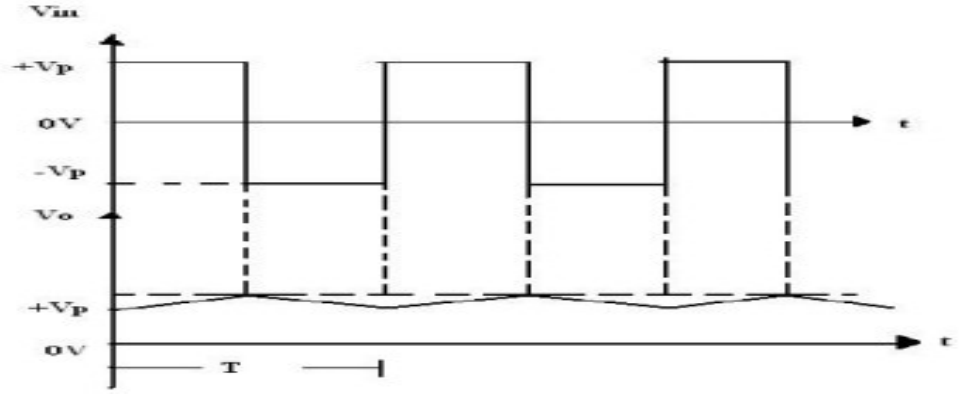
$(2\pi f)^2 = \frac{1}{(RC)^2}$

$$\boxed{f = \frac{1}{2\pi RC}}$$

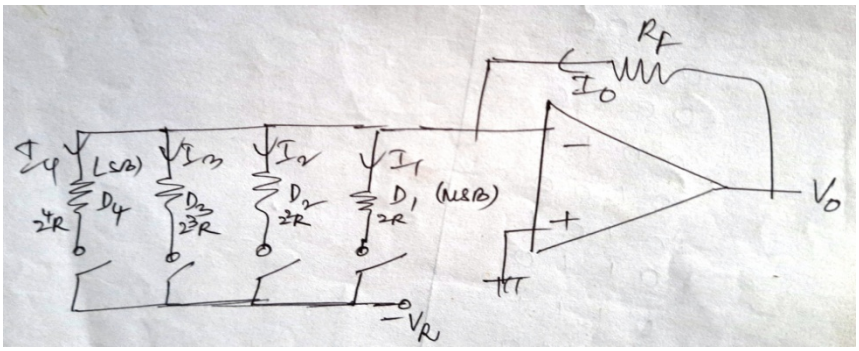
6.a **Explanation 3M + Circuit diagram 2M = 5M**



- AC voltmeters are used to measure rms value of pure sinusoidal signals.
- So it is not suitable to measure square , triangular , saw tooth waveforms (non-sinusoidal signals).
- so peak values are measured for non sinusoidal signals using peak detector..
- Let us consider a square wave as input.
- Case 1: For positive half cycle of V_{in} , the o/p of op-amp $V_0^1 = +V_{sat}$.
  Hence D_1 is forward biased, D_2 reverse biased.
  So the capacitor is allowed to charge to the positive peak value of V_{in} i.e. the circuit acts as a voltage follower
- case 2: for Negative half cycle of V_{in} , $V_0^1 = -V_{sat}$
  hence D_1 is reverse biased and D_2 forward biased.
  Hence the capacitor will not be charging and retains the voltage across it.
- For proper operation of circuit , charging and discharging constants must be $CR_d <= T/10$ and $CR_L >= 10T$
- Where R_d on resistance of D_1 , R_L load resistance.
- Negative peaks can be detected by reversing the diodes D_1 ,D_2
- The i/p and o/p waveforms are shown below.



6.b **Expressions 3M + Circuit diagram 2M = 5M**



- The circuit acts as inverting Summing amplifier with Binary weighted resistor network.
- D_1, D_2, D_3, D_4 are digital inputs.
- When $D_1 = 1$, then the switch is closed and reference voltage ($-V_R$) is connected to op-amp inverting terminal.
- When $D_1 = 0$, then resistor is connected to ground.
- Writing KCL at inverting input junction (node x)of op-amp

  $I_0 = - (I_1 + I_2 + I_3 + I_4)$

  $V_0 / R_F = - (V_R/2R) D_1 – (V_R/2^2R) D2 – (V_R/2^3R)D_3 – (V_R/2^4R)D_4$

  $V_0 / R_F = - V_R/R (D_1/2 + D_2 /2^2 + D_3/2^3 + D_4/2^4)$

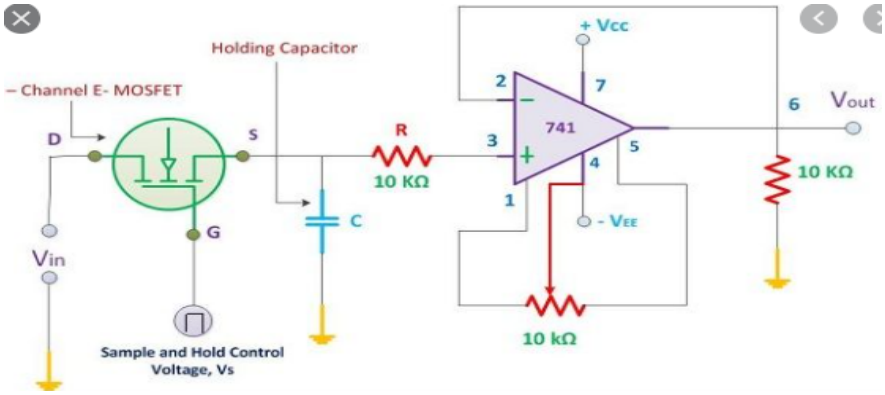
  When $R_F = R$,

  $V_0 = - V_R (D_1/2 + D_2 /2^2 + D_3/2^3 + D_4/2^4)$

  When $V_R = -5V$ (negative voltage)
- The relation between i/p digital and o/p analog voltage we can see

Digital input $D_1D_2D_3D_4$	**Analog output V_0**
0000	= 0V
0001	-5x(0+0+0+1/16) = 0.3125V
0010	-5X(0 +0 +1/8 + 0) = 0.625V
0011	-5(0+ 0+ 1/8+ 1/16) = 0.9375V
0100	-5 (0+1/4 + 0 + 0) = 1.25V
0101	-5(0+1/4+0+1/16) = 1.5625V
0110	-5(0+1/4+1/8+0) = 1.875V
0111	-5(0+1/4+1/8+1/16) = 2.1875V
1000	-5(1/2+0+0+0) = 2.5V
1001	-5(1/2+0+0+1/16) = 2.8125V
1010	-5(1/2+0+1/8+0) = 3.125V
1011	-5(1/2+0+1/8+1/16) = 3.4375V
1100	-5(1/2+1/4+0+0) = 3.75V
1110	-5(1/2+1/4+1/8+0) = 4.375V
1111	-5(1/2+1/4+1/8+1/16) = 4.6875V

7.a **Diagram 2M + Explanation 1M + Expressions 2M=5M**



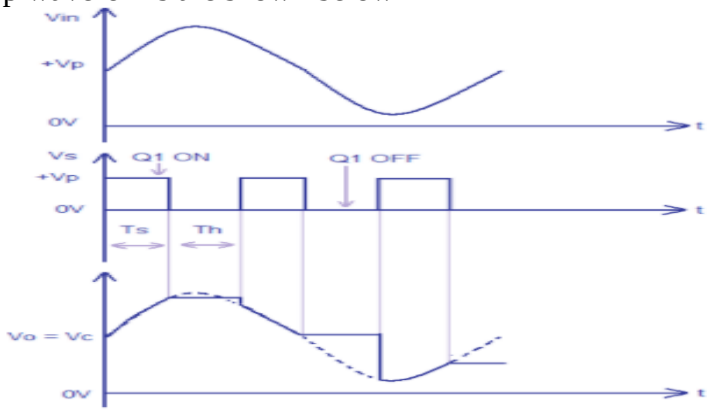
Ckt operation :

1. it samples an input signal and holds on to its last sampled value until the input is sampled again.
2. n-channel E-MOSFET acts as switch, controlled by the sample and hold voltage (V_s)
3. the capacitor serves as a storage element.
4. the analog signal to be sampled is applied Drain and control voltage to Gate terminal of E-MOSFET.
5. For high positive value of V_s the Gate is closed and E-MOSFET conducts. It allows the i/p voltage to charge the capacitor. Now the voltage across capacitor will be the o/p voltage.
6. when control voltage V_s is low or negative , then the Gate is opened and E-MOSFET is off state (non-conducting state) and acts as a open switch.
7. Holding capacitor must be a low leak like teflon , polysterene, etc. Now the capacitor does not charge and retains the last sampled peak value till the next sampling period.
8. the voltage across capacitor appears at o/p of op-amp, since it acts as a voltage follower.
9. during the switch is ON , the capacitor starts charging to the instantaneous value of i/p signal with a time constant , $\tau = (R_0 + r_{ds\ ON})C$.

where R_0 =o/p resistance of voltage follower (op-amp) , $r_{ds\ ON}$ = is the ON resistance of E-MOSFET.

10. the frequency of control voltage should be kept high (twice) w.r.t. i/p signal frequency so as to retrieve the i/p from o/p waveform.

Sample and hold circuit available in IC form as LF398, LF198 ,HA2420. The i/p and o/p waveforms are shown below



7.b **Diagram 2M + Bits conversion 3M = 5M**

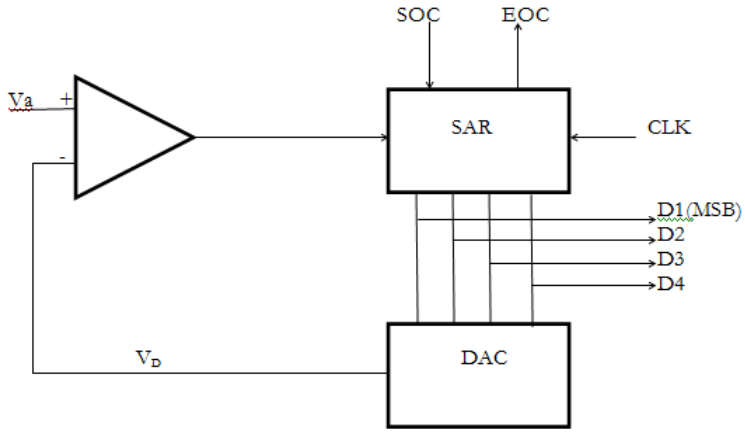
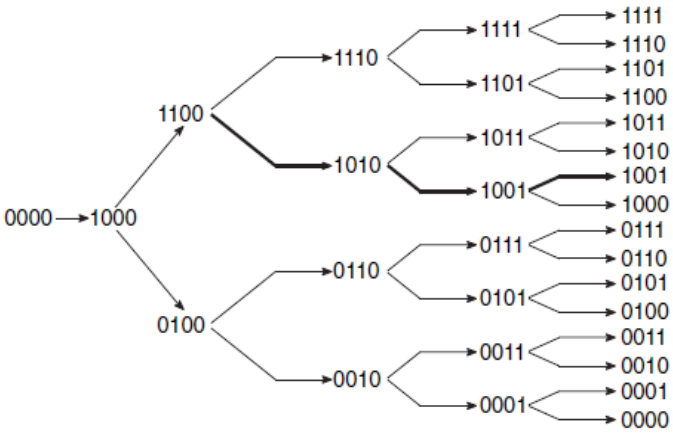


Figure 1 : Block diagram of successive approximation ADC



Conversion process in a successive approximation type A/D converter.

8.a **Diagrams 3M + Explanation 2M = 5M**

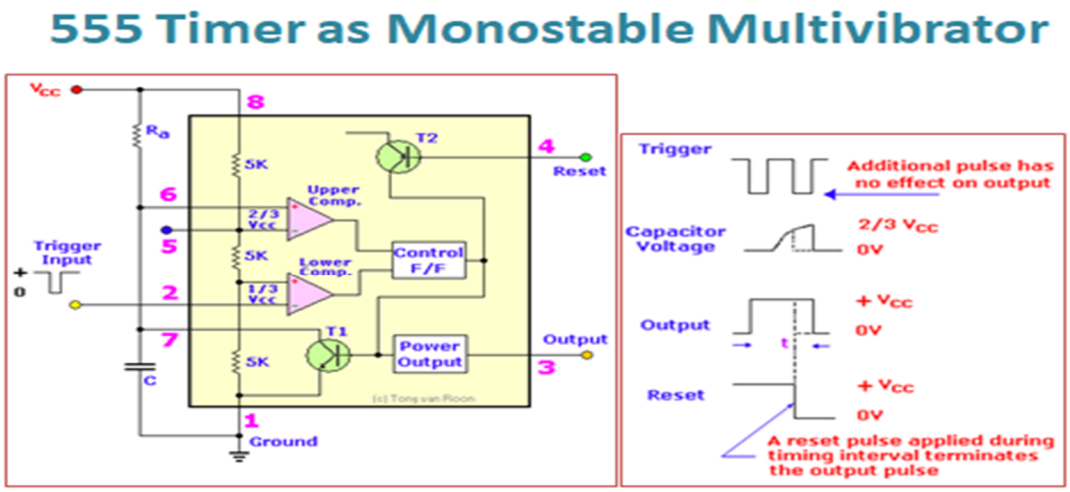
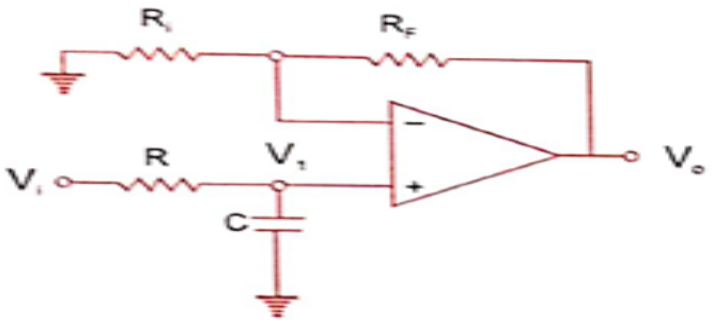


Fig (a): Timer in Monostable Operation with Functional Diagram
Fig (b): Output wave Form of Monostable

8.b **Circuit Diagram 2M+Expressions 3M=5M**



The voltage V_1 across the capacitor C in the s-domain is

$$V_1(s) = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_i(s)$$

So, $$\frac{V_1(s)}{V_i(s)} = \frac{1}{RCs + 1}$$

where $V(s)$ is the Laplace transform of v in time domain.

The closed loop gain A_o of the op-amp is,

$$A_o = \frac{V_o(s)}{V_1(s)} = \left(1 + \frac{R_F}{R_i}\right)$$

So, the overall transfer function from Eqs. (7.4) and (7.5) is

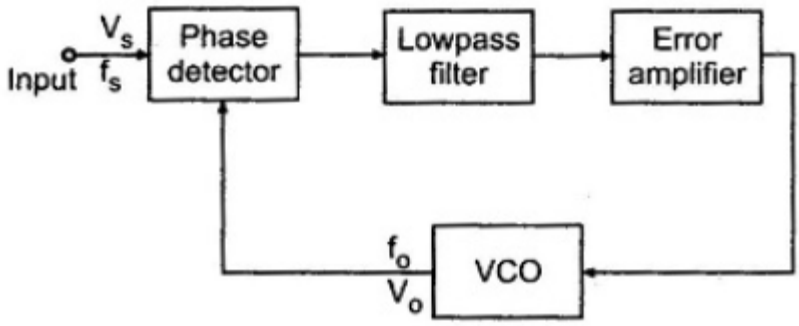
$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_1(s)} \cdot \frac{V_1(s)}{V_i(s)} = \frac{A_o}{RCs + 1}$$

Let $$\omega_h = \frac{1}{RC}$$

$$H(j\omega) = \frac{A_o}{1 + j\omega RC} = \frac{A_o}{1 + j(f/f_h)}$$

$$f_h = \frac{1}{2\pi RC} \text{ and } f = \frac{\omega}{2\pi}$$

9.a **Circuit Diagram 2M + Explanation 1M + Expressions 2M=5M**

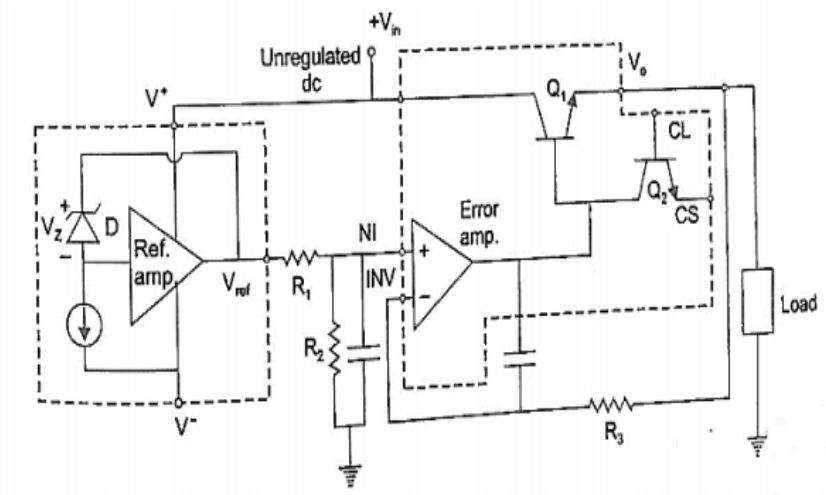


Phase locked loop construction and operation:

- The PLL consists of i) Phase detector ii) LPF iii) VCO. The phase detector or comparator compares the input frequency fIN with feedback frequency fOUT.

- The output of the phase detector is proportional to the phase difference between fIN & fOUT. The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage.
- The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO.
- The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.
- PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

9.b **Circuit Diagram 2M + Explanation 1M+Expressions 2M=5M**



- <u>Circuit operation :</u> the voltage at NI i/p terminal of error amplifier due to R_1 , R_2 resistive network is given by
- $V_{NI} = V_{ref} (R_2 / R_1 + R_2)$
- Now the difference b/n V_{NI} and V_0 is amplified by error amp.
- Now the o/p of error amp drives the series pass transistor Q_1 so as to minimize the difference b/n NI &INV inputs of error amplifier.
- Q_1 acts as emitter follower
- Hence $V_{NI} – V_0 = 0 = V_{ref} (R_2 / R_1 + R_2) – V_0$
- So $V_0 = V_{ref} (R_2 / R_1 + R_2)$
- If o/p voltage becomes low , V_0 low , then the INV i/p of error amp also goes down.
- It makes o/p of error amp more positive, thereby driving Q_1 more into conduction.
- More conduction of Q_1 reduces voltage drop across it .
- Hence more current flows into load causing voltage drop across load to increase.
- The initial drop in the load voltage has been compensated.
- Any increase in load voltage or changes in the i/p voltage get regulated.
- Since $V_{ref} = 7.15V$, $V_0 = 7.15 (R_2 / R_1 + R_2) < 7V$ (always)
- Hence it is a low voltage regulator