III/IV B.Tech REGULAR DEGREE EXAMINATION

February, 2021 — **Electrical and Electronics Engineering**

Fifth Semester — **Power Electronics(18EE503)**

Time: Three Hours — **Maximum:** 50 Marks

*Answer **ALL** Questions from PART-A.* (1X10 = 10 Marks)

*Answer **ANY FOUR** questions from PART-B.* (4X10=40 Marks)

PART-A

1a) The latching current is the smallest amount of anode current is required for preserving the thyristor in the ON condition instantly once a thyristor is turned ON then the gate signal has been detached.

b) VSI requires DC-link capacitor and AC filter inductors; CSI requires DC-link inductor and AC filter capacitors. VSI requires constant DC-link voltage, and generates AC voltages in the form of voltage pulses; CSI requires constant DC-link current, and generates AC currents in the form of current pulses.

c) Increase DC voltage for a given firing angle due to the elimination of negative portions of the instantaneous dc waveform in a SCR phase controlled converter, Will reduce the generated ripple voltage on the DC side of a SCR phase controlled converter due to same reason as in above, reducing the filtering requirements. Will improve the input PF in an SCR phase controlled converter due to ending the input current waveform earlier by permitting internal free-wheeling.

d) $\frac{3\,\omega L_s}{\pi} I_0$

e) Modulation index is defined as the ratio of the fundamental component amplitude of the line-to-neutral inverter output voltage to one-half of the available DC bus voltage

$$\text{Modulation index} = M = \frac{A_r}{A_c}$$

f) Forced Commutation

g) $v_n = \frac{8\,V_s}{n\pi} \sin n\gamma \cdot \sin \frac{nd}{2}$

h) A chopper is a device that converts fixed DC input to a variable DC output voltage directly.

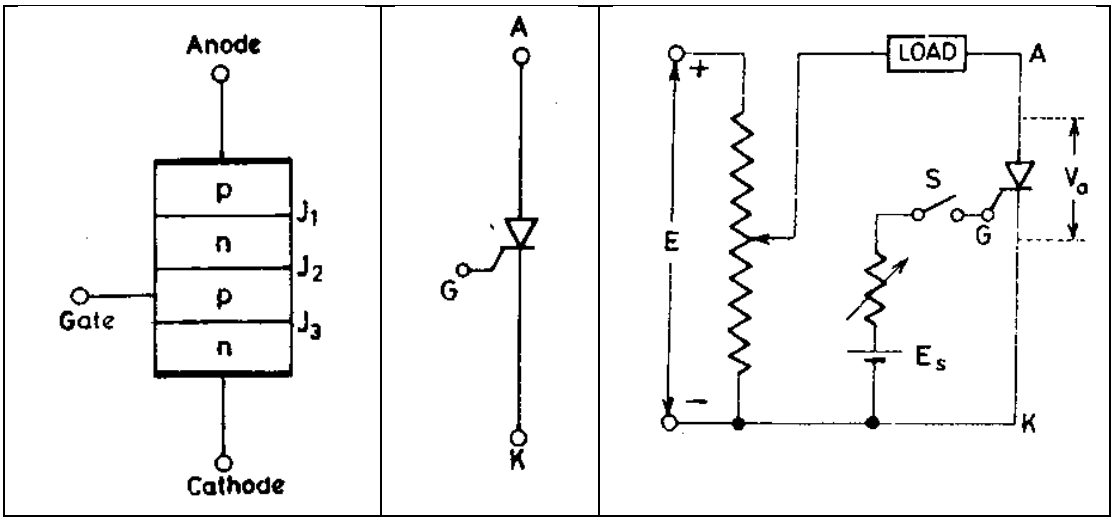
I) AC drives, propulsion systems, high frequency induction heating, synchronous motors in sea and undersea vehicles, electromagnetic launchers, Traction system.

J) ac voltage controllers, allow controlling the output **voltage** only, while the output frequency **is** the same **cycloconverters**, the output frequency can be controlled, but it **is** at least one order **of** magnitude lower than the input frequency.

PART-B

2a)

Thyristor is a four layer, three-junction, p-n-p-n semiconductor switching device. It has three terminals ; anode, cathode and gate. Fig. 4.1 (a) gives constructional details of a typical thyristor. Basically, a thyristor consists of four layers of alternate p-type and n-type silicon semiconductors forming three junctions J_1, J_2 and J_3 as shown in Fig. 4.1 (a). The threaded portion is for the purpose of tightening the thyristor to the frame or heat sink with the help of a nut. Gate terminal is usually kept near the cathode terminal Fig. 4.1 (a). Schematic diagram and circuit symbol for a thyristor are shown respectively in Figs. 4.1 (b) and (c). The terminal connected to outer p region is called anode (A), the terminal connected to outer n region is called cathode and that connected to inner p region is called the gate (G). For large current applications, thyristors need better cooling ; this is achieved to a great extent by

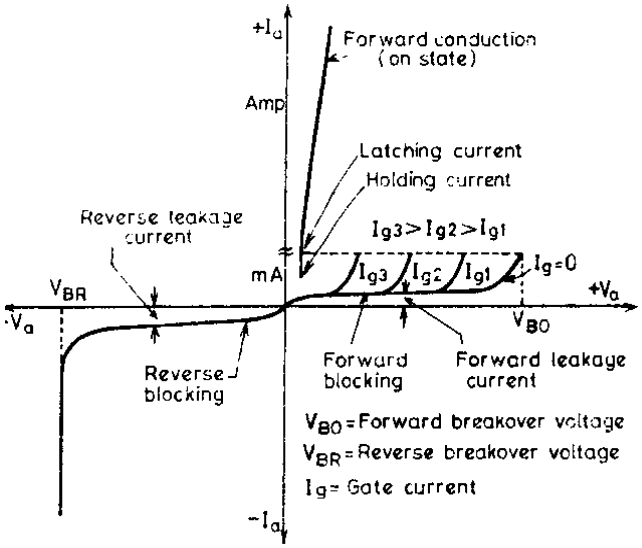


An elementary circuit diagram for obtaining static V-I characteristics of a thyristor is shown in Fig. . The anode and cathode are connected to main source through the load. The gate and cathode are fed from a source E_s which provides positive gate current from gate to cathode.

Fig. shows static V-I characteristics of a thyristor. Here V_a is the anode voltage across thyristor terminals A, K and I_a is the anode current. Typical SCR V-I characteristic shown in Fig. reveals that a thyristor has three basic modes of operation ; namely, reverse blocking mode, forward blocking (off-state) mode and forward conduction (on-state) mode. These three modes of operation are now discussed below :

Reverse Blocking Mode. When cathode is made positive with respect to anode with switch S open, Fig. , thyristor is reverse biased as shown in Fig. . Junctions J_1, J_3 are seen to be reverse biased whereas junction J_2 is forward biased. The device behaves as if two diodes are connected in series with reverse voltage applied across them. A small leakage current of the order of a few milliamperes (or a few microamperes depending upon

the SCR rating) flows. This is reverse blocking mode, called the off-state, of the thyristor. If the reverse voltage is increased, then at a critical breakdown level, called reverse breakdown voltage V_{BR}, an avalanche occurs at J_1 and J_3 and the reverse current increases rapidly. A large current associated with V_{BR} gives rise to more losses in the SCR. This may lead to thyristor damage as the junction temperature may exceed its permissible temperature rise. It should, therefore, be ensured that maximum working reverse voltage across a thyristor does not exceed V_{BR}. When reverse voltage applied across a thyristor is less than V_{BR}, the device offers a high impedance in the reverse direction. The SCR in the reverse blocking mode may therefore be treated as an open switch.



Forward Blocking Mode : When anode is positive with respect to the cathode, with gate circuit open, thyristor is said to be forward biased as shown in Fig. . . It is seen from this figure that junctions J_1, J_3 are forward biased but junction J_2 is reverse biased. In this mode, a small current, called forward leakage current, flows as shown in Figs. and . . In case the forward voltage is increased, then the reverse biased junction J_2 will

Forward Conduction Mode : In this mode, thyristor conducts currents from anode to cathode with a very small voltage drop across it. A thyristor is brought from forward blocking mode to forward conduction mode by turning it on by exceeding the forward breakover voltage or by applying a gate pulse between gate and cathode. In this mode, thyristor is in on-state and behaves like a closed switch. Voltage drop across thyristor in the on state is of the order of 1 to 2 V depending on the rating of SCR. It may be seen from Fig. that this voltage drop increases slightly with an increase in anode current. In conduction mode, anode current is limited by load impedance alone as voltage drop across SCR is quite small. This small voltage drop v_T across the device is due to ohmic drop in the four layers.

3a)

(*a*) *Resistance firing circuits.* As stated above, resistance trigger circuits are the simplest and most economical. They however, suffer from a limited range of firing angle control (0° to 90°), great dependence on temperature and difference in performance between individual SCRs.

Fig. . . shows the most basic resistance triggering circuit. R_2 is the variable resistance, R is the stabilizing resistance. In case R_2 is zero, gate current may flow from source, through load, R_1, D and gate to cathode. This current should not exceed maximum permissible gate current I_{gm}. R_1 can therefore, be found from the relation,

$$\frac{V_m}{R_1} \le I_{gm} \quad \text{or} \quad R_1 \ge \frac{V_m}{I_{gm}}$$

where V_m = maximum value of source voltage

It is thus seen that function of R_1 is to limit the gate current to a safe value as R_2 is varied.

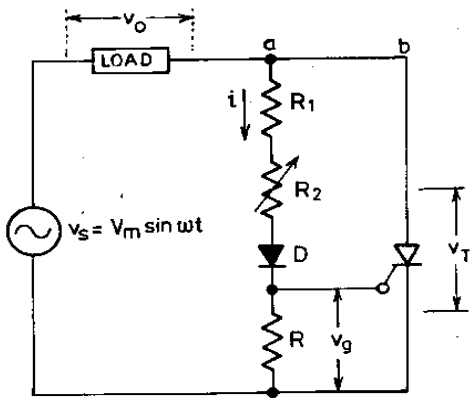


Fig. Resistance firing circuit.

Resistance R should have such a value that maximum voltage drop across it does not exceed maximum possible gate voltage V_{gm}. This can happen only when R_2 is zero. Under this condition,

$$\frac{V_m}{R_1 + R} \cdot R \le V_{gm}$$

or,

$$R \le \frac{V_{gm} \cdot R_1}{V_m - V_{gm}}$$

As resistances R_1, R_2 are large, gate trigger circuit draws a small current. Diode D allows the flow of current during positive half cycle only, *i.e.* gate voltage v_g is half-wave dc pulse. The amplitude of this dc pulse can be controlled by varying R_2.

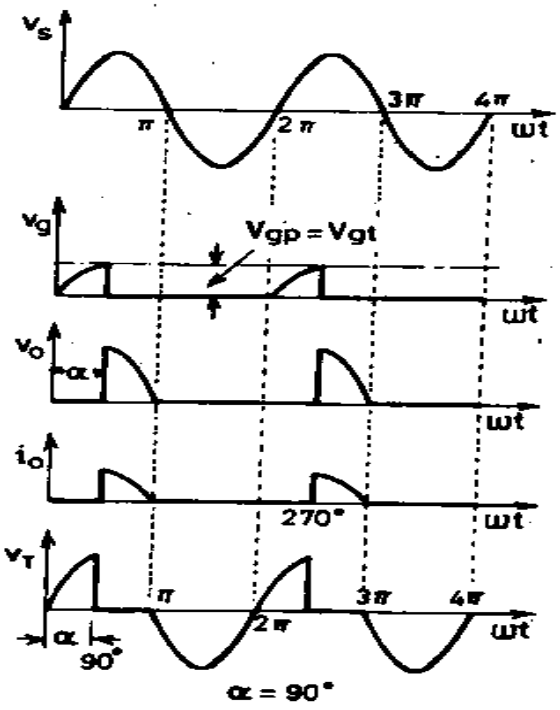
...)

$$V_{gp} \sin \alpha = V_{gt}$$

$$\alpha = \sin^{-1} (V_{gt}/V_{gp})$$

$$V_{gp} = \frac{V_m R}{R_1 + R_2 + R}$$

$$\alpha = \sin^{-1} \left[\frac{V_{gt} \cdot (R_1 + R_2 + R)}{V_m R} \right]$$



3b)

THYRISTOR TURN-ON METHODS

With anode positive with respect to cathode, a thyristor can be turned on by any one of the following techniques :

(*a*) Forward voltage triggering
(*b*) gate triggering
(*c*) *dv/dt* triggering
(*d*) Temperature triggering
(*e*) Light triggering.

These methods of turning-on a thyristor are now discussed one after the other.

(*a*) *Forward Voltage Triggering :* When anode to cathode forward voltage is increased with gate circuit open, the reverse biased junction J_2 will break. This is known as avalanche breakdown and the voltage at which avalanche occurs is called forward breakover voltage V_{BO}. At this voltage, thyristor changes from off-state (high voltage with low leakage current) to on-state characterised by low voltage across thyristor with large forward current. As other junctions J_1, J_3 are already forward biased, breakdown of junction J_2 allows free movement of carriers across three junctions and as a result, large forward anode-current flows. As stated before, this forward current is limited by the load impedance. In practice, the transition from off-state to on-state obtained by exceeding V_{BO} is never employed as it may destroy the device.

(*b*) *Gate Triggering* : Turning on of thyristors by gate triggering is simple, reliable and efficient, it is therefore the most usual method of firing the forward biased SCRs. A thyristor with forward breakover voltage (say 800 V) higher than the normal working voltage (say 400 V) is chosen. This means that thyristor will remain in forward blocking state with normal working voltage across anode and cathode and with gate open. However, when turn-on of a thyristor is required, a positive gate voltage between gate and cathode is applied. With gate current thus established, charges are injected into the inner p layer and voltage at which forward breakover occurs is reduced. The forward voltage at which the device switches to

(*d*) *Temperature Triggering* : During forward blocking, most of the applied voltage appears across reverse biased junction J_2. This voltage across junction J_2 associated with leakage

current may raise the temperature of this junction. With increase in temperature, leakage current through junction J_2 further increases. This cumulative process may turn on the SCR at some high temperature.

(*e*) *Light Triggering*. For light-triggered SCRs, a recess (or niche) is made in the inner p-layer as shown in Fig. 4.5 (*a*). When this recess is irradiated, free charge carriers (holes and electrons) are generated just like when gate signal is applied between gate and cathode. The pulse of light of appropriate wavelength is guided by optical fibres for irradiation. If the intensity of this light thrown on the recess exceeds a certain value, forward-biased SCR is turned on. Such a thyristor is known as light-activated SCR (LASCR).

Light-triggered thyristors have now been used in high-voltage direct current (HVDC) transmission systems. In these several SCRs are connected in series-parallel combination and their light-triggering has the advantage of electrical isolation between power and control circuits.

4a)

Three-phase Full Converters

If all the diodes of F[illegible] are replaced by thyristors, a three-phase full-converter bridge as shown in Fig. [illegible] is obtained. The three-phase input supply is connected to terminals A, B, C and the load RLE is connected across the output terminals of converter as shown. As in a single-phase full-converter, thyristor power circuit of Fig. [illegible] works as a three-phase ac to dc converter for firing angle delay $0° < \alpha \leq 90°$ and as three-phase line-commutated inverter for $90° < \alpha < 180°$. A three-phase full converter is, therefore, preferred where regeneration of power is required. The numbering of SCRs in Fig. 6.24 is 1, 3, 5 for the positive group and 4 (= 1 + 3), 6 (= 3 + 3), 2(= 5 + 3 – 6) for the negative group. This numbering scheme is adopted here as it agrees with the sequence of gating of the six thyristors in a 3-phase full converter.

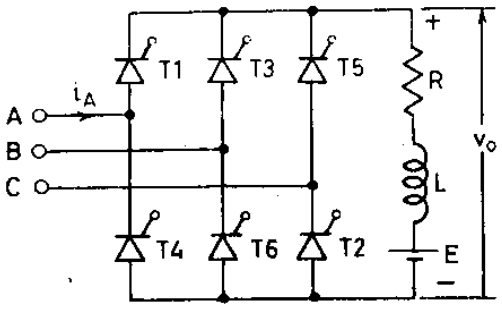
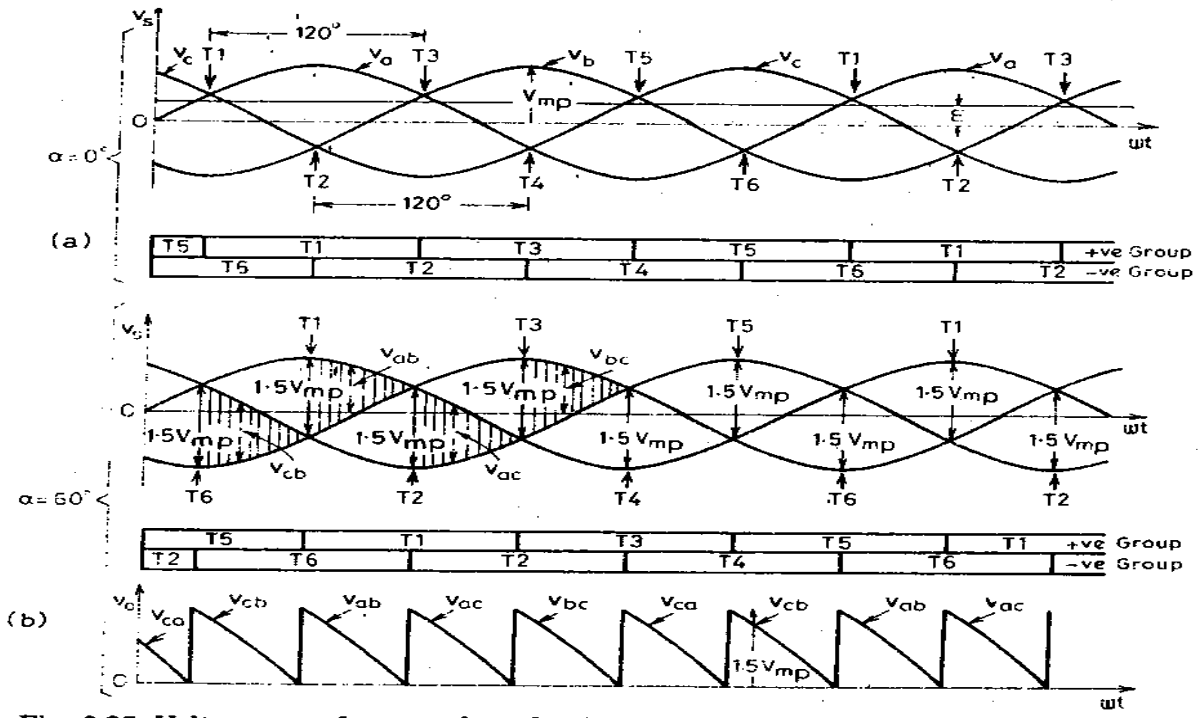


Fig. [illegible]. Power circuit for a 3-phase full-converter feeding RLE load.



If sine function is used for the source voltage, then $v_{ab} = V_{ml} \sin \omega t$ because $v_{ab} = 0$ at $\omega t = 0$.

$$\therefore \quad V_0 = \frac{3}{\pi} \int_{\frac{\pi}{3}+\alpha}^{\frac{2\pi}{3}+\alpha} V_{ml} \sin \omega t \cdot d(\omega t)$$

$$= -\frac{3V_{ml}}{\pi}\left[\cos\left(\frac{2\pi}{3}+\alpha\right) - \cos\left(\frac{\pi}{3}+\alpha\right)\right] = \frac{3V_{ml}}{\pi}\cos\alpha \quad \ldots$$

It is observed from Fig. 6.26 that source current for phase A, *i.e.* i_A (or for any other phase) flows for 120° for every 180°. Therefore, in case output current is assumed constant at I_0, the rms value of source current is

$$I_s = \sqrt{I_0^2 \frac{2\pi}{3} \times \frac{1}{\pi}} = I_0 \sqrt{\frac{2}{3}}$$

Each SCR conducts for 120° for every 360°. Therefore, the rms value of thyristor current is

$$I_{Th} = \sqrt{I_0^2 \frac{2\pi}{3} \times \frac{1}{2\pi}} = I_0 \sqrt{\frac{1}{3}}$$

The sequence of events in Fig. 6.25 can also be shown more conveniently if line voltages, instead of phase voltages, are considered. In Fig. are shown line voltages v_{ab}, v_{ac}, v_{bc}, v_{ba} etc. For $\alpha = 0°$, SCRs T1, T2,....T6 behave as diodes and the output voltage waveform is as shown in Fig. by v_{ab}, v_{ac}, v_{bc} etc. In this figure, for $\alpha = 0$, T1 is turned on at $\omega t = 60°$, T2 at $\omega t = 120°$, T3 at $\omega t = 180°$ and so on. In Fig. 6.26 (*a*), therefore, firing angle is measured from $\omega t = 60°$ for T1, from $\omega t = 120°$ for T2, from $\omega t = 180°$ for T3 and so on.

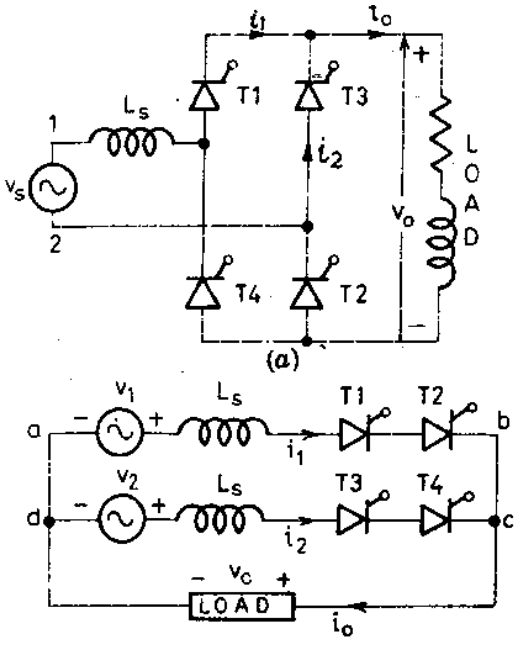
The question may arise in the minds of the readers as to why T1, for $\alpha = 0$, conducts from $\omega t = 60°$ and not from $\omega t = 0°$. Here the use of subscripts *ab*, *ac*, *bc*, *ba* etc come to the rescue of readers. As observed, the subscripts in sequence appear twice. When *first* subscript appears twice, the SCR in the positive group pertaining to that line conducts for 120°. Likewise, when *second* subscript comes twice, the SCR in the negative group pertaining to that line conducts for 120°. For example, first subscript 'a' appears twice in v_{ab}, v_{ac} ; therefore SCR from positive group T1 will begin conduction when v_{ab} appears *i.e.* at $\omega t = 60°$. In v_{ac}, v_{bc}, second subscript '*C*' appears twice, therefore SCR from negative group T2 will begin conduction when v_{ac} appears *i.e.* from $\omega t = 120°$ in Fig. Similarly, first subscript '*b*' appears twice in v_{bc}, v_{ba}, so SCR from positive group T3 will begin conduction when v_{bc} appears *i.e.* from $\omega t = 180°$

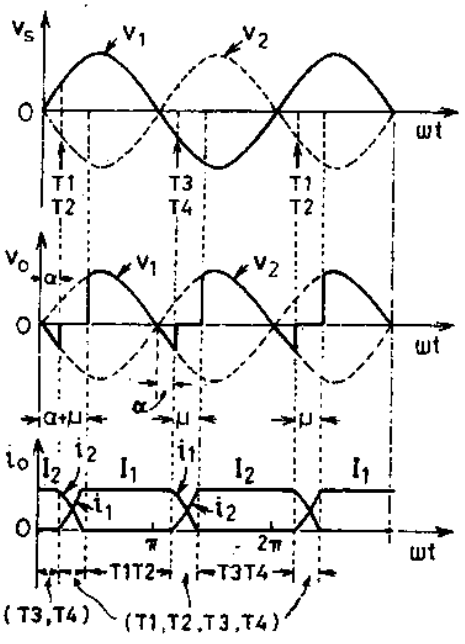
5a)

Single-phase Full Converter

The commutation overlap is more predominant in full converters than in semiconverters.

In the single-phase full converter shown in Fig. , L_s is the source inductance. The load current is assumed constant (analysis with pulsating load current is more involved). Fig. gives the equivalent circuit for Fig. 6.32 (*a*) for analytical purposes. When terminal 1 of source voltage v_s is positive in Fig. 6.32 (*a*), current i_1 flows through L_s, T1, load and T2; this is shown as v_1, L_s, T1 T2 and load in Fig. 6.32 (*b*). Similarly, when terminal 2 of v_s is positive, load current i_2 flows through T3, load, T4 ; this is shown as v_2, L_3, T3 T4 and load





$$v_1 - L_s \cdot \frac{di_1}{dt} = v_2 - L_s \frac{di_2}{dt}$$

or
$$v_1 - v_2 = L_s \left(\frac{di_1}{dt} - \frac{di_2}{dt} \right)$$

It is seen from Fig. 6.32 (c) that if $v_1 = V_m \sin \omega t$, then $v_2 = -V_m \sin \omega t$.

$\therefore$
$$L_s \left(\frac{di_1}{dt} - \frac{di_2}{dt} \right) = 2 V_m \sin \omega t$$

As the load current is assumed constant throughout $i_1 + i_2 = I_0$

or
$$\frac{di_1}{dt} + \frac{di_2}{dt} = 0$$

From
$$\frac{di_1}{dt} - \frac{di_2}{dt} = \frac{2V_m}{L_s} \sin \omega t$$

Load current i_1 through thyristor pair T1, T2 builds up from zero to I_0 during the overlap angle μ; *i.e.* at $\omega t = \alpha$,

$$i_1 = 0 \text{ and at } \omega t = (\alpha + \mu),\ i_1 = I_0$$

$\therefore$ From Eq. ( ),
$$\int_0^{I_0} di_1 = \frac{V_m}{L_s} \int_{\alpha/\omega}^{(\alpha+\mu)/\omega} \sin \omega t \cdot dt$$

or
$$I_0 = \frac{V_m}{\omega L_s} [\cos \alpha - \cos (\alpha + \mu)]$$

It is seen from Fig. ( ) (middle figure) that output voltage v_0 is zero from α to $(\alpha + \mu)$. Thus the average output voltage V_0 is given by

$$V_0 = \frac{V_m}{\pi} \int_{(\alpha+\mu)}^{(\alpha+\pi)} \sin \omega t \cdot d(\omega t) = \frac{V_m}{\pi} [\cos (\alpha + \mu) - \cos (\alpha + \pi)]$$

$$= \frac{V_m}{\pi} [\cos \alpha + \cos (\alpha + \mu)]$$

From Eq. ( ), $\cos (\alpha + \mu) = \cos \alpha - \dfrac{\omega L_s}{V_m} I_0$

5b)

Solution. The *dc* load current, from Eq. (6.71), is given by

$$I_o = \frac{V_m}{\omega L_s}[\cos\alpha - \cos(\alpha+\mu)]$$

Let μ_1 be the overlap angle for firing angle α_1.

$$\therefore \quad I_o = \frac{V_m}{\omega L_s}[\cos\alpha - \cos(\alpha+\mu)] = \frac{V_m}{\omega L_s}[\cos\alpha_1 - \cos(\alpha_1+\mu_1)]$$

or $$\cos\alpha_1 - \cos(\alpha_1+\mu_1) = \cos\alpha - \cos(\alpha+\mu)$$

It is given that for $\alpha = 0$, $\mu = 15°$

$$\therefore \quad \cos\alpha_1 - \cos(\alpha_1+\mu_1) = \cos 0° - \cos(0+15°) = 1 - \cos 15° = 0.03407$$

or $$\cos(\alpha_1+\mu_1) = \cos\alpha_1 - 0.03407$$

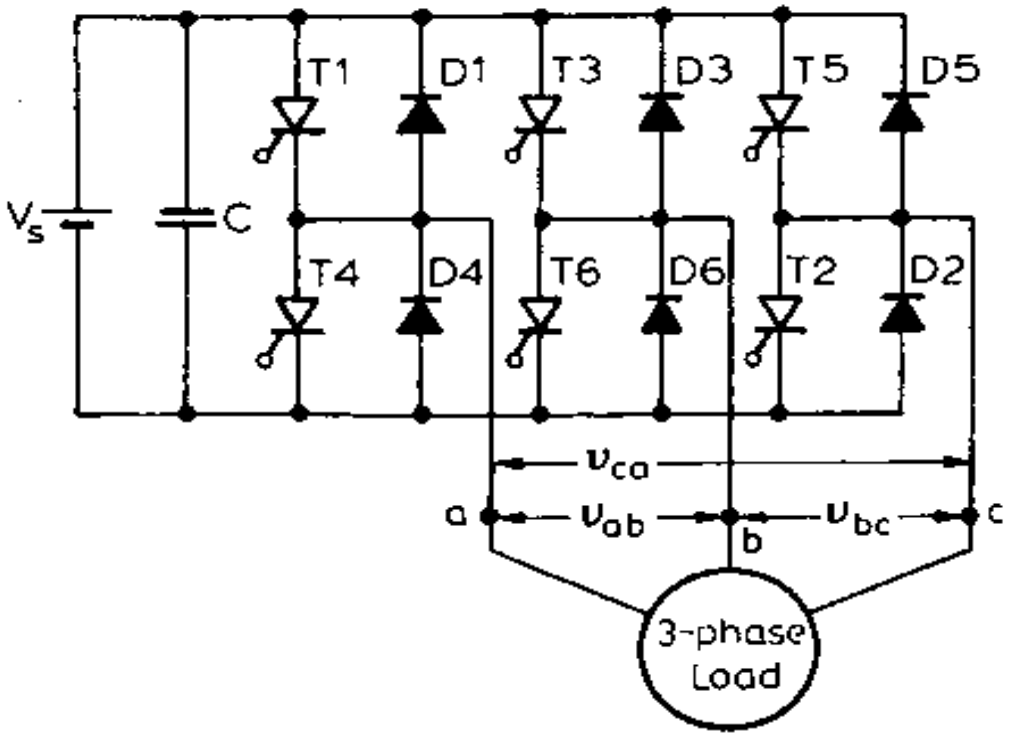
(a) For firing angle $\alpha_1 = 30°$, $\cos(30+\mu_1) = \cos 30 - 0.03407$ $\quad \therefore \mu_1 = 3.7°$.

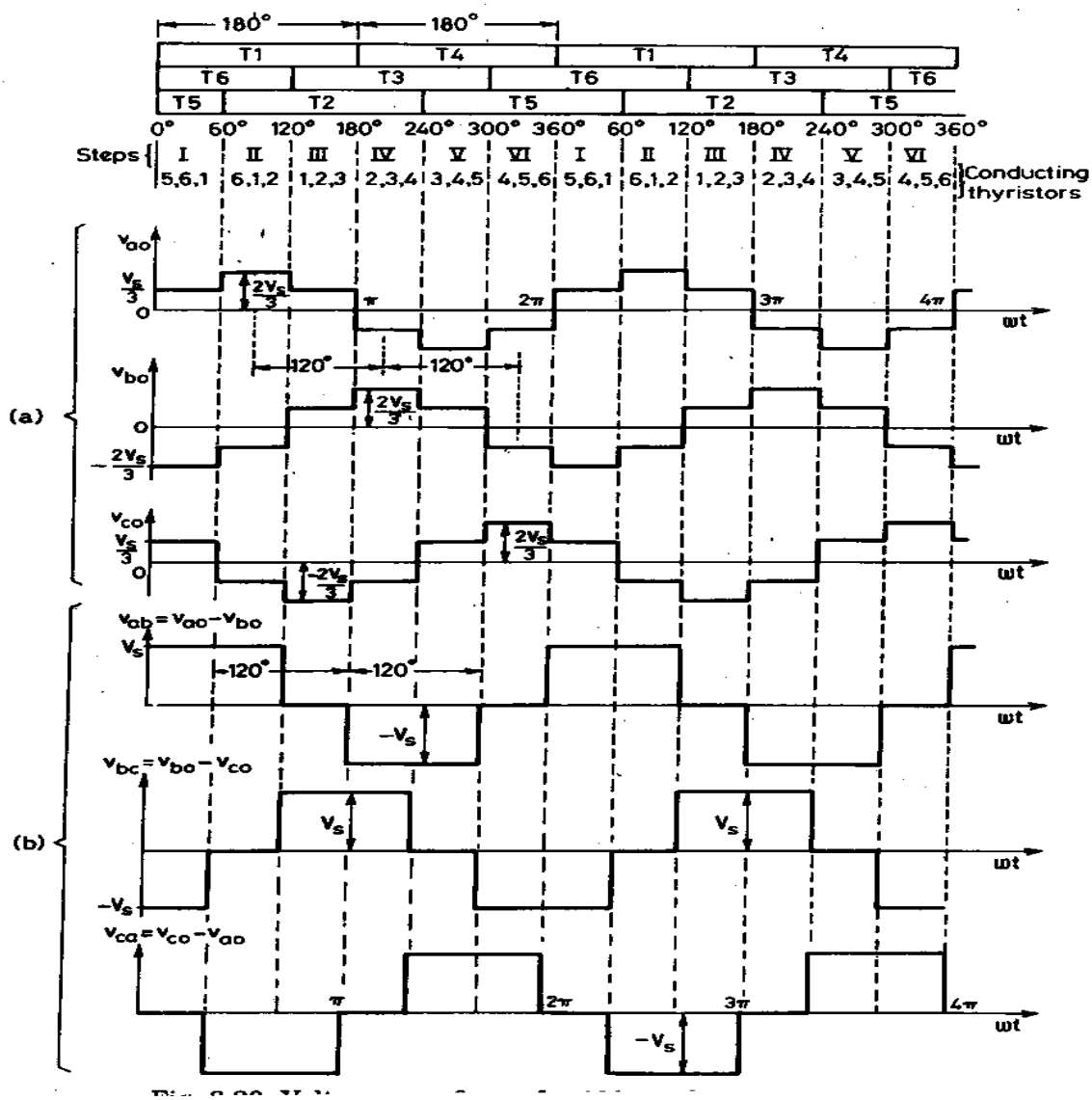
(b) For $\alpha_2 = 45°$, $\cos(45+\mu_1) = \cos 45° - 0.03407$ $\quad \therefore \mu_1 = 2.7°$

6a)

Three-phase 180 Degree Mode VSI

In the three-phase inverter of Fig. 8.19, each SCR conducts for 180° of a cycle. Thyristor pair in each arm, *i.e.* T1, T4 ; T3, T6 and T5, T2 are turned on with a time interval of 180°.





It means that T1 conducts for 180° and T4 for the next 180° of a cycle. Thyristors in the upper group, *i.e.* T1, T3, T5 conduct at an interval of 120°. It implies that if T1 is fired at $\omega t = 0°$, then T3 must be fired at $\omega t = 120°$ and T5 at $\omega t = 240°$. Same is true for lower group of SCRs. On the basis of this firing scheme, a table is prepared as shown at the top of Fig. 8.20. In this table, first row shows that T1 from upper group conducts for 180°, T4 for the next 180° and then again T1 for 180° and so on. In the second row, T3 from the upper group is shown to start conducting 120°after T1 starts conducting. After T3 conduction for 180°, T6 conducts for the next 180° and again T3 for the next 180° and so on. Further, in the third row, T5 from the upper group starts conducting 120° after T3 or 240° after T1. After T5 conduction for 180°, T2 conducts for the next 180°, T5 for the next 180° and so on. In this manner, the pattern of firing the six SCRs is identified. This table shows that T5, T6, T1 should be gated for step I ; T6, T1, T2 for step II ; T1, T2, T3 for step III ; T2, T3, T4 for step IV and so on. Thus the sequence of firing the thyristors is T1, T2, T3, T4, T5, T6 ; T1, T2.... It is seen from the table that in every step of 60° duration, only three SCRs are conducting-one from upper group and two from the lower group or two from the upper group and one from the lower group.

During step I, $0 \le \omega t < \frac{\pi}{3}$, Fig. - (a), thyristors conducting 5, 6, 1.

Current, $$i_1 = \frac{V_s}{Z + \frac{Z}{2}} = \frac{2}{3} \cdot \frac{V_s}{Z}$$

The line to neutral voltages are

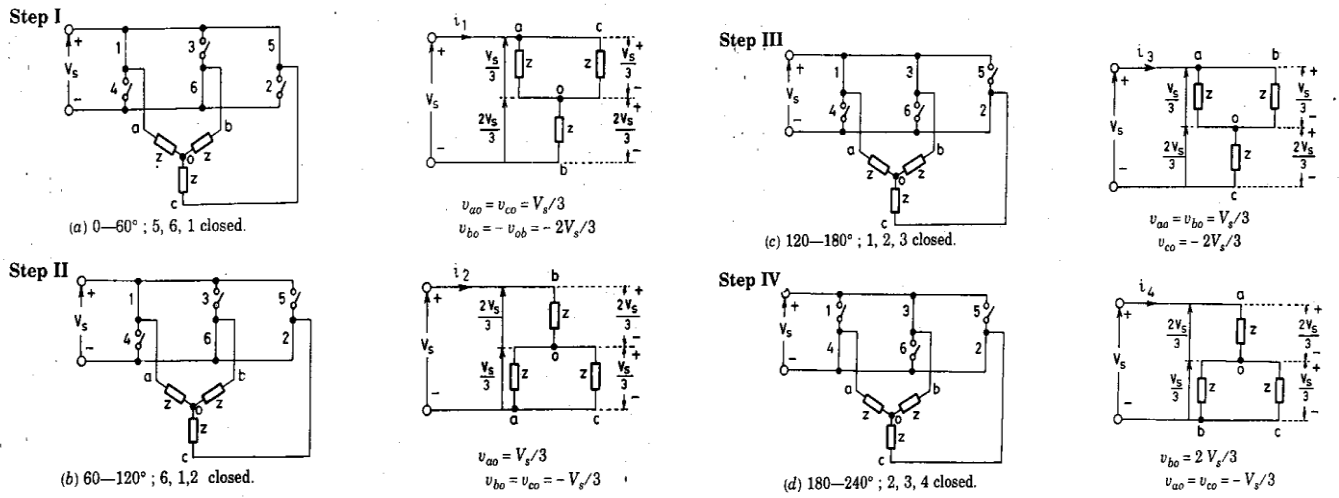
$$v_{ao} = v_{co} = i_1 \frac{Z}{2} = \frac{V_s}{3}$$

$$v_{0b} = i_1 Z = \frac{2 V_s}{3}$$

$$i_2 = \frac{2}{3} \frac{V_s}{Z}$$

$$v_{a0} = i_2 Z = \frac{2 V_s}{3} \; ; \; v_{0b} = v_{0c} = i_2 \frac{Z}{2} = \frac{V_s}{3}$$

$$v_{a0} = \frac{2V_s}{3}, \; v_{b0} = v_{c0} = -\frac{V_s}{3}.$$



The line voltage waveforms shown in Fig. 8.20 represent a balanced set of three-phase alternating voltages. During the six intervals, these voltages are well defined. Therefore, these voltages are independent of the nature of load circuit which may consist of any combination of resistance, inductance and capacitance and the load may be balanced or unbalanced, linear or nonlinear.

Fourier series expansion of line to neutral voltage v_{ao} in Fig. ... is given by

$$v_{ao} = \sum_{n = 6k \pm 1}^{\infty} \frac{2 V_s}{n\pi} \sin n\omega t$$

where $k = 0, 1, 2, \ldots$

Rms value of fundamental line voltage,

$$V_{L1} = \frac{4\,V_s}{\sqrt{2}\cdot\pi}\cos\frac{\pi}{6} = 0.7797\,V_s$$

It is seen from line voltage waveform v_{ab} in Fig. ... that line voltage is to 120°. Therefore, rms value of line voltage V_L is

$$V_L = \left[\frac{1}{\pi}\int_0^{2\pi/3} V_s^2\, d\,(\omega t)\right]^{1/2} = \sqrt{\frac{2}{3}}\,V_s = 0.8165\,V_s$$

Rms value of phase voltage V_p is

$$V_p = \frac{V_L}{\sqrt{3}} = \frac{\sqrt{2}}{3}\,V_s = 0.4714\,V_s$$

Rms value of fundamental phase voltage, from Eq. (8.47), is

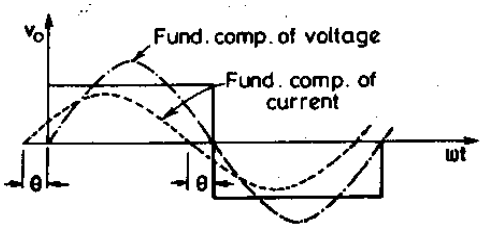
$$V_{p1} = \frac{2V_s}{\sqrt{2}\,\pi} = 0.4502\,V_s = \frac{V_{L1}}{\sqrt{3}}$$

7a)

VSI	CSI
VSI is fed from a DC voltage source having small or negligible impedance.	CSI is fed with adjustable current from a DC voltage source of high impedance.
Input voltage is maintained constant	The input current is constant but adjustable.
Output voltage does not dependent on the load	The amplitude of output current is independent of the load.
The waveform of the load current as well as its magnitude depends upon the nature of load impedance.	The magnitude of output voltage and its waveform depends upon the nature of the load impedance.
VSI requires feedback diodes	The CSI does not require any feedback diodes.
The commutation circuit is complicated	Commutation circuit is simple as it contains only capacitors.
Power BJT, Power MOSFET, IGBT, GTO with self commutation can be used in the circuit.	They cannot be used as these devices have to withstand reverse voltage.

7b)

Solution. The value of C should be such that RLC load is underdamped. Moreover when load voltage passes through zero, the load current must pass through zero before the voltage wave, *i.e.* the load current must lead the load voltage by an angle θ as shown in Fig. . . Recall the phasor diagam for RLC series circuit. From this phasor diagram,



. . Pertaining to Example 8.3.

$$\tan\theta = \frac{X_C - X_L}{R}$$

Here $X_C > X_L$ as the current is leading the voltage. Now (θ/ω) must be at least equal to circuit turn-off time, *i.e.* $1.5 \times 10 = 15$ μsec.

$$\therefore \quad \frac{\theta}{\omega} = 15 \times 10^{-6} \text{ sec}$$

Now $$f = \frac{10^3}{0.1} = 10^4 \text{ Hz}$$

$$\therefore \quad \theta = 2\pi \times 10^4 \times 15 \times 10^{-6} = 0.9424778 \text{ rad} = 54°$$

$$\therefore \quad \tan 54° = \frac{X_C - 10}{2}$$

or $$X_C = 12.752764 = \frac{1}{2\pi \times 10^4 \times C}$$

or $$C = 1.248 \ \mu\text{F}.$$

8a)

Voltage-Commutated Chopper

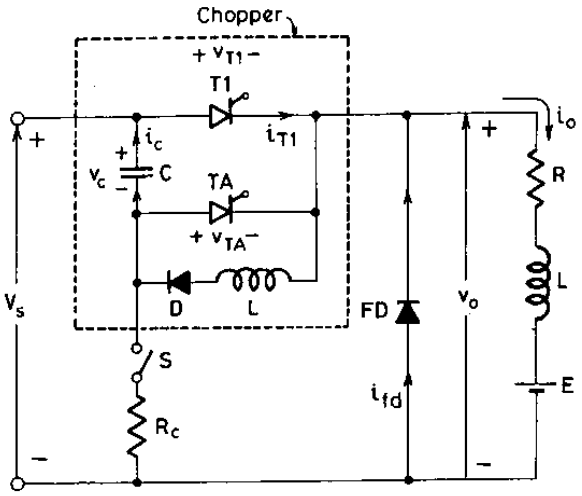
One of the earliest chopper circuits which has been in wide use is the voltage-commutated chopper. This chopper is generally used in high-power circuits where load fluctuation is not very large. This chopper is also known as *parallel-capacitor turn-off chopper, impulse-commutated chopper* or *classical chopper.* Fig. 7.21 gives the power circuit diagram for this type of chopper. In this diagram, thyristor T1 is the main power switch. Commutation circuitry for this chopper is made up of an auxiliary thyristor *TA*, capacitor *C*, diode *D* and inductor *L*. *FD* is the freewheeling diode connected across the RLE type load.

Working of this chopper can start only if the capacitor C is charged with polarities as marked in Fig. 7.21. This can be achieved in one of the two ways as under :

(*i*) Close switch S so that capacitor gets charged to voltage V_s through source V_s, C, S and charging resistor R_C. Switch S is then opened.

(*ii*) Auxiliary thyristor TA is triggered so that C gets charged through source V_s, C, TA and the load. The charging current through capacitor C decays and as it reaches zero, $v_c = V_s$ and TA is turned off.

With capacitor C charged with the polarities as shown in Fig. 7.21, the chopper circuit is ready for operation. The current

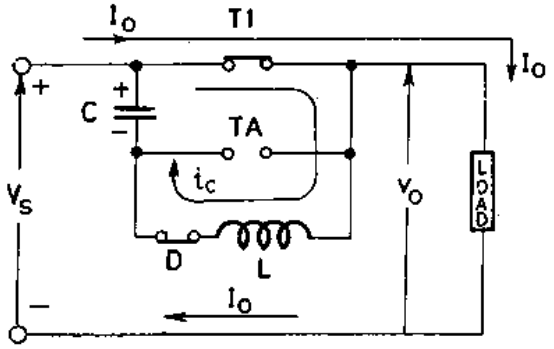


. . Voltage-commutated chopper.

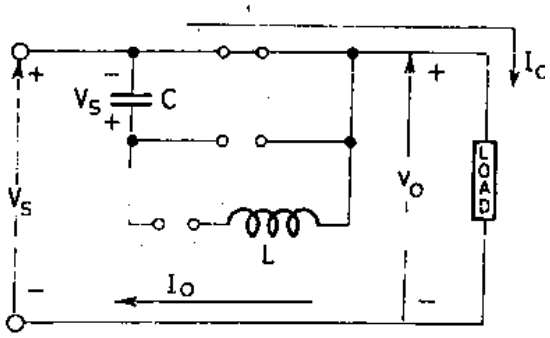
Mode I. The main thyristor is triggered at $t = 0$ and RLE load gets connected across source V_s so that load voltage $v_0 = V_s$. During this mode, there are two current paths as shown in Fig. 7.22 (a). Load current I_0 constitute one path and commutation current i_c the other path. Load current I_0 flows through source V_s, main thyristor T1 and load whereas the current i_c flows through the oscillatory circuit formed by C, T_1, L and D. The capacitor (or commutation) current first rises from zero to a maximum value when voltage across C is zero at $t = t_1/2$. As i_c decreases to zero, capacitor is charged to voltage $(-V_s)$ as shown at $t = t_1$ in Fig. 7.23, see Example 7.12. The capacitor current changes sinusoidally whereas the capacitor voltage cosinusoidally from $t = 0$ to $t = t_1$. This voltage is held constant at $(-V_s)$ by diode D. Voltage across TA is $(-V_s)$ at $t_1 = 0$, zero at $t_1/2$ and V_s at t_1, this variation is shown as cosine wave in Fig. 7.22. The thyristor current i_{T1} has a peak at $t_1/2$, because $i_{T1} = i_C + I_0$ between $t = 0$ and $t = t_1$. At the end of mode I, *i.e.* at t_1 ; $i_C = 0$, $i_{T1} = I_0$, $v_c = -V_s$, $v_{TA} = V_s$, $v_0 = V_s$ as shown in Fig. 7.23.

Mode II. The conditions existing at t_1 continue during mode II. In other words, for $t_1 \le t < t_2$, $i_c = 0$, $i_{T1} = I_0$, $v_c = V_s$, $v_{TA} = V_s$, $v_0 = V_s$, $i_D = 0$ as shown. Note that during this mode, only main SCR T1 is conducting.

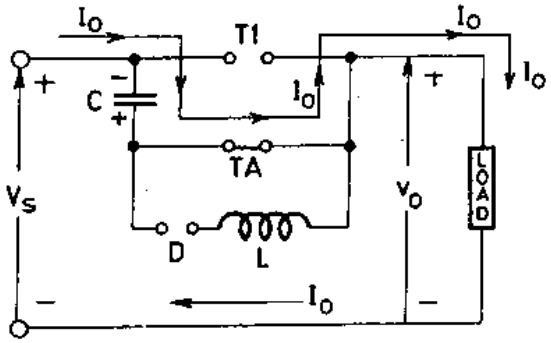
Mode III. When main thyristor T1 is to be turned off, auxiliary thyristor TA is triggered



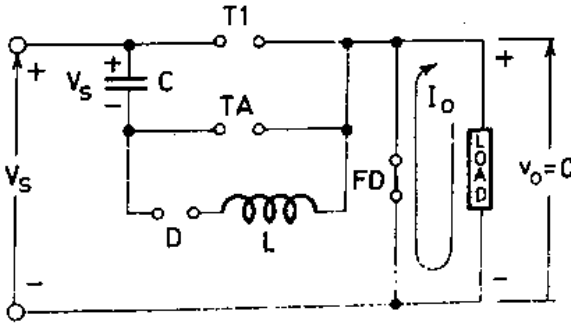
(*a*) Mode I, $0 < t < t_1$



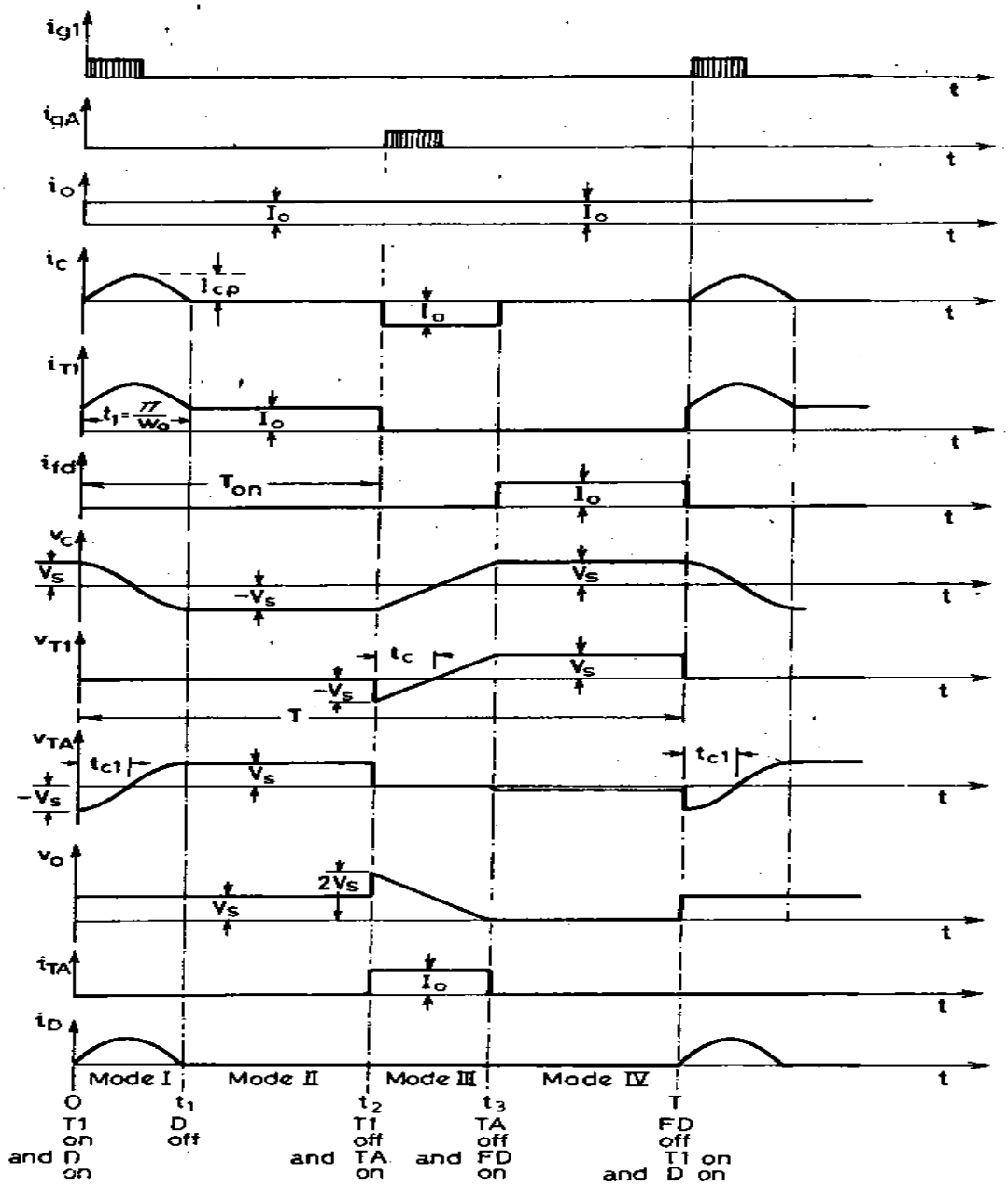
(*b*) Mode II, $t_1 \le t \le t_2$



(*c*) Mode III, $t_2 \le t < t_3$



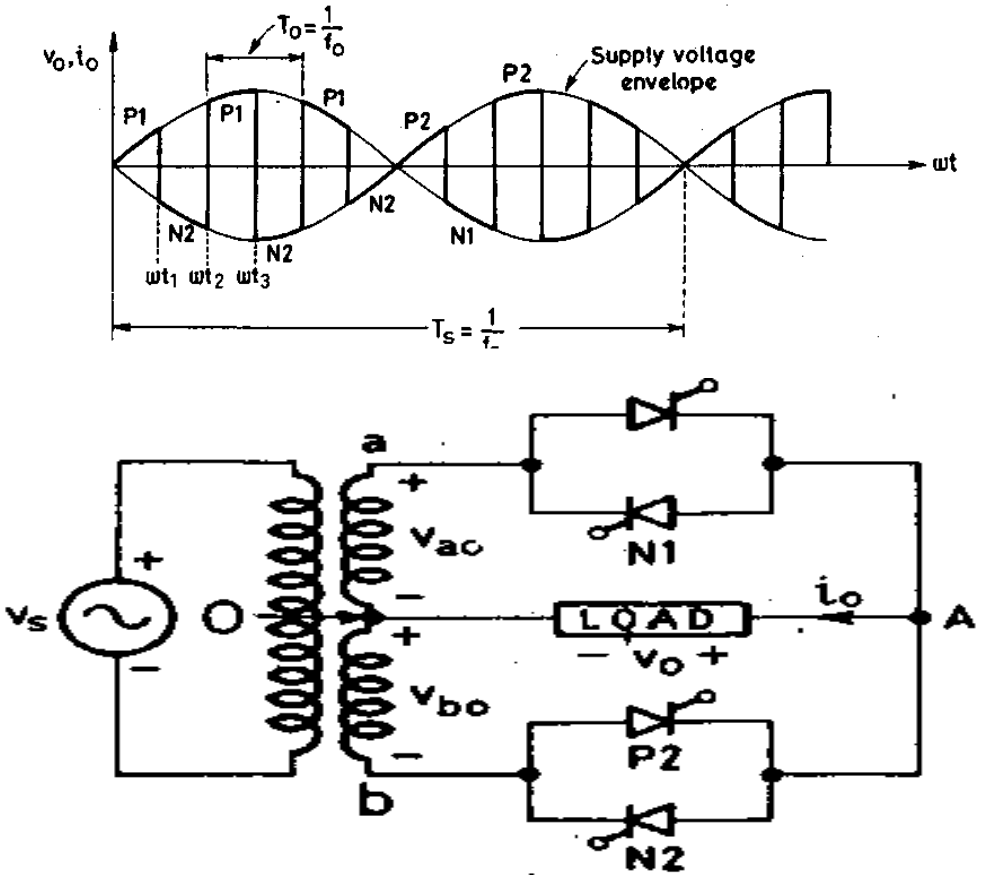
(*b*) Mode IV, $t_3 < t < T$



Mode IV. For this mode, $t_3 \leq t < T$. At t_3, $v_c = v_{T1} = V_s$, $v_0 = 0$, i_c or i_{TA} becomes zero and TA is therefore turned off naturally. As capacitor is slightly overcharged at t_3, freewheeling diode FD gets forward biased. The load current after t_3 freewheels through the load and FD, see Fig. 7.22 (*d*). Note that during freewheeling period from t_3 to T, v_{TA} is slightly negative as C is somewhat overcharged. During this mode, $i_c = 0$, $i_{T1} = 0$, $i_{fd} = I_0$, $v_{T1} = V_s$, $v_c = V_s + \Delta V$, $v_{TA} = -\Delta V$, $v_0 = 0$, $i_{TA} = 0$.

9a)

Mid-point cycloconverter. It consists of a single-phase transformer with mid-tap on the secondary winding and four thyristors. Two of these thyristors P1, P2 are for positive group and the other two N1, N2 are for the negative group. Load is connected between secondary winding mid-point 0 and terminal A as shown in Fig. 10.1 (a). Positive directions for output voltage v_0 and output current i_0 are marked in Fig. 10.1.

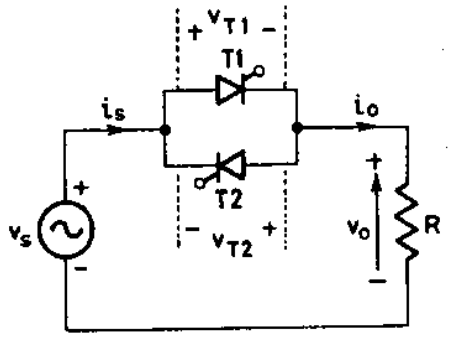


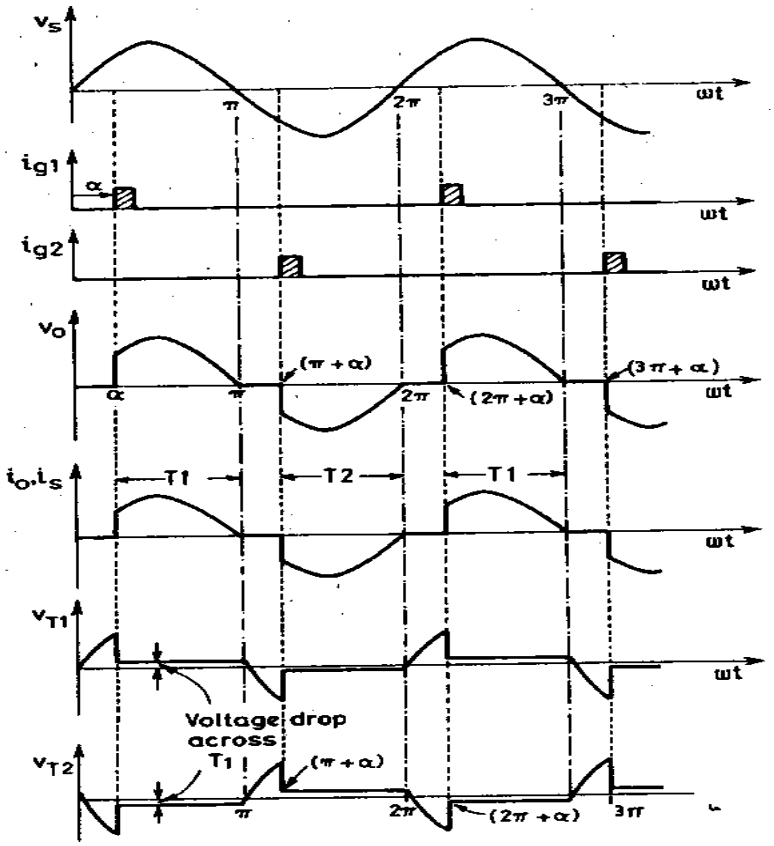
In Fig. [illegible], during the positive half cycle of supply voltage of Fig. [illegible] terminal a is positive with respect to terminal b. Therefore, in this positive half cycle, both SCRs P1 and N2 are forward biased from $\omega t = 0$ to $\omega t = \pi$. As such SCR P1 is turned on at $\omega t = 0°$ so that load voltage is positive with terminal A positive and 0 negative. The load voltage now follows the positive envelope of the supply voltage, Fig. 10.2. At instant ωt_1, P1 is force commutated and forward-biased thyristor N2 is turned on so that load voltage is negative with terminal 0 positive and A negative. The load, or output, voltage now traces the negative envelope of the supply voltage, Fig. 10.2. At ωt_2, N2 is force commutated and P1 is turned on, the load voltage is now positive and follows the positive envelope of supply voltage, Fig. [illegible]. After $\omega t = \pi$, terminal b is positive with respect to terminal a ; both SCRs P2 and N1 are therefore forward biased from $\omega t = \pi$ to 2π. At $\omega t = \pi$, N2 is force commutated and forward biased SCR P2 is turned on. At $\omega t = \frac{1}{2f_s} + \frac{1}{2f_o}$, P2 is force commutated and forward biased SCR N1 is turned on. In this manner, thyristors P1, N2 for first half cycle ; P2, N1 in the second half cycle and so on are switched alternately between positive and negative envelopes at a high frequency. As a result, output voltage of frequency f_0, higher than the supply frequency f_s, is obtained In Fig. [illegible], f_s is the supply frequency and f_0 is the output frequency. Also $f_0 = 6 f_s$ in Fig.

9b)

Single-phase Voltage Controller with R Load

Fig. [illegible] shows a single-phase voltage controller feeding power to a resistive load R. As stated before, two thyristors are connected in ant parallel. Waveforms for source voltage v_s, gating pulses i_{g1}, i_{g2}, load current i_0, source current i_s, load voltage v_0, voltage across T1 as v_{T1} and that across T2 as v_{T2} are shown in Fig. [illegible]





$$V_{or} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2 \omega t \cdot d(\omega t)\right]^{1/2}$$

$$= \frac{V_m}{\sqrt{2}}\left[\frac{1}{\pi}\left\{(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right\}\right]^{1/2}$$

$$I_{or} = \frac{V_{or}}{R} = \text{rms value of load, or source current}$$

(b) Voltage and current waveforms for [illegible]

Thyristors T1 and T2 are forward biased during positive and negative half cycles respectively. During positive half cycle, T1 is triggered at a firing angle α. T1 starts conducting and source voltage is applied to load from α to π. At π, both v_0, i_0 fall to zero. Just after π, T1 is subjected to reverse bias, it is therefore turned off. During negative half cycle, T2 is triggered at (π + α). T2 conducts from π + α to 2π. Soon after 2π, T2 is subjected to a reverse bias, it is therefore commutated. Load and source currents have the same waveform.

From zero to α, T1 is forward biased, $v_{T1} = v_s$ as shown. From α, T1 conducts, v_{T1} is therefore about 1 V. After π, T1 is reverse biased by source voltage, therefore $v_{T1} = v_s$ from

π to $\pi + \alpha$. From $\pi + \alpha$ to 2π, T2 conducts ; T1 is therefore reverse biased by voltage drop across T2 which is about 1 to 1.5 V. The voltage variation v_{T1} across SCR T1 is shown in Fig. . . . . Similarly, the variation of voltage v_{T2} across T2 can be drawn. In Fig. . . . , voltage drop across thyristors T1 and T2 is purposely shown just to highlight the duration of reverse bias across T1 and T2. Examination of this figure reveals that for any value of α, each thyristor is reverse biased for π/ω sec.

There is thus no restriction on the value of firing angle α. Firing angle can, therefore, be controlled from zero to π and rms output voltage from V_s to zero. Here V_s is the rms value of source voltage.

$\therefore$ Circuit turn-off time, $t_c = \frac{\pi}{\omega}$ sec.

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