18EED23

Hall Ticket Number:

IV/IV B.Tech (Regular/Supplementary) DEGREE EXAMINATION

November, 2022 — **Electrical and Electronics Engineering**

Seventh Semester — **Switched Mode Power Supply**

Time: Three Hours — **Maximum:** 50 Marks

Answer Question No.1 compulsorily. (10X1 = 10 Marks)

Answer ONE question from each unit. (4X10=40 Marks)

1.	a)	List the design constraints of Inductor?	CO1	L1	
	b)	List out different type of capacitors in power electronic systems?	CO1	L2	
	c)	What are various steady state analysis requirements for power electronic devices?	CO1	L3	
	d)	Draw the magnitude plot of phase lead compensator?	CO2	L1	
	e)	Write the transfer function of buck converter in terms of duty ratio?	CO2	L3	
	f)	List out various feedback compensators?	CO2	L4	
	g)	What are zvs and zcs converters?	CO2	L3	
	h)	How load resonant converters are classified?	CO3	L1	
	i)	Explain the concept of PWM technique?	CO4	L3	
	j)	What are the various types of pulse width modulated rectifiers?	CO4	L4	
		Unit -I			
2.	a)	Explain about design constraints of capacitor in power electronic systems?	CO1	L1	5M
	b)	Explain about Input filter design specifications?	CO1	L3	5M
		(OR)			
3.	a)	Explain about design constraints of transformer in power electronic systems?	CO1	L1	5M
	b)	Explain basic concepts of second and higher order switched mode power converters?	CO1	L4	5M
		Unit -II			
4.	a)	Explain about control action of feedback compensators?	CO2	L2	4M
	b)	Obtain the gain and phase plot of the non-ideal boost converter from its transfer function.	CO2	L4	6M
		(OR)			
5.	a)	Explain about frequency programmed concepts in switched mode power converters?	CO2	L2	5M
	b)	Obtain the gain and phase plot of the non-ideal buck converter from its transfer function.	CO2	L1	5M
		Unit -III			
6.	a)	Explain about zero-voltage switching converters with wave forms?	CO3	L1	5M
	b)	Explain about Multi resonant converter with neat circuit diagram?	CO3	L3	5M
		(OR)			
7.	a)	Explain about zero-current switching converters with wave forms?	CO3	L2	5M
	b)	Explain load resonant converters with neat circuit diagram and wave forms?	CO3	L4	5M
		Unit -IV			
8.	a)	List the properties of Ideal rectifier?	CO4	L2	4M
	b)	Explain about three phase converter systems in PWM rectifiers?	CO4	L1	6M
		(OR)			
9.	a)	Explain about single phase converter systems in pulse width modulated rectifiers?	CO4	L4	5M
	b)	Explain the concepts of bifurcation and chaos?	CO4	L3	5M

Scheme of Evaluation

One Mark Questions 10X1 = 10 Marks

1 a) List the design constraints of Inductor?

Ans: The design requires,

i) The size of wire to be used for the electric circuit, to carry the rated current safely.

ii) The size and shape of magnetic core to be used such that

- The peak flux is carried safely by the core without saturation.
- The required size of the conductors is safely accommodated in the core.

iii) The number of turns of the electric circuit to obtain the desired inductance

b) List out different type of capacitors in power electronic systems?

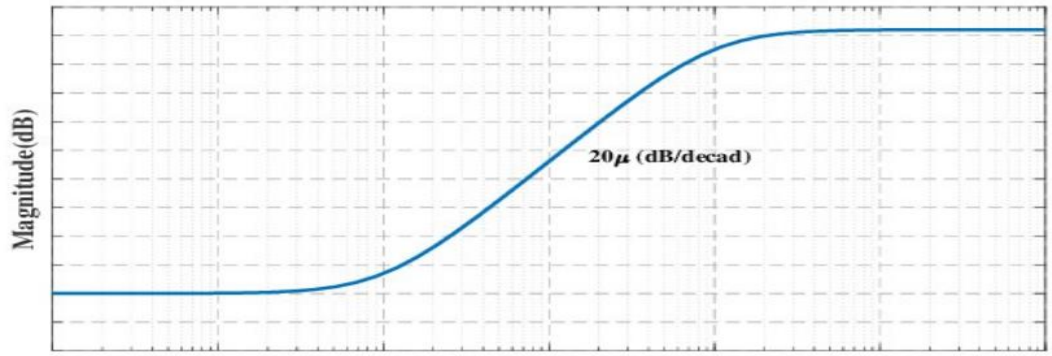
Ans: i) Coupling Capacitors ii) Power capacitors (low frequency) iii) Power capacitors (high frequency) iv) Filter capacitors v) Pulse capacitors vi) Damping capacitors vii)Commutation capacitors viii) Resonant capacitors

c) What are various steady state analysis requirements for power electronic devices?

Ans: To Analyse the behaviour of Power Electronic Converters, In first step we need to analyse the working principle of the converter using wave forms of various quantities in the converter circuit and need to use the various techniques like state space, small signal, circuit averaging etc.. to represent the physical phenomenon by its mathematical equivalent.

d) Draw the magnitude plot of phase lead compensator?

Ans:



e) Write the transfer function of buck converter in terms of duty ratio?

Ans:

$$V_0 = DV_i \quad \frac{\Delta v_{out}}{\Delta D} = \frac{V_{IN}}{1+s^2LC+s\frac{L}{R}} \quad , \quad \frac{\Delta i_L}{\Delta D} = \frac{V_{IN}}{R} \cdot \frac{1+sRC}{1+s^2LC+s\frac{L}{R}}$$

f) List out various feedback compensators?

Ans: Voltage Mode, Current Mode, Critical Conductance method, Hysteresis Method etc..

g) What are zvs and zcs converters?

Ans: Zero Volt Switching and Zero Current Switching converters are used to make the switch transition at Zero Volt Crossing and Zero Current crossing Points.

h) How load resonant converters are classified?

Ans: Series Loaded and Parallel Loaded and Hybrid Converters.

i) Explain the concept of PWM technique?

Ans: Pulse width modulation (PWM) is a modulation technique that generates variable-width pulses to represent the amplitude of an analog input signal.

j) What are the various types of pulse width modulated rectifiers?

Ans: The three conventional types of pulse width modulation are: Trail Edge Modulation. Lead Edge Modulation. Pulse Centre Two Edge Modulation. And various types of single phase and three-phase converter systems are made by incorporating ideal rectifier characteristics using the above Modulation Techniques.

2 a) Explain about design constraints of capacitor in power electronic systems?
Ans:

Power electronic systems employ capacitors as power conditioning elements. Unlike in signal conditioning applications, the capacitors in PES are required to handle large power. As a result they must be capable of carrying large current without overheating. To satisfy the demands in PES, the capacitors must be very close to their ideal characteristics namely low equivalent series resistance (ESR) and low equivalent series inductance (ESL). Low ESR will ensure low losses in the capacitor. Low ESL will ensure that the capacitor can be used in a large range of operating frequency. Figure shows the impedance of a capacitor as a function of frequency. It is seen that a real capacitor is

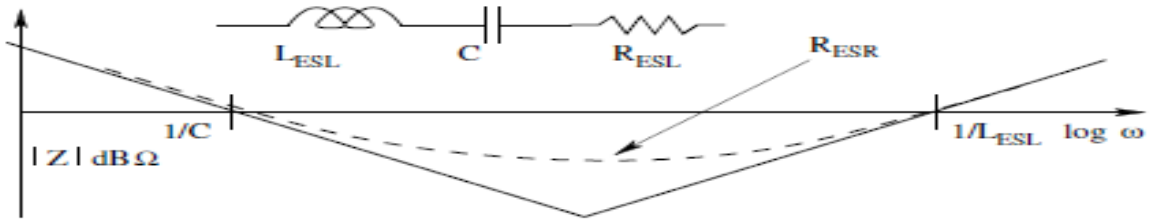


Figure Impedance of a Capacitor as a Function of Frequency

close to the ideal at lower frequencies. At higher frequencies, the ESR and the ESL of the real capacitor make it deviate from the ideal characteristics. For PES applications, it is necessary that the ESR and ESL of the capacitor are low.

There are different types of capacitors for SMPS:

i) Coupling Capacitors
ii) ii) Power capacitors (low frequency)
iii) iii) Power capacitors (high frequency)
iv) iv) Filter capacitors
v) v) Pulse capacitors
vi) vi) Damping capacitors
vii) vii)Commutation capacitors
viii) viii) Resonant capacitors

b) Explain about Input filter design specifications?
Ans:

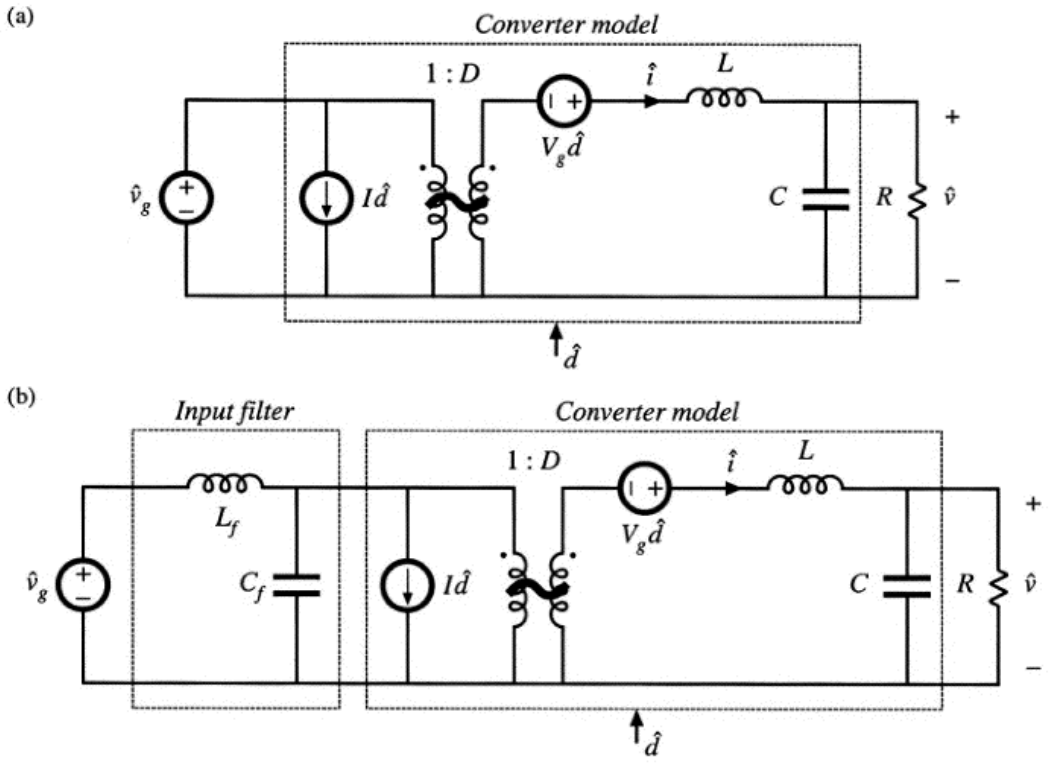


Fig. 10.3 Small-signal equivalent circuit models of the buck converter: (a) basic converter model, (b) with addition of input filter.

The situation faced by the design engineer is typically as follows. A switching regulator has been designed, which meets performance specifications. The regulator was properly designed as discussed in Chapter 9, using a small-signal model of the converter power stage such as the equivalent circuit of Fig. 10.3(a). In consequence, the transient response is well damped and sufficiently fast, with adequate phase margin at all expected operating points. The output impedance is sufficiently small over a wide frequency range. The line-to-output transfer function $G_{vg}(s)$, or *audiosusceptibility,* is sufficiently small, so that the output voltage remains regulated in spite of variations in $\hat{v}_g(t)$.

Having developed a good design that meets the above goals regarding dynamic response, the problem of conducted EMI is then addressed. A low-pass filter having attenuation sufficient to meet conducted EMI specifications is constructed and added to the converter input. A new problem then arises: the input filter changes the dynamics of the converter. The transient response is modified, and the control system may even become unstable. The output impedance may become large over some frequency range, possibly exhibiting resonances. The audiosusceptibility may be degraded.

The problem is that the input filter affects the dynamics of the converter, often in a manner that degrades regulator performance. For example, when a single-section *L-C* input filter is added to a buck converter as in Fig. 10.2(a), the small-signal equivalent circuit model is modified as shown in Fig. 10.3(b). The input filter elements affect all transfer functions of the converter, including the control-to-output transfer function $G_{vd}(s)$, the line-to-output transfer function $G_{vg}(s)$, and the converter output impedance $Z_{out}(s)$. Moreover, the influence of the input filter on these transfer functions can be quite severe.

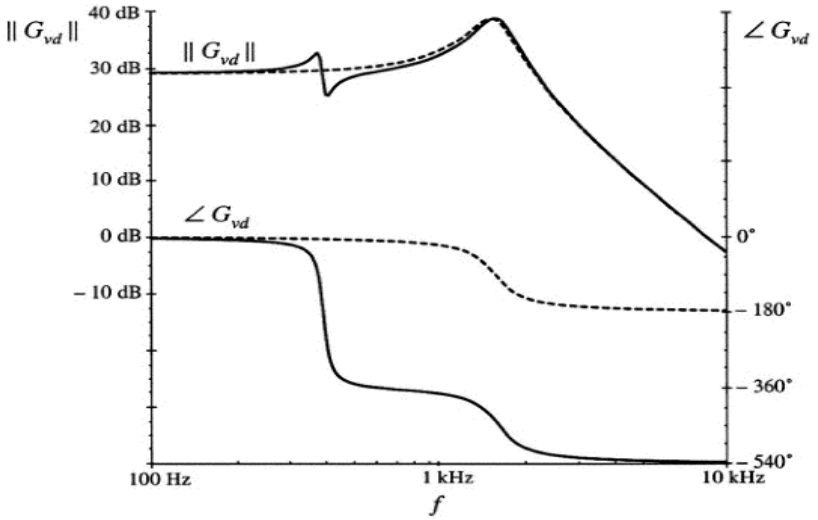


Fig. 10.4 Control-to-output transfer functions predicted by the equivalent circuit models of Fig. 10.3. *Dashed lines:* without input filter [Fig. 10.3(a)]. *Solid lines:* with input filter [Fig. 10.3(b)].

As an illustration, let's examine how the control-to-output transfer function $G_{vd}(s)$ of the buck converter of Fig. 10.1 is altered when a simple *L-C* input filter is added as in Fig. 10.2. For this example, the element values are chosen to be: $D = 0.5$, $L = 100\ \mu H$, $C = 100\ \mu F$, $R = 3\ \Omega$, $L_f = 330\ \mu H$, $C_f = 470\ \mu F$. Figure 10.4 contains the Bode plot of the magnitude and phase of the control-to-output transfer function $G_{vd}(s)$. The dashed lines are the magnitude and phase before the input filter was added, generated by solution of the model of Fig. 10.3(a). The complex poles of the converter output filter cause the phase to approach – 180° at high frequency. Usually, this is the model used to design the regulator feedabck loop and to evaluate the phase margin (*see* Chapter 9). The solid lines of Fig. 10.4 show the magnitude and phase after addition of the input filter, generated by solution of the model of Fig. 10.3(b). The magnitude exhibits a "glitch" at the resonant frequency of the input filter, and an additional - 360° of phase shift is introduced into the phase. It can be shown that $G_{vd}(s)$ now contains an additional complex pole pair and a complex right half-plane zero pair, associated with the input filter dynamics. If the crossover frequency of the regulator feedback loop is near to or greater than the resonant frequency of the input filter, then the loop phase margin will become negative and instability will result. Such behavior is typical; consequently, input filters are notorious for destabilizing switching regulator systems.

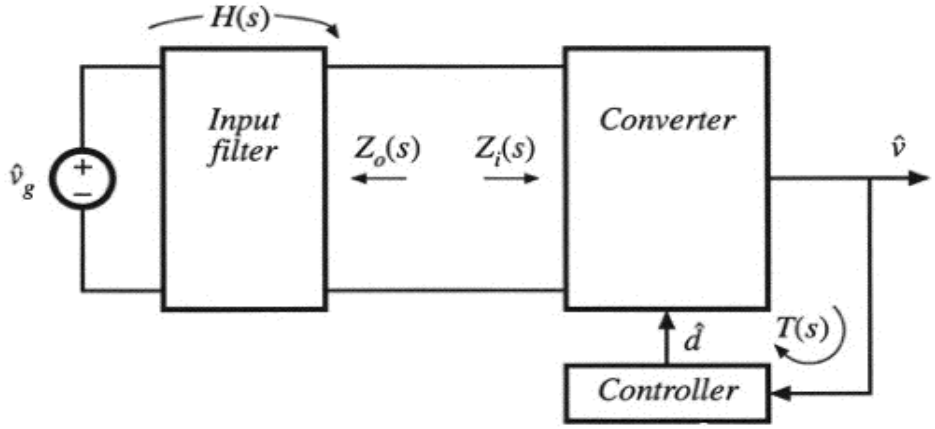


Fig. 10.5 Addition of an input filter to a switching voltage regulator system.

3 a) Explain about design constraints of transformer in power electronic systems?

Ans:

Unlike the inductor, the transformer does not store energy. The transformer consists of more than one winding. Also, in order to keep the magnetization current low, the transformer does not have air gap in its magnetizing circuit. Consider a transformer with a single primary and single secondary . Let the specifications be

Primary: V_1 volt; I_1 ampere;
Secondary: V_2 volt; I_2 ampere;
VA Rating: $V_1\ I_1 = V_2\ I_2$;
Frequency: f Hz

For square wave of operation, the voltage of the transformer is

$$V_1 = 4\ f\ B_m\ A_C\ N_1\ ;\ V_2 = 4\ f\ B_m\ A_C\ N_2$$

The window for the transformer accommodates both the primary and the secondary. With the same notation as for inductors,

$$k_w\ A_W = N_1\ I_1 + N_2\ I_2$$

From the above equations,

$$V_1\ I_1 + V_2\ I_2 = 4\ k_w\ J\ B_m\ A_C\ A_W$$

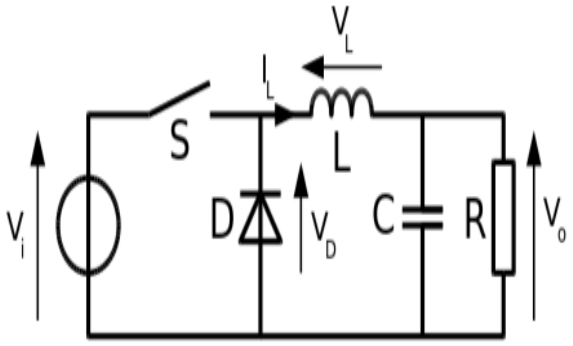
$$VA = 2\ f\ B_m\ J\ A_C\ A_W$$

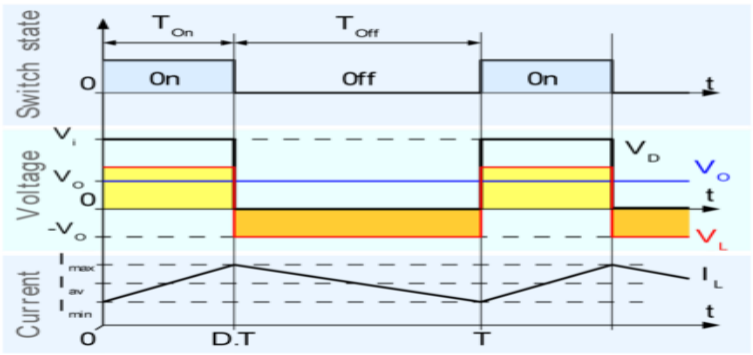
$$A_C A_W = \frac{VA}{2\ f\ B_m\ J\ k_w}$$

The above equation relates the area product $(A_C A_W)$ required for a transformer to handle a given VA rating.

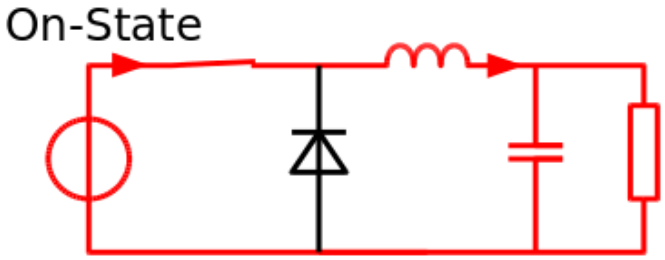
b) Explain basic concepts of second and higher order switched mode power converters?

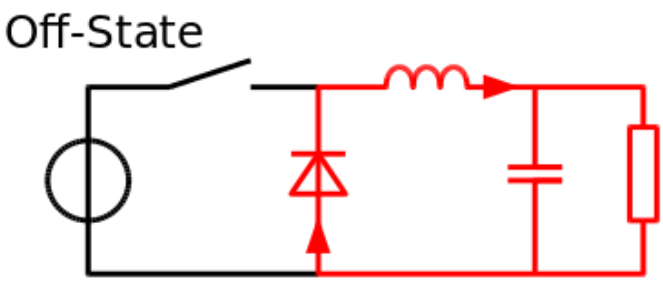
Ans: A buck converter (step-down converter) is a DC-to-DC power converter which steps down voltage (while stepping up current) from its input (supply) to its output (load). It is a class of switched-mode power supply (SMPS) typically containing at least two semiconductors (a diode and a transistor, although modern buck converters frequently replace the diode with a second transistor used for synchronous rectification) and at least one energy storage element, a capacitor, inductor, or the two in combination. To reduce voltage ripple, filters made of capacitors (sometimes in combination with inductors) are normally added to such a converter's output (load-side filter) and input (supply-side filter). Its name derives from the inductor that “bucks” or opposes the supply voltage. The basic operation of the buck converter has the current in an inductor controlled by two switches .





In a physical implementation, these switches are realized by a transistor and a diode, or two transistors





Buck converters operate in continuous mode if the current through the inductor (I_L) never falls to zero during the commutation cycle. In this mode, the operating principle is described by the plots in figure 4:

- When the switch pictured above is closed (top of figure 2), the voltage across the inductor is $V_\mathrm{L} = V_\mathrm{i} - V_\mathrm{o}$. The current through the inductor rises linearly (in approximation, so long as the voltage drop is almost constant). As the diode is reverse-biased by the voltage source V, no current flows through it;
- When the switch is opened (bottom of figure 2), the diode is forward biased. The voltage across the inductor is $V_\mathrm{L} = -V_\mathrm{o}$ (neglecting diode drop). Current I_L decreases.

The energy stored in inductor L is

$$E = \frac{1}{2} L I_\mathrm{L}^2$$

Therefore, it can be seen that the energy stored in L increases during on-time as I_L increases and then decreases during the off-state. L is used to transfer energy from the input to the output of the converter.

The rate of change of I_L can be calculated from:

$$V_\mathrm{L} = L \frac{\mathrm{d}I_\mathrm{L}}{\mathrm{d}t}$$

With V_L equal to $V_\mathrm{i} - V_\mathrm{o}$ during the on-state and to $-V_\mathrm{o}$ during the off-state. Therefore, the increase in current during the on-state is given by:

$$\Delta I_{L_\mathrm{on}} = \int_0^{t_\mathrm{on}} \frac{V_\mathrm{L}}{L}\,\mathrm{d}t = \frac{V_\mathrm{i} - V_\mathrm{o}}{L} t_\mathrm{on}, \qquad t_\mathrm{on} = DT$$

where D is a scalar called the duty cycle with a value between 0 and 1.

Conversely, the decrease in current during the off-state is given by:

$$\Delta I_{L_{\text{off}}} = \int_{t_{\text{on}}}^{T=t_{\text{on}}+t_{\text{off}}} \frac{V_{\text{L}}}{L}\,\mathrm{d}t = -\frac{V_{\text{o}}}{L}t_{\text{off}}, \qquad t_{\text{off}} = (1-D)T$$

Assuming that the converter operates in the steady state, the energy stored in each component at the end of a commutation cycle T is equal to that at the beginning of the cycle. That means that the current I_{L} is the same at $t = 0$ and at $t = T$ (figure 4).

So, from the above equations it can be written as:

$$\Delta I_{L_{\text{on}}} + \Delta I_{L_{\text{off}}} = 0$$

$$\frac{V_{\text{i}} - V_{\text{o}}}{L}t_{\text{on}} - \frac{V_{\text{o}}}{L}t_{\text{off}} = 0$$

4 a) Explain about control action of feedback compensators?

Ans: The compensated systems are shown in Series or cascade compensation, Feedback or parallel compensation, and State feedback compensation have one degree of freedom which intimates that the system has a single controller. The disadvantage of one degree of freedom controller is that the performance criteria realized using these -compensation techniques are limited.

In simple words, the compensators introduce additional poles/zeros to an -existing system so that the desired specification is achieved.

Effects of Addition of Poles
The following are the effects of addition of poles to an existing system:

The root locus of a compensated system will be shifted towards the right-hand side of the s-plane.
Stability of a system gets lowered.
Settling time of a system increases.
Accuracy of a system is improved by the reduction of steady-state error.
Effects of Addition of Zeros
The following are the effects of addition of zeros to an existing system:

The root locus of a compensated system will be shifted towards the left-hand side of the s-plane.
Stability of a system gets increased.
Settling time of a system decreases.
Accuracy of a system is lowered as steady-state error of the system increases.
Choice of Compensators
The choice of compensators from the different categories discussed in the previous sections is based on the following factors:

Nature of signal to the system
Available components
Experience of the designer
Cost
Power levels at different points and so on

b) Obtain the gain and phase plot of the non-ideal boost converter from its transfer function.
Ans:

Figure 1 shows the block diagram of the boost converter. Using the *state space averaging model*, the small-signal transfer function from the duty cycle (*D*) of the switch to the boost converter output (v_o) in continuous conduction mode (CCM) can be derived. Equation 1 through Equation 6 are well known simplified equations for this model as derived

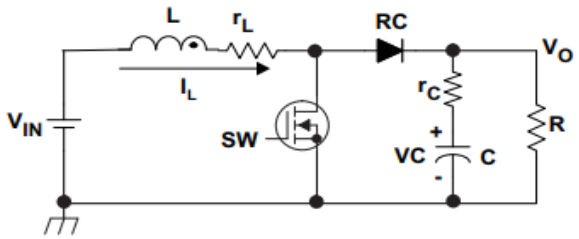


Figure 1. Boost Converter Block Diagram

$$G_{dv} = \frac{\hat{v}_O}{\hat{d}} \cong G_{do} \cdot \frac{\left(1+\frac{s}{\omega_{Z1}}\right)\cdot\left(1-\frac{s}{\omega_{RHP-zero}}\right)}{1+\frac{s}{\omega_0 \cdot Q}+\frac{s^2}{\omega_0^2}} \quad (1)$$

Where

$$G_{do} \approx \frac{V_{IN}}{(1-D)^2} = \frac{V_o^2}{V_{IN}} \quad (2)$$

$$\omega_{Z1} = \frac{1}{r_C \cdot C} \quad (3)$$

$$\omega_{RHP-zero} \approx \frac{(1-D)^2 \cdot (R-r_L)}{L} \approx \frac{R}{L}\cdot\left(\frac{V_{IN}}{V_o}\right)^2 \quad \text{or} \quad \left(f_{RHP-zero} \approx \frac{R}{2\pi \cdot L}\left(\frac{V_{IN}}{V_o}\right)^2\right) \quad (4)$$

$$\omega_0 \approx \frac{1}{\sqrt{L \cdot C}} \cdot \sqrt{\frac{r_L + (1-D)^2 \cdot R}{R}} \approx \frac{1}{\sqrt{L \cdot C}} \cdot \frac{V_{IN}}{V_o} \quad \text{or} \quad \left(f_O \approx \frac{1}{2\pi\sqrt{LC}} \cdot \frac{V_{IN}}{V_o}\right) \quad (5)$$

$$Q \approx \frac{\omega_0}{\frac{r_L}{L} + \frac{1}{C \times (R + r_C)}} \quad (6)$$

Equation 1 consists of a double-pole, RHP-zero and ESR-zero. For this discussion, the ESR-zero will be ignored because it is at a much higher frequency than the double-pole frequency and RHP-zero. Figure 2 shows a Bode plot of the double-pole transfer function.

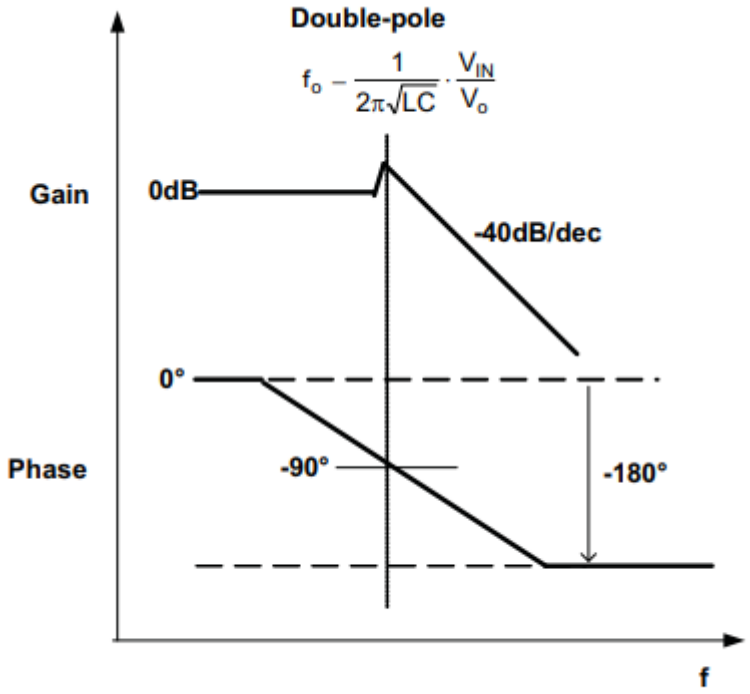


Figure 2. Bode plot of the Double-Pole Transfer Function

5 a) Explain about frequency programmed concepts in switched mode power converters?

Ans: A controller is required for the converter to maintain the output voltage constant irrespective of variations in the DC source voltage Vin and the load current.In this method as shown in fig.4 the output voltage is maintained at a constant value given by V_{ref}. The error voltage given by $V_{ref} - V$ is passed through a Controller to generate control signal V_c which is passed through PWM modulator to generate appropriate d.

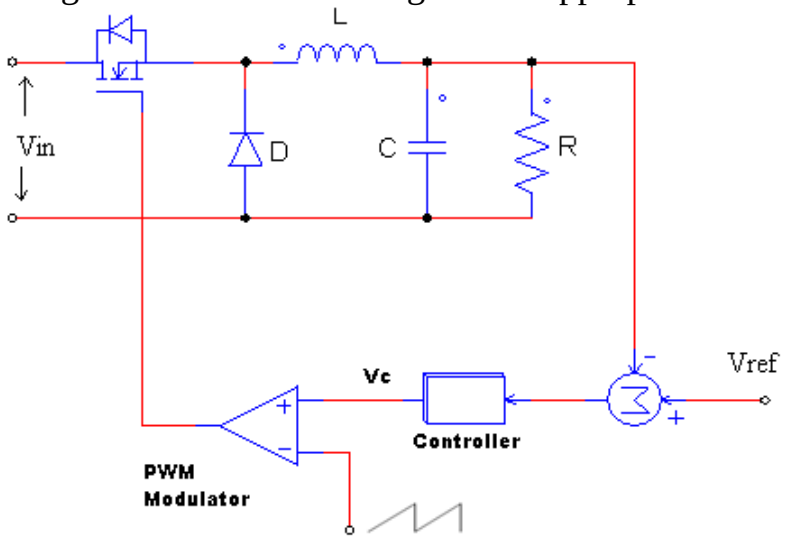


Fig.4

The above circuit is modeled and simulated in MATLAB with the fallowing parameters Vin=28v, V=15v, L=50µH, C=500µF, R=3Ω, fs=100 KHz.

Fig.5 shows the simulink block diagram. The PWM modulator is represented by a small signal gain $1/V_m$ where V_m is the peak magnitude of the saw tooth wave.

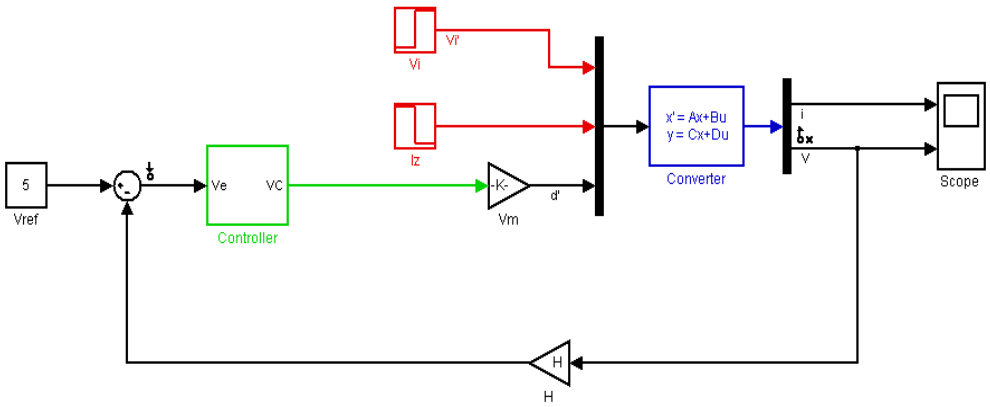


Fig.5

Fig.6 shows the uncompensated open loop control to output frequency response v/v_e. Which is having low phase margin (3deg) at 2.7 KHz.

To improve phase margin to 52 deg at 5 KHz. A lead compensator is require with zero at 1.7 KHz, Pole at 14.5 KHz and with a gain of $G_{co} = \left(\frac{1}{|T_u|}\right) * \sqrt{fz / fp} =$ 1.15

Where T_u =-10.5 db=0.298

$$f_z = 5K * \sqrt{\frac{1-\sin 52^o}{1+\sin 52^o}} = 1.7\text{KHz} \qquad f_p = 5K * \sqrt{\frac{1+\sin 52^o}{1-\sin 52^o}} = 14.5\ \text{KHz}$$

And to improve the low frequency response a inverted zero is added at one tenth of the cross over frequency i.e. at 500Hz. Finally the open loop response with the compensator is shown in fig.7 with 48 deg of phase margin at 5 KHz.

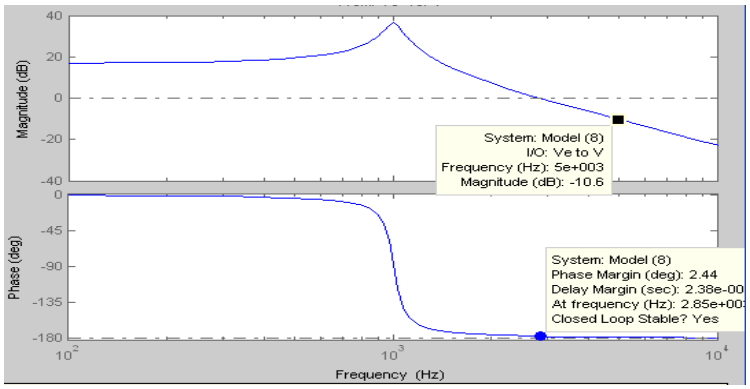


Fig.6

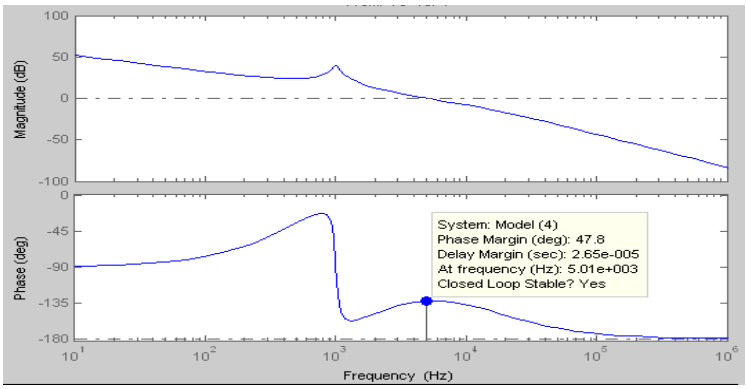


Fig.7

The simulation results are sown in fig.8. Though phase margin requirement is satisfied the initial peak over shoot is very high which can damage the circuit. So to decrease this we have to reduce the gain of the compensator which results in decreasing the phase margin as shown in Fig.9 and hence more damping nature response as shown in Fig.10 for a Step change of -5A in output current at 0.03 sec and a step change of 5v in input voltage at 0.06sec.

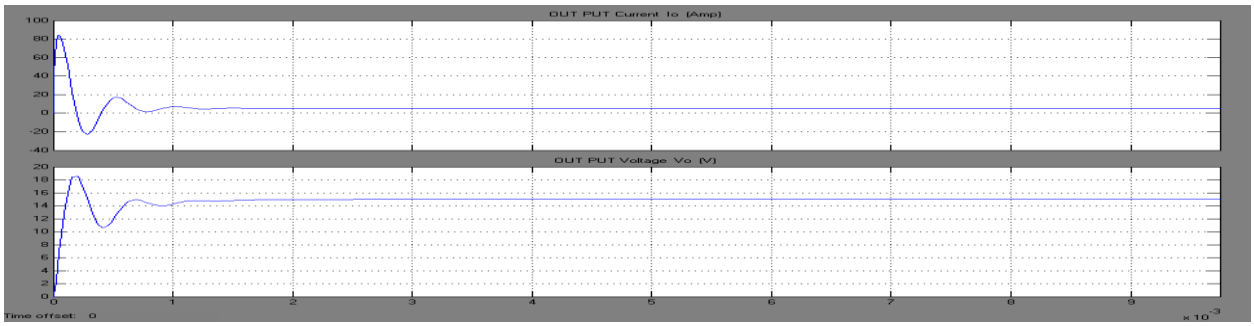


Fig.8

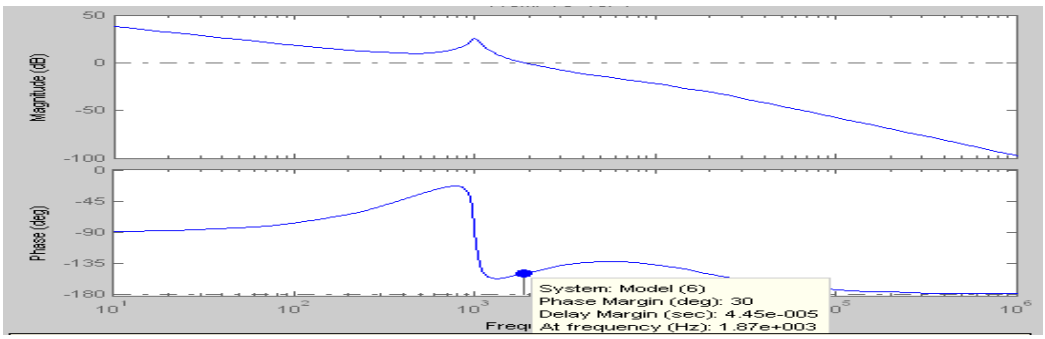
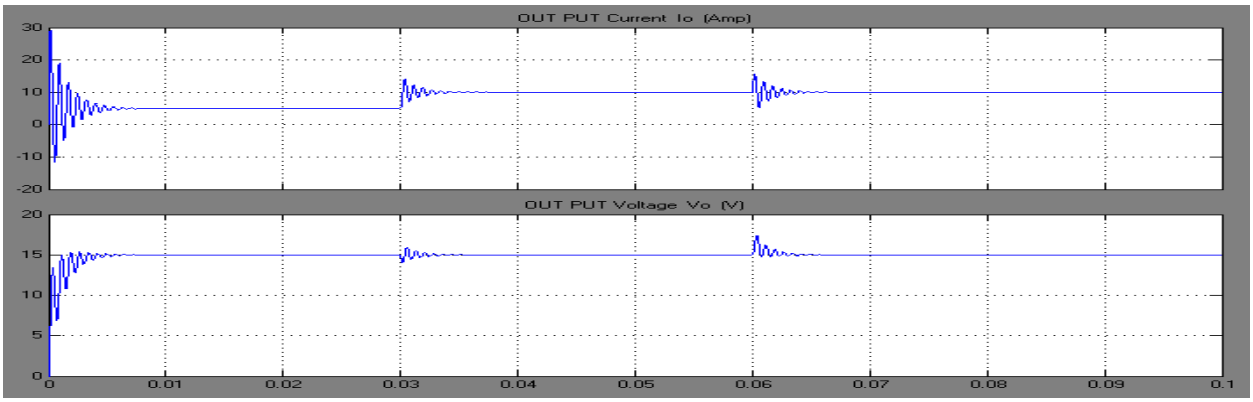


Fig.9



b) Obtain the gain and phase plot of the non-ideal buck converter from its transfer function.
Ans:

A controller is required for the converter to maintain the output voltage constant irrespective of variations in the DC source voltage Vin and the load current. So the first step in designing a controller for any converter starts with finding mathematical equations which relate input, output and controlling parameters of the converter.

State space averaging is the most common averaging technique and is used here to model the model the buck converter. In this method state space equations are obtained for each mode in one complete cycle. In continuous current mode (CCM) only two modes exists i.e. when the power switch is ON and when switch is OFF. Fig.2 shows the circuit configuration of the buck converter corresponding to ON state of power switch. In order to examine the effect of load changes on the response of the converter, a current generator i_z is added in parallel with the load resistor. Corresponding state space equations for this ON state are

$$\begin{bmatrix} \dot{i} \\ \dot{v} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix}}_{A_{ON}} \begin{bmatrix} i \\ v \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix}}_{B_{ON}} \begin{bmatrix} v_{in} \\ i_z \end{bmatrix} \longrightarrow (3)$$

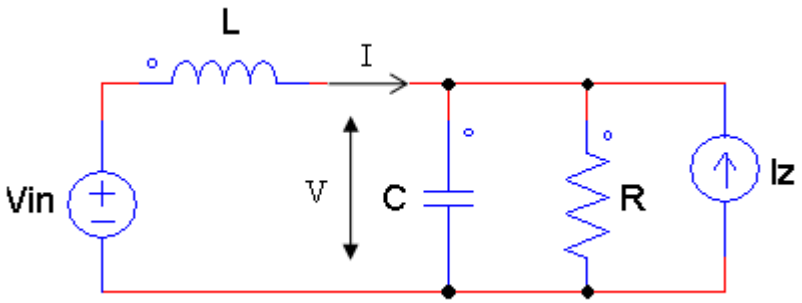


Fig.2

Fig.3 shows the circuit configuration of the buck converter corresponding to OFF state of power switch and corresponding sate space equations are

$$\begin{bmatrix} \dot{i} \\ \dot{v} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix}}_{A_{OFF}} \begin{bmatrix} i \\ v \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{C} \end{bmatrix}}_{B_{OFF}} \begin{bmatrix} v_{in} \\ i_z \end{bmatrix} \longrightarrow (4)$$

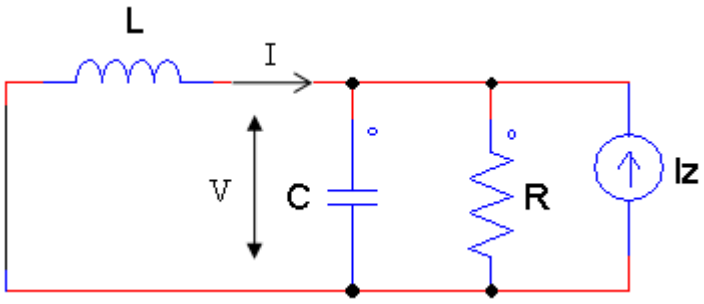


Fig.3

The inductor current 'i' and the output voltage 'v' are the two elements of a state vector x, while the input vector u has v_{in} and i_z .

The state –space averaged model of the converter is formed by taking a weighted average of the equations of fig.2 and Fig.3 as

$$\dot{x} = Ax + Bu \longrightarrow (5)$$

Where A= $dA_{ON} + (1- d) A_{OFF}$

B= $dB_{ON} + (1 – d) B_{OFF}$

Therefore the averaged matrices for the buck converter are

$$A = \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \qquad B = \begin{bmatrix} \frac{-d}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix} \longrightarrow (6)$$

The control input to the converter, duty ratio is in matrix B, therefore the averaged model is time varying and difficult to solve. To simplify the model equ.4 is linearised, by considering small variations in the variables.

Each variable is written as a sum of steady state or DC component and small signal or AC component as

$$\left.\begin{aligned} x &= X + \hat{x} \\ u &= U + \hat{u} \\ d &= D + \hat{d} \end{aligned}\right\} \longrightarrow (7)$$

Where $\hat{x} \prec\prec X$

$\hat{u} \prec\prec U$

$\hat{d} \prec\prec D$

Substituting eq.7 in eq.5 and neglecting the higher order terms, the equation which relates small changes in variables is

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} + (A_{ON} - A_{OFF})\hat{d}X + (B_{ON} - B_{OFF})\hat{d}U$$

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} + E\hat{d} \longrightarrow (8)$$

Where $E = (A_{ON} - A_{OFF})X + (B_{ON} - B_{OFF})U$

And the E matrix for buck converter is

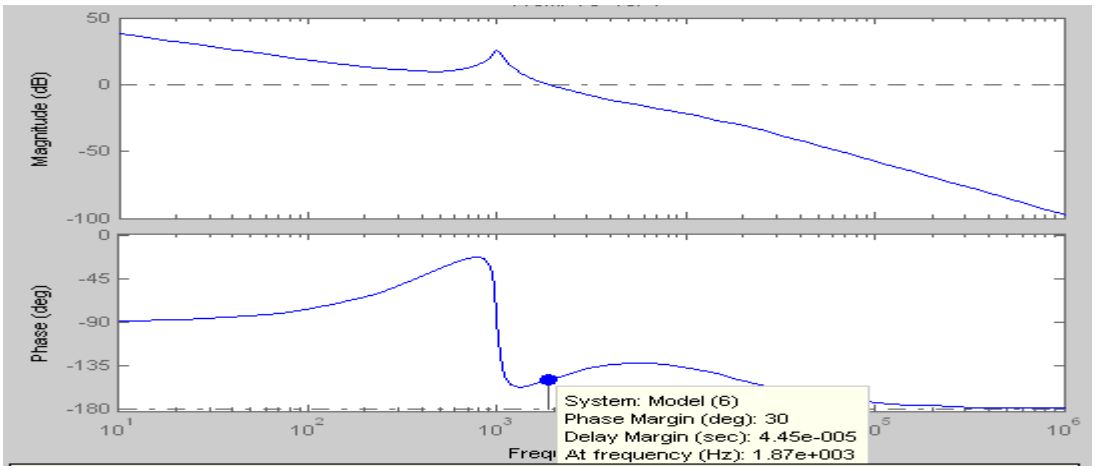
$$E = \begin{bmatrix} \frac{Vin}{L} \\ 0 \end{bmatrix} \longrightarrow (9)$$

State Model
dX/dt=AX+BU State Equation
Y=CX+DU output Equation

A= System Matrix
B=Input Matrix
C=Output Matrix
D= Direct Transistion Matrix

X= State Varibles
U=Input Variables
Y= Output Variables

T.F= C(sI-A)-1*B+D



6 a) Explain about zero-voltage switching converters with wave forms?

Ans:

In these converters, the resonant capacitor produces a zero voltage across the switch, at which instant the switch can be turned on or off. Such a step-down dc–dc converter circuit is shown in Fig. 9-31*a*, where a diode D_r is connected in antiparallel with the switch. As discussed previously, the output current i_o can be assumed to be a current of constant magnitude I_o in Fig. 9-31*a* during a high-frequency resonant cycle.

Initially, the switch is conducting I_o and therefore, $I_{Lo} = I_o$ and $V_{co} = 0$. The converter operation can be divided into the following intervals for which the converter waveforms as well as the corresponding circuit states are shown in Fig. 9-31*b* and 9-31*c*, respectively:

1. *Time interval* 1 *(between* t_0 *and* t_1*).* At time t_0, the switch is turned off. Because of C_r, the voltage across the switch builds up slowly but linearly from zero *to* V_d at t_1. This results in a zero-voltage turn-off of the switch.
2. *Time interval 2 (between* t_1 *and* t_2*).* Beyond t_1, since $v_c > V_d$, the diode D becomes forward biased, C_r and L_r resonate, and the analysis of Section 9-3-1-1 applies. At t_1', i_L goes through zero and v_c reaches its peak of $V_d + Z_0 I_o$. At t_1'', $v_c = V_d$ and $i_L = -I_o$. At t_2, the capacitor voltage reaches zero and cannot reverse its polarity because the diode D_r begins to conduct.

   Note that the load current I_o should be sufficiently large so that $Z_0 I_o > V_d$. Otherwise, the switch voltage will not come back to zero naturally and the switch will have to be turned on at a nonzero voltage, resulting in turn-on losses (the energy stored in C_r will dissipate in the switch).
3. *Time interval* 3 *(between* t_2 *and* t_3*).* Beyond t_2, the capacitor voltage is clamped to zero by D_r, which conducts the negative i_L. The gate drive to the switch is applied once its antiparallel diode begins to conduct. Now i_L increases linearly and goes through zero at time t_2', at which instant i_L begins to flow through the switch. Therefore, the switch turns on at a zero voltage and zero current. Here i_L increases linearly to I_o at t_3.
4. *Time interval 4 (between* t_3 *and* t_4*).* Once i_L reaches I_o at t_3, the freewheeling diode D turns off. Because a small negative slope is associated with di/dt through the diode at turn-off, there are no diode reverse-recovery problems like the ones encountered in the switch mode. The switch conducts I_o as long as it is kept on until t_4. The interval $t_4 - t_3$ can be controlled. At t_4, the switch is turned off and the next cycle ensues.

It is clear from the waveforms of Fig. 9-31*b* that the switch current is limited to I_o. The voltage v_{oi} across the output diode as defined in Fig. 9-31*a*, is plotted in Fig. 9-32.

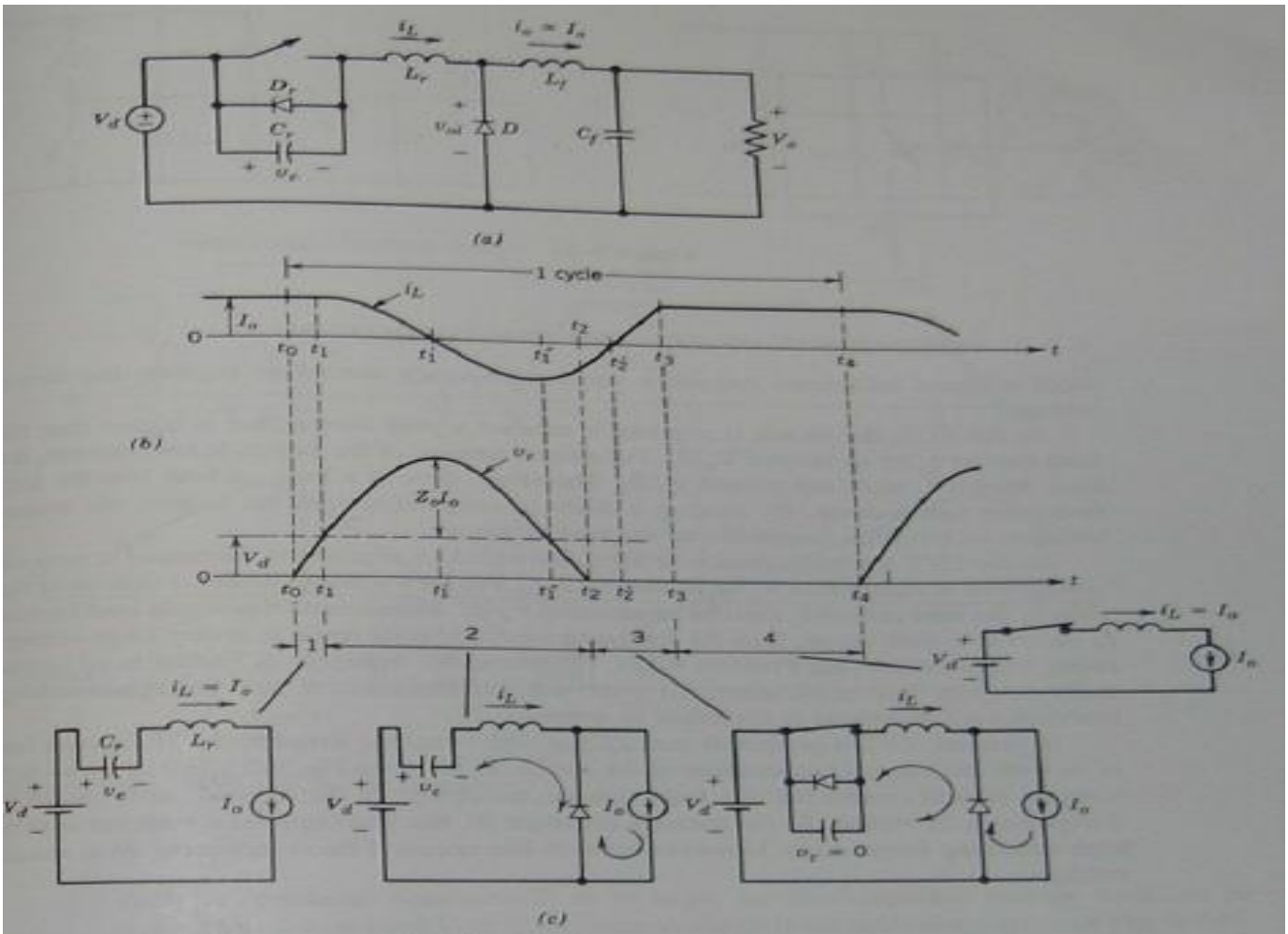


Figure 9-31 ZVS resonant-switch dc–dc converter.

b) Explain about Multi resonant converter with neat circuit diagram?

Ans:

This topology consists of a series-resonant circuit as shown in Fig. 9-22 but the load is connected in parallel with only part of the capacitance, for example, one-third of the total capacitance, and the other two-thirds of the capacitance appears in series. The purpose of this topology is to benefit from the advantageous properties of both the SLR and the PLR converters, namely that an SLR converter offers an inherent current limiting under short-circuit conditions and a PLR converter acts as a voltage source, and thus regulating its voltage at no load with a high-Q resonant tank is not a problem. These converters can be analyzed based on the discussion presented in the previous two sections. These are

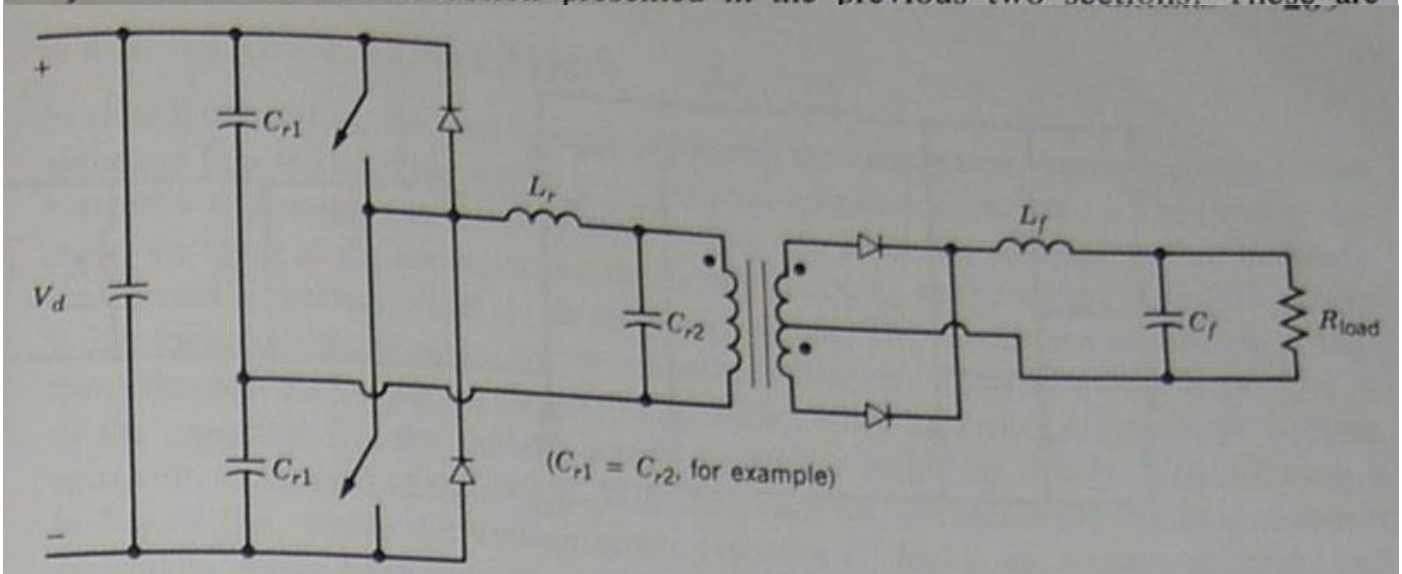


Figure 9-22 Hybrid-resonant dc–dc converter.

7 a) Explain about zero-current switching converters with wave forms?

Ans:

losses.

Zero-current switching can also be obtained by connecting C_r in parallel with D as shown in Fig. 9-30*a*. As discussed previously, i_o can be assumed to be a current of constant magnitude I_o in Fig. 9-30*a* during a high-frequency resonant cycle.

Initially both the capacitor voltage (across C_r) and the inductor current (through L_r) are assumed to be zero and the load current I_o freewheels through the diode D. The converter operation can be divided into the following intervals for which the converter waveforms as well as the corresponding circuit states are shown in Fig. 9-30*b* and 9-30*c*:

1. *Time interval* 1 *(between* t_0 *and* t_1*).* At time t_0, the switch is turned on. Because of I_o flowing through the diode it appears as a short circuit and the entire input voltage V_d appears across L_r. Therefore, the switch current builds up linearly until it becomes equal to I_o at time t_1. Beyond this time, the diode turns off and the voltage clamp across C_r is removed.
2. *Time interval* 2 *(between* t_1 *and* t_2*).* Beyond t_1, $i_T > I_o$ and their difference $(i_T - I_o)$ flows through C_r. At t_1', i_T peaks and $v_c = V_d$. At time t_1'', the switch current drops from its peak value to I_o and the capacitor voltage reaches $2V_d$. The switch current eventually drops to zero at t_2 and cannot reverse through the switch (if a BJT or a MOSFET is used as a switch, then a diode in series with it must be used to block a negative voltage and to prevent the flow of reverse current through the switch). Thus, the switch current is commutated off naturally and the gate/base drive from the switch should be removed at this point.
3. *Time interval (between* t_2 *and* t_3*).* Beyond the time t_2 with the switch off, the capacitor C_r discharges into the output load and the capacitor voltage linearly drops to zero at t_3.
4. *Time interval* 4 *(between* t_3 *and* t_4*).* Beyond t_3, the load current just freewheels through the diode until a time t_4, when the switch is turned on and the next switching cycle begins. This time interval is controlled to adjust the output voltage.

Under a steady-state operating condition, the average voltage across the filter inductor is zero; therefore the voltage across C_r averaged over one switching cycle equals the output voltage V_o. By controlling the freewheeling time interval 4 (i.e., by controlling the switching frequency), the output voltage V_o can be regulated.

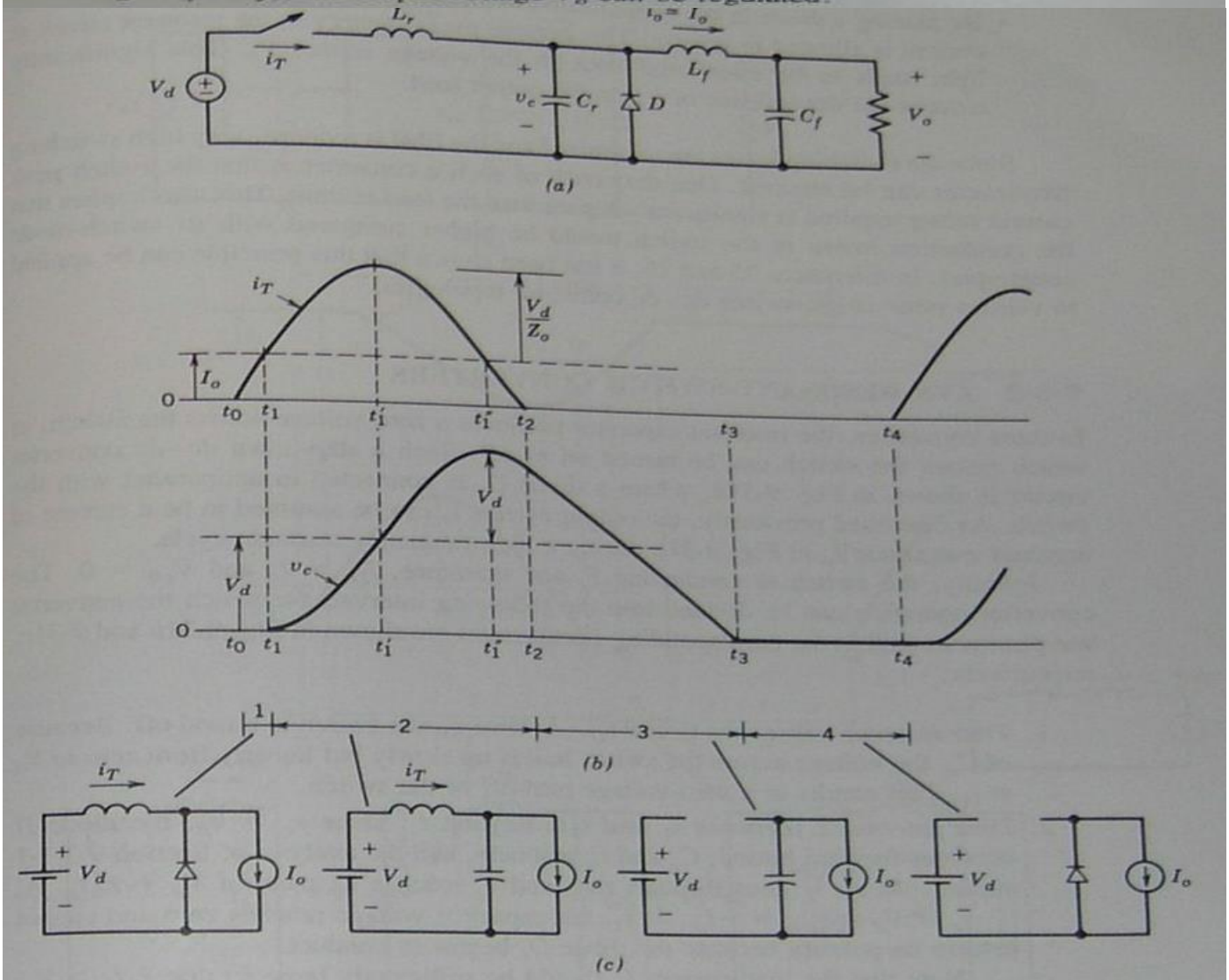


Figure 9-30 ZCS resonant-switch dc–dc converter; alternate configuration.

b) Explain load resonant converters with neat circuit diagram and wave forms?
Ans:

A half-bridge configuration of the SLR converter is shown in Fig. 9-10*a*. The waveforms and the operating principles are the same for the full-bridge configurations. A transformer can be included to provide the output voltage of a desired magnitude as well as the electrical isolation between the input and the output.

The series-resonant tank is formed by L_r and C_r, and the current through the resonant tank circuit is full-wave rectified at the output, and $|i_L|$ feeds the output stage. Therefore, as the name suggests, the output load appears in series with the resonant tank.

The filter capacitor C_f at the output is usually very large, and therefore the output voltage across the capacitor can be assumed to be a dc voltage without any ripple. The

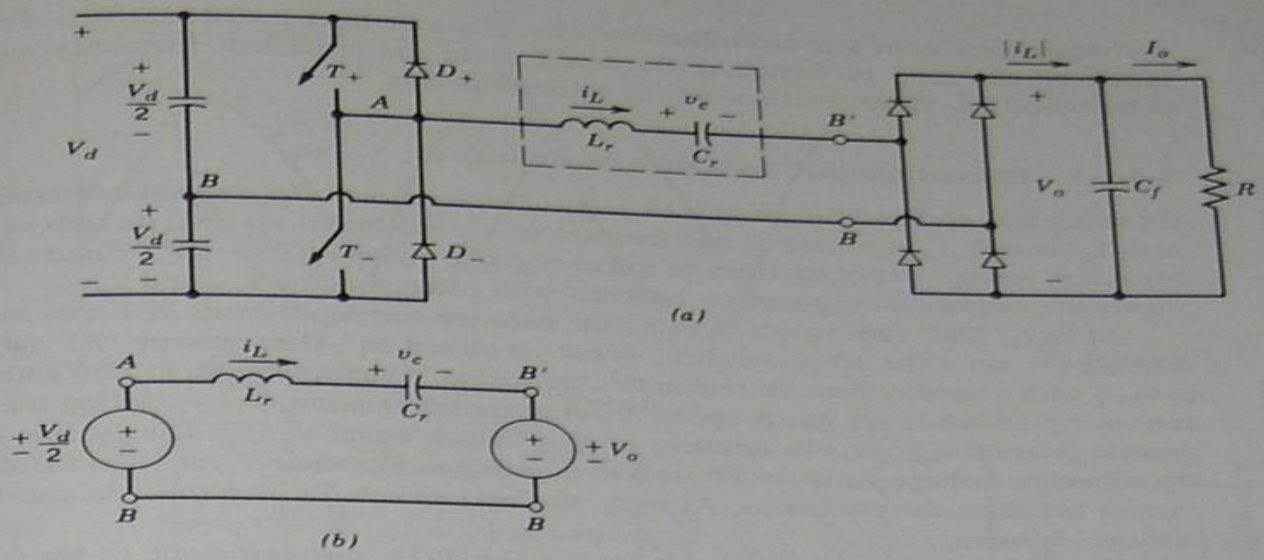


Figure 9-10 SLR dc–dc converter: (*a*) half-bridge; (*b*) equivalent circuit.

resistive power loss in the resonant circuit is assumed to be negligible, which greatly simplifies the analysis. The output voltage V_o is reflected across the rectifier input as $v_{B'B}$, where $v_{B'B} = V_o$ if i_L is positive and $v_{B'B} = -V_o$ if i_L is negative.

When i_L is positive, it flows through T_+ if it is on; otherwise it flows through the diode D_-. Similarly, when i_L is negative, it flows through T_- if it is on; otherwise it flows through the diode D_+. Therefore, in the circuit of Fig. 9-10*a*,

For $i_L > 0$

T_+ conducting: $v_{AB} = +\frac{1}{2}V_d$ $v_{AB'} = +\frac{1}{2}V_d - V_o$ (9-25)

D_- conducting: $v_{AB} = -\frac{1}{2}V_d$ $v_{AB'} = -\frac{1}{2}V_d - V_o$ (9-26)

For $i_L < 0$

T_- conducting: $v_{AB} = -\frac{1}{2}V_d$ $v_{AB'} = -\frac{1}{2}V_d + V_o$ (9-27)

D_+ conducting: $v_{AB} = +\frac{1}{2}V_d$ $v_{AB'} = +\frac{1}{2}V_d + V_o$ (9-28)

The foregoing equations show that the voltage applied across the tank ($v_{AB'}$) depends on which device is conducting and on the direction of i_L. The conditions described by Eqs. 7-25 through 9-28 can be represented by an equivalent circuit of Fig. 9-10*b*. The solution for the circuit of Fig. 9-5*a* is applied to the equivalent circuit of Fig. 9-10*b* for each interval, based on the initial conditions and the voltages V_{AB} and $V_{B'B}$, which appear as dc voltages for a given interval.

In the steady-state symmetrical operation, both the switches are operated identically. Similarly, the two diodes operate identically. Therefore, it is sufficient to analyze only one half-cycle of operation, since the other half is symmetrical. It can be shown that in the SLR converter of Fig. 9-10*a*, the output voltage V_o cannot exceed the input voltage $\frac{1}{2}V_d$, that is, $V_o \leq \frac{1}{2}V_d$.

The switching frequency f_s ($=\omega_s/2\pi$), with which the circuit waveforms repeat, can be controlled to be less than or greater than the resonance frequency f_0 ($=\omega_0/2\pi$) if the converter consists of self-controlled switches. There are three possible modes of operation based on the ratio of switching frequency ω_s to the resonance frequency ω_0, which determines if i_L flows continuously or discontinuously.

8 a) Find List the properties of Ideal rectifier?
Ans:

It is desired that the ideal single-phase rectifier present a resistive load to the ac system. The ac line current and voltage will then have the same waveshape and will be in phase. Unity power factor rectification is the result. Thus, the rectifier input current $i_{ac}(t)$ should be proportional to the applied input voltage $v_{ac}(t)$:

$$i_{ac}(t) = \frac{v_{ac}(t)}{R_e} \tag{18.1}$$

where R_e is the constant of proportionality. An equivalent circuit for the ac port of an ideal rectifier is therefore an effective resistance R_e, as shown in Fig. 18.1(a). R_e is also known as the *emulated resistance*. It should be noted that the presence of R_e does not imply the generation of heat: the power apparently

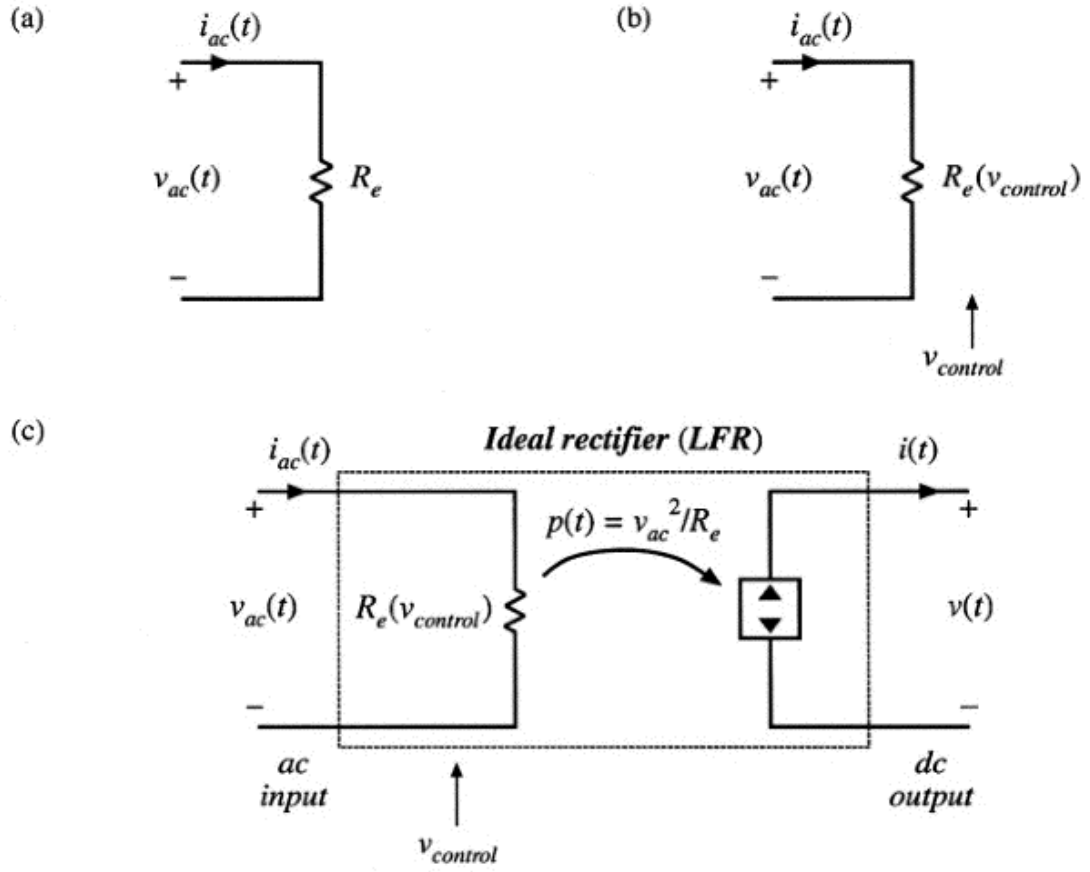


Fig. 18.1 Development of the ideal rectifier equivalent circuit model: (a) input port resistor emulation; (b) the value of the emulated resistance, and hence the power throughput, is controllable; (c) output port power source characteristic, and complete model.

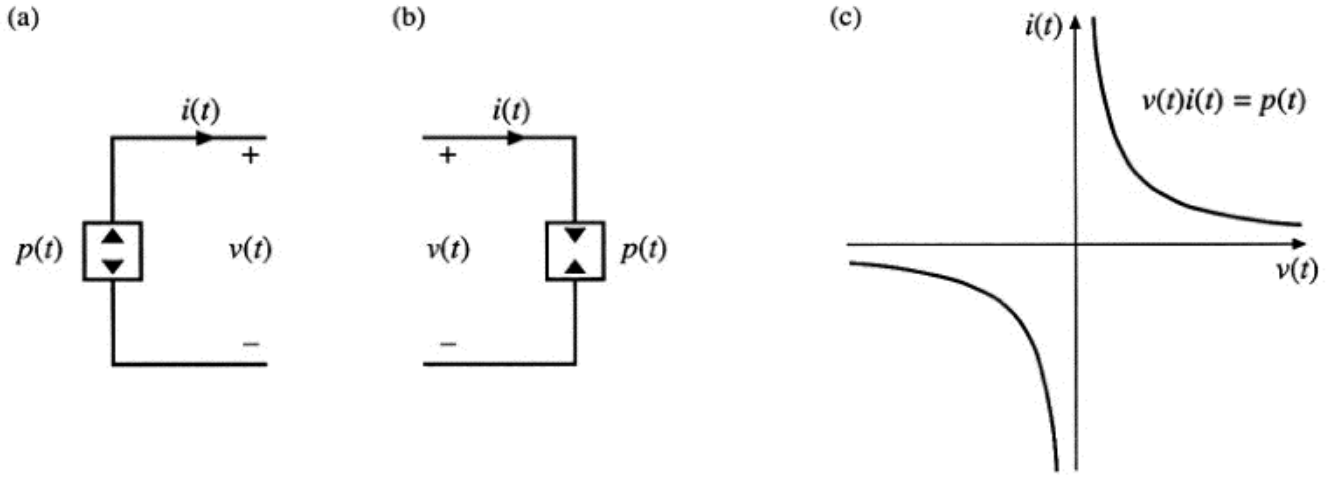


Fig. 18.2 The dependent power source: (a) power source schematic symbol, (b) power sink schematic symbol, (c) i–v characteristic.

"consumed" by R_e is actually transferred to the rectifier dc output port. R_e simply models how the ideal rectifier loads the ac power system.

Output regulation is accomplished by variation of the effective resistance R_e, and hence the value of R_e must depend on a control signal $v_{control}(t)$ as in Fig. 18. l(b). This allows variation of the rectifier power throughput, since the average power consumed by R_e is

$$P_{av} = \frac{V_{ac,rms}^2}{R_e(v_{control})} \tag{18.2}$$

Note that changing R_e results in a time-varying system, with generation of harmonics. To avoid generation of significant amounts of harmonics and degradation of the power factor, variations in R_e and in the control input must be slow with respect to the ac line frequency.

To the extent that the rectifier is lossless and contains negligible internal energy storage, the instantaneous power flowing into R_e must appear at the rectifier output port. Note that the instantaneous power throughput

$$p(t) = \frac{v_{ac}^2(t)}{R_e\left(v_{control}(t)\right)} \tag{18.3}$$

is dependent only on $v_{ac}(t)$ and the control input $v_{control}(t)$, and is independent of the characteristics of the load connected to the output port. Hence, the output port must behave as a source of constant power, obeying the relationship

$$v(t)i(t) = p(t) = \frac{v_{ac}^2(t)}{R_e} \tag{18.4}$$

The *dependent power source* symbol of Fig. 18.2(a) is used to denote such an output characteristic. As illustrated in Fig. 18.1(c), the output port is modeled by a power source that is dependent on the instantaneous power flowing into R_e.

Thus, a two-port model for the ideal unity-power-factor single-phase rectifier is as shown in Fig. 18.1(c) [2–4]. The two port model is also called a *loss-free resistor* (LFR) because (1) its input port obeys Ohm's law, and (2) power entering the input port is transferred directly to the output port without loss of

energy. The defining equations of the LFR are:

$$i_{ac}(t) = \frac{v_{ac}(t)}{R_e\left(v_{control}\right)} \tag{18.5}$$

$$v(t)\,i(t) = p(t) \tag{18.6}$$

$$p(t) = \frac{v_{ac}^2(t)}{R_e\left(v_{control}(t)\right)} \tag{18.7}$$

When the LFR output port is connected to a resistive load of value R, the dc output rms voltages and currents V_{rms} and I_{rms} are related to the ac input rms voltages and currents $V_{ac,rms}$ and $I_{ac,rms}$ as follows:

$$\frac{V_{rms}}{V_{ac,rms}} = \sqrt{\frac{R}{R_e}} \tag{18.8}$$

$$\frac{I_{ac,rms}}{I_{rms}} = \sqrt{\frac{R}{R_e}} \tag{18.9}$$

The properties of the power source and loss-free resistor network are discussed in Chapter 11. Regardless of the specific converter implementation, any single-phase rectifier having near-ideal properties can be modeled using the LFR two-port model.

b) Find Explain about three phase converter systems in PWM rectifiers?
Ans:

The single-phase ideal rectifier concepts of the previous sections can be generalized to cover ideal three-phase rectifiers. Figure 18.38(a) illustrates the properties of an ideal three-phase rectifier, which presents a balanced resistive load to the utility system. A three-phase converter system is controlled such that resistor emulation is obtained in each input phase. The rectifier three-phase input port can then be modeled by per-phase effective resistances R_e, as illustrated in Fig. 18.38(a). The instantaneous powers apparently consumed by these resistors are transferred to the rectifier dc output port. The rectifier output port can therefore be modeled by power sources equal to the instantaneous powers flowing into the effective resistances R_e. It is irrelevant whether the three power sources are connected in series or in parallel; in either event, they can be combined into a single source equal to the total three-phase instantaneous input power as illustrated in Fig. 18.38(b).

If the three-phase ac input voltages are

$$\begin{aligned} v_{an}(t) &= V_M \sin\left(\omega t\right) \\ v_{bn}(t) &= V_M \sin\left(\omega t - 120°\right) \\ v_{cn}(t) &= V_M \sin\left(\omega t - 240°\right) \end{aligned} \tag{18.150}$$

then the instantaneous powers flowing into the phase a, b, and c effective resistances R_e are

$$
\begin{aligned}
p_a(t) &= \frac{v_{an}^2(t)}{R_e} = \frac{V_M^2}{2R_e}\left(1 - \cos\left(2\omega t\right)\right) \\
p_b(t) &= \frac{v_{bn}^2(t)}{R_e} = \frac{V_M^2}{2R_e}\left(1 - \cos\left(2\omega t - 240^\circ\right)\right) \\
p_c(t) &= \frac{v_{cn}^2(t)}{R_e} = \frac{V_M^2}{2R_e}\left(1 - \cos\left(2\omega t - 120^\circ\right)\right)
\end{aligned}
\tag{18.151}
$$

Each instantaneous phase power contains a dc term $V_M^2/(2R_e)$, and a second-harmonic term. The total instantaneous three-phase power is

$$
p_{tot}(t) = p_a(t) + p_b(t) + p_c(t) = \frac{3}{2}\frac{V_M^2}{R_e} \tag{18.152}
$$

This is the instantaneous power which flows out of the rectifier dc output port. Note that the second harmonic terms add to zero, such that the rectifier instantaneous output power is constant. This is a consequence of the fact that the instantaneous power flow in any balanced three-phase ac system is constant. So, unlike the single-phase case, the ideal three-phase rectifier can supply constant instantaneous power to a dc load, without the need for internal low-frequency energy storage.

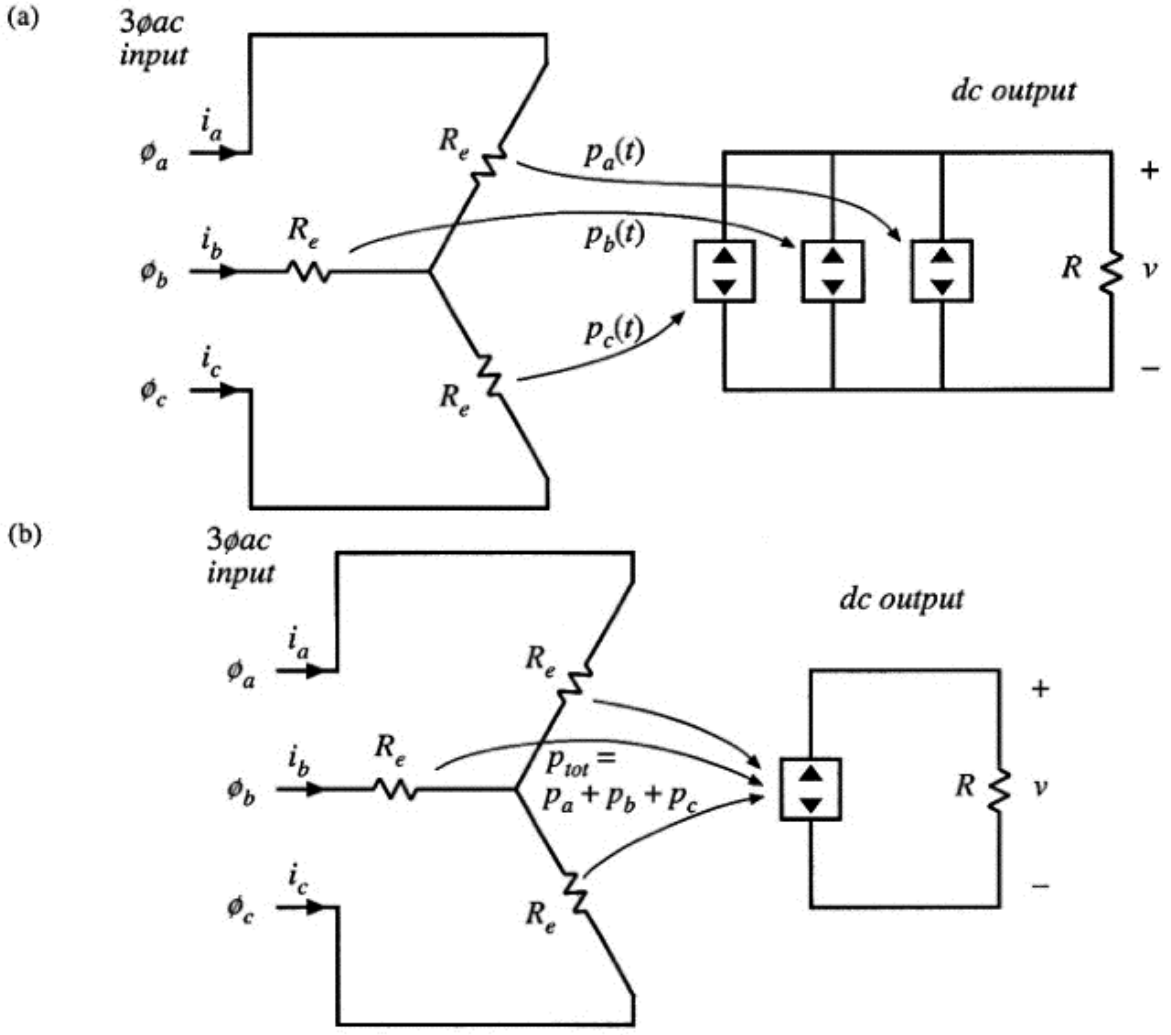


Fig. 18.38 Development of the ideal three-phase rectifier model: (a) three ideal single-phase rectifiers, (b) combination of the three power sources into an equivalent single power source.

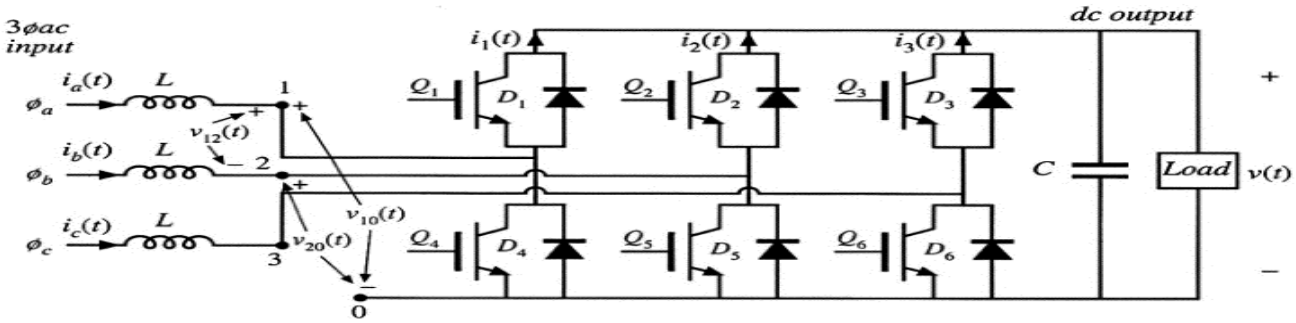


Fig. 18.39 Boost-type 3øac–dc PWM rectifier.

A variety of 3øac–dc PWM rectifiers are known; a few of the many references on this subject are listed in the references [42–59]. The most well-known topology is the three-phase ac–dc boost rectifier, illustrated in Fig. 18.39. This converter requires six SPST current-bidirectional two-quadrant switches. The inductors and capacitor filter the high-frequency switching harmonics, and have little influence on the low-frequency ac components of the waveforms. The switches of each phase are controlled to obtain input resistor emulation, either with a multiplying controller scheme similar to Fig. 18.5, or with some other approach. To obtain undistorted line current waveforms, the dc output voltage V must be greater than or equal to the peak line-to-line ac input voltage $V_{L\text{-}pk}$. In a typical realization, V is somewhat greater than $V_{L\text{-}pk}$. This converter resembles the voltage-source inverter, discussed briefly in Chapter 4, except that the converter is operated as a rectifier, and the converter input currents are controlled via high-frequency pulse-width modulation.

The three-phase boost rectifier of Fig. 18.39 has several attributes that make it the leading candidate for most 3øac–dc rectifier applications. The ac input currents are nonpulsating, and hence very little additional input EMI filtering is required. As in the case of the single-phase boost rectifier, the rms transistor currents and also the conduction losses of the three-phase boost rectifier are low relative to other 3øac–dc topologies such as the current-source inverter. The converter is capable of bidirectional power flow. A disadvantage is the requirement for six active devices: when compared with a dc–dc converter of similar ratings, the active semiconductor utilization (discussed in Chapter 6) is low. Also, since the rectifier has a boost characteristic, it is not suitable for direct replacement of traditional buck-type phase-controlled rectifiers.

9 a) Explain about single phase converter systems in pulse width modulated rectifiers?
Ans:

It is usually desired that the dc output voltage of a converter system be regulated with high accuracy. In practice, this is easily accomplished using a high-gain wide-bandwidth feedback loop. A well-regulated dc output voltage $v(t) = V$ is then obtained, which has negligible ac variations. For a given constant load characteristic, the load current I and the instantaneous load power $p_{load}(t) = P_{load}$, are also constant:

$$p_{load}(t) = v(t)i(t) = VI \tag{18.82}$$

However, the instantaneous input power $p_{ac}(t)$ of a single-phase ideal rectifier is not constant:

$$p_{ac}(t) = v_g(t)i_g(t) \tag{18.83}$$

If $v_g(t)$ is given by Eq. (18.11), and if $i_g(t)$ follows Eq. (18.1), then the instantaneous input power becomes

$$p_{ac}(t) = \frac{V_M^2}{R_e}\sin^2(\omega t) = \frac{V_M^2}{2R_e}\left(1 - \cos(2\omega t)\right) \tag{18.84}$$

which varies with time. The instantaneous input power is zero at the zero crossings of the ac input voltage. Equations (18.82) and (18.84) are illustrated in Fig. 18.24(a). Note that the desired instantaneous load power $p_{load}(t)$ is not equal to the desired instantaneous rectifier input power $p_{ac}(t)$. Some element within the rectifier system must supply or consume the difference between these two instantaneous powers.

Since the ideal rectifier does not consume or generate power, nor does it contain significant internal energy storage, it is necessary to add to the system a low-frequency energy storage element such

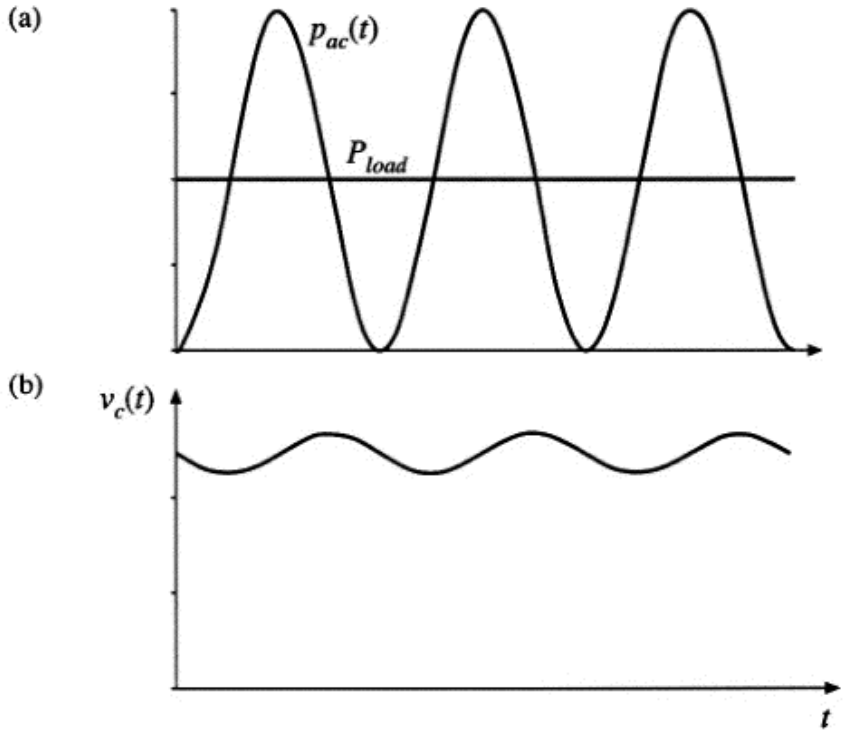


Fig. 18.24 Waveforms of a single-phase ideal rectifier system: (a) pulsating ac input power $p_{ac}(t)$, and constant dc load power P_{load}; (b) energy storage capacitor voltage $v_C(t)$.

as an electrolytic capacitor. The difference between the instantaneous input and load powers flows through this capacitor.

The waveforms of rectifier systems containing reactive elements can be determined by solution of the rectifier energy equation [36,37]. If the energy storage capacitor C is the only system element capable of significant low-frequency energy storage, then the power $p_C(t)$ flowing into the capacitor is equal to the difference between the instantaneous input and output powers:

$$p_C(t) = \frac{dE_C(t)}{dt} = \frac{d\left(\frac{1}{2}Cv_C^2(t)\right)}{dt} = p_{ac}(t) - p_{load}(t) \tag{18.85}$$

where C is the capacitance, $v_C(t)$ is the capacitor voltage, and $E_C(t)$ is the energy stored in the capacitor. Hence as illustrated in Fig. 18.24(b), when $p_{ac}(t) > p_{load}(t)$ then energy flows into the capacitor, and $v_C(t)$ increases. Likewise, $v_C(t)$ decreases when $p_{ac}(t) < p_{load}(t)$. So the capacitor voltage $v_C(t)$ must be allowed to increase and decrease as necessary to store and release the required energy. In steady-state, the average values of $p_{ac}(t)$ and $p_{load}(t)$ must be equal, so that over one ac line cycle there is no net change in capacitor stored energy.

Where can the energy storage capacitor be placed? It is necessary to separate the energy storage capacitor from the regulated dc output, so that the capacitor voltage is allowed to independently vary as illustrated in Fig. 18.24(b). A conventional means of accomplishing this is illustrated in Fig. 18.25. A second dc–dc converter is inserted, between the energy storage capacitor and the regulated dc load. A wide-bandwidth feedback loop controls this converter, to attain a well-regulated dc load voltage. The capacitor voltage $v_C(t)$ is allowed to vary. Thus, this system configuration is capable of (1) wide-bandwidth control of the ac line current waveform, to attain unity power factor, (2) internal low-frequency energy storage, and (3) wide-bandwidth regulation of the dc output voltage. It is also possible to integrate these functions into a single converter, provided that the required low-frequency independence of the input, output, and capacitor voltages is maintained [38].

The energy storage capacitor also allows the system to function in other situations in which the instantaneous input and output powers differ. For example, it is commonly required that the output volt-

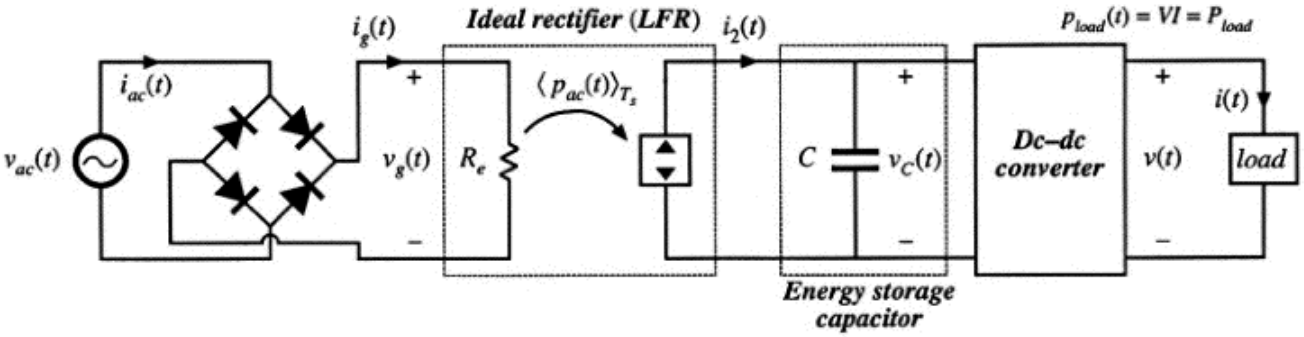


Fig. 18.25 Elements of a single-phase-ac to dc power supply, in which the ac line current and dc load voltage are independently regulated with high bandwidth. An internal independent energy storage capacitor is required.

age remain regulated during ac line voltage failures of short duration. The *hold-up time* is the duration that the output voltage $v(t)$ remains regulated after $v_{ac}(t)$ has become zero. A typical requirement is that the system continue to supply power to the load during one complete missing ac line cycle, that is, for 20 msec in a 50 Hz system. During the hold-up time, the load power is supplied entirely by the energy storage capacitor. The value of capacitance should be chosen such that at the end of the hold-up time, the capacitor voltage $v_C(t)$ exceeds the minimum value that the dc–dc converter requires to produce the desired load voltage.

b) Explain the concepts of bifurcation and chaos?

Ans:

The term bifurcation was coined by Poincaré to designate the emergence of several solutions from a given solution. Whenever the solution to an equation, or system of equations, changes qualitatively at a fixed value of a parameter, called a critical value, the phenomenon is called a bifurcation. The dynamic system and chaos can be related as follows: when a dynamical system, described by a set of parameterized differential equations, changes qualitatively, as a function of an external parameter, the nature of its long-time limiting behaviour in terms of fix points or limit cycles, one speaks of a bifurcation. the appearance of chaos in a system is usually associated with systems whose mathematical model has a parameter that can vary. For a given range of values of this parameter, the system will exhibit a chaotic behaviour. The point that marks this change is called a bifurcation point.

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