18ECI02

Hall Ticket Number:

IV/IV B.Tech (Regular/Supplementary) DEGREE EXAMINATION

November,2022 **Institutional Elective (Common to all branches)**

Seventh Semester **Embedded Systems**

Time: Three Hours **Maximum: 5**0 Marks

Answer Question No. 1 Compulsorily. (10X1 = 10 Marks)

*Answer **ANY ONE** question from each Unit.* (4X10=40 Marks)

1.	a)	Cite about tradeoff.	CO1(BL1)	
	b)	Recall about pipe lining	CO1(BL1)	
	c)	State the purpose of RS485.	CO2(BL2)	
	d)	Present why embedded systems are realized as real time systems.	CO2(BL2)	
	e)	Mention significant improvements of PSMM	CO2(BL2)	
	f)	Mention about pipes.	CO3(BL1)	
	g)	Identify the significance of task.	CO3(BL1)	
	h)	Interpret about interrupt latency.	CO3(BL2)	
	i)	Specify the function of circuit emulator.	CO4(BL2)	
	j)	What is a cross compiler?	CO4(BL1)	
		Unit - I		
2.	a)	Differentiate between Single purpose and general purpose processors	CO1(BL3)	**5M**
	b)	Describe different components of Embedded system with necessary diagram	CO1(BL2)	**5M**
		(OR)		
3.	a)	Explain the design metrics of an embedded system with some specific example	CO1(BL4)	**5M**
	b)	Discriminate between Harvard and Von-Neumann Architecture	CO1(BL3)	**5M**
		Unit - II		
4.	a)	Elaborate about concurrent process model	CO2(BL2)	**5M**
	b)	Describe the need for communication interfaces.	CO2(BL3)	**5M**
		(OR)		
5.	a)	Demonstrate about Data flow model	CO2(BL2)	**5M**
	b)	Illustrate the working of IEEE802.11 communication	CO2(BL3)	**5M**
		Unit - III		
6.	a)	Explain about Interrupt service routines in an RTOS environment.	CO3(BL3)	**5M**
	b)	Describe about mail boxes and message queues.	CO3(BL2)	**5M**
		(OR)		
7.	a)	Describe about semaphores	CO3(BL4)	**5M**
	b)	Explain Task &Task scheduler	CO3(BL3)	**5M**
		Unit - IV		
8.	a)	Differentiate between RTOS and embedded OS	CO4(BL3)	**5M**
	b)	Elucidate about logic synthesis.	CO4(BL2)	**5M**
		(OR)		
9.	a)	Discriminate between Handheld OS and RT Linux	CO4(BL4)	**5M**
	b)	Present about priority inversion problem and specify when it occurs.	CO4(BL3)	**5M**

Scheme-18ECI02-Embedded Systems(Nov-2022)

10*1=10M

1a) A trade-off is a situational decision that involves diminishing or losing one quality, quantity, or property of a set or design in return for gains in other aspects. In simple terms, a tradeoff is where one thing increases, and another must decrease.

1b) Pipelining is acommon way to increase the instruction throughput of a microprocessor

1c) *RS485* is a standard defining the electrical characteristics of serial lines for use in serial communications systems.

1d) Real-time embedded systems are those that incorporate a real-time operating system, ensuring that the device can respond to sensory inputs within the time constraints specified by the embedded software

1e) The program-state machine(PSM)model extends state machines to allow use of sequential program code to define a state's actions,including extensions for complex data types and variables

1f) A Pipe is a device used for the inter process communication.

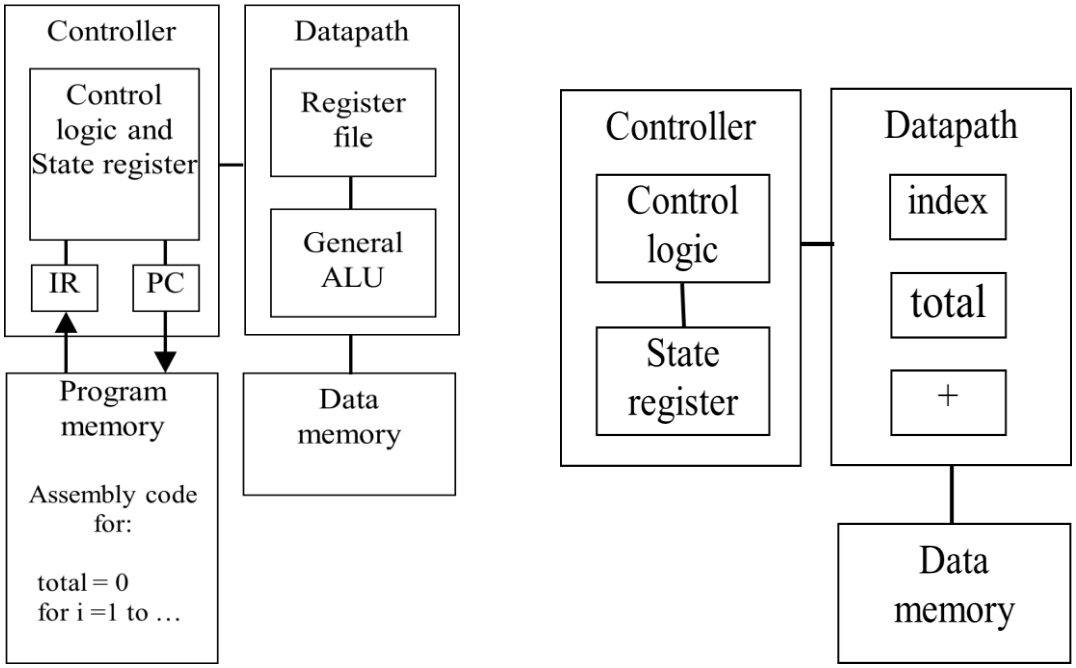
1g) A *Task is the smallest schedulable unit managed by the OS*

1h) Interrupt latency :Maximum time for which interrupts are disabled plus time to start the execution of the first instruction in the ISR is called interrupt latency.

1i) An in-circuit emulator (ICE) provides a window into the embedded system. The programmer uses the emulator to load programs into the embedded system, run them, step through them slowly, and view and change data used by the system's software.

1j) A cross compiler creates code for a different processor architecture than the one you're working with.

2a) General Purpose Processor (3M) & Single purpose Processor (2M)



i)The designer of general pupose processor builds a programmable device that is suitable for a variety of applications to maximize the number of devices sold.

- Features: Program memory, General Datapath, General ALU
- Benefits: Low time to market, low NRE cost, high flexibility

ii)Single purpose processor is a digital circuit designed to execute exactly one program

- Features
  - Datapath contains only the essential components needed to execute a single program
  - No program memory
- Benefits
  - Fast , Low power, Small size

2b) Components of Embedded system **5M**

An embedded system has three main components: Hardware, Software and Real time Operating System. Hardware consists of processors, system application specific circuits, timers, and memory. Softwares must do a specific tasks in a series, so it has a software that keeps in view three constrains which are : availability of system memory, availability of processor speed, and the need to limit the power dissipation. Moving on to the last component, Real time operating system, it organizes the system and provides a technique that lets the processor run as per scheduling and then switches from one processor to the other.For the embedded system the power supply is the key component to provide the power to the embedded system circuit. Usually, the embedded system requires 5 V supply or can be range from 1.8 to 3.3. V.

3a) Design metrics:(any 5) **5M**

- Unit cost: the monetary cost of manufacturing each copy of the system, excluding NRE cost
- NRE cost (Non-Recurring Engineering cost): The one-time monetary cost of designing the system
- Size: the physical space required by the system
- Performance: the execution time or throughput of the system
- Power: the amount of power consumed by the system
- Flexibility: the ability to change the functionality of the system without incurring heavy NRE cost
- Time-to-prototype: the time needed to build a working version of the system
- Time-to-market: the time required to develop a system to the point that it can be released and sold to customers
- Maintainability: the ability to modify the system after its initial release
- Correctness, safety.

3b)Harvard vs Von Neumann architecture **5M**

Harvard architecture	Von-Neumann architecture
⊡ It has separate buses for instruction as well as data fetching.	⊡ It shares single common bus for instruction and data fetching.
⊡ Easier to pipeline, so high performance can be achieve.	⊡ Low performance as compared to Harvard architecture.
⊡ Comparatively high cost.	⊡ It is cheaper.
⊡ Since data memory and program memory are stored physically in different locations, no chances exist for accidental corruption of program memory.	⊡ Accidental corruption of program memory may occur if data memory and program memory are stored physically in the same chip,

4a) Concurrent process model: **5M**

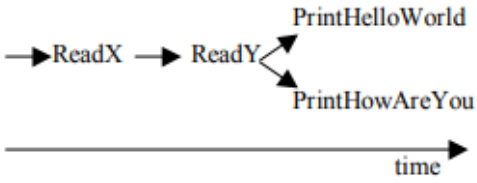
It allows to describe the functionality of a system in terms of two or more concurrently executing sub tasks.

```
ConcurrentProcessExample()
  x = ReadX()
  y = ReadY()
  Call concurrently:
    PrintHelloWorld(x) and
    PrintHowAreYou(y)

PrintHelloWorld(x)
  while (1) {
    print "Hello world."
    delay(x);
  }

PrintHowAreYou(x)
  while (1) {
    print "How are you?"
    delay(y);
  }
```

(a)



(b)

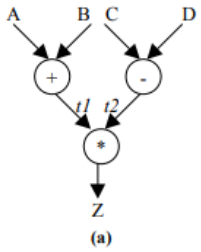
```
Enter X: 1
Enter Y: 2
Hello world.      (Time = 1 s)
Hello world.      (Time = 2 s)
How are you?      (Time = 2 s)
Hello world.      (Time = 3 s)
How are you?      (Time = 4 s)
Hello world.      (Time = 4 s)
...
```

(c)

4b)Need for communication interfaces: **5M**

- An embedded system can be accessed over internet.
- The software can be upgraded
- To exchange data
- For monitoring by a host system.
- To interface with the external world.

5a)Data flow model: **5M**



(a)

In a dataflow model, we describe system behavior as a set of nodes representing transformations, and a set of directed edges representing the flow of data from one node to another. Each node consumes data from its input edges, performs its transformation, and produces data on its output edge. All nodes may execute concurrently

5b) IEEE802.11: **5M**

- Proposed standard for wireless LANs
- Specifies parameters for PHY and MAC layers of network
  - PHY layer
    - physical layer
    - handles transmission of data between nodes
    - provisions for data transfer rates of 1 or 2 Mbps
    - operates in 2.4 to 2.4835 GHz frequency band (RF)
    - or 300 to 428,000 GHz (IR)
  - MAC layer
    - medium access control layer
    - protocol responsible for maintaining order in shared medium
    - collision avoidance/detection

6a) ISR: 5M

Interrupt is a hardware signal that informs the CPU that an important event has occured.

- Interrupt latency:

Maximum time for which interrupts are disabled plus time to start the execution of the first instruction in the isr is called interrupt latency.

- Interrupt response time:

Time between receipt of interrupt signal and starting the code that handles the interrupt is called Interrupt response time.

- Interrupt recovery time:

time required for cpu to return to interrupt code /highest priority task is called interrupt recovery time

6b)Mailboxes 2M

The operation of a mailbox object is similar to our postal mailbox. When someone posts a message in our mailbox, we take out the message.

Function calls: Create a mailbox,Delete a mailbox, Query a mailbox, Post a message in a mailbox, Read a message form a mailbox.

Message queues: Definition-1M

Message queues can be considered as an array of mailboxes. At the time of creating a queue, the queue is given a name or ID, queue length, sending task waiting list and receiving task waiting list

Function calls:- create a queue, delete a queue, flush a queue, post a message in queue, read a message from queue, show queue information, show queue waiting list **1M**

Applications: One way communication, Two way communication, Broadcasting **1M**

7a) Definition: A semaphore is a kernel object that is used for both resource synchronization, task synchronization 1M

Explanation of binary semaphore and counting semaphore 3M

Semaphores Function calls: 1M

Create a semaphore, Delete a semaphore, Acquire a semaphore, release a semaphore, Query a semaphore

7b)**Task and Task Scheduler**

Task states:- **2M**

1.Running state 2.ready to run state 3.waiting state 4.ISR

Scheduling Algorithms:- (any 3) **3M**

1.First in First out 2.Round robin 3.Round robin with priority 4.shortest job first

5.Non-preemptive Multitasking 6.Preemptive Multitasking

8a) RTOS: **2M**

A real-time operating system (RTOS) is an operating system (OS) for real-time applications that processes data and events that have critically defined time constraints. RTOS have mechanisms to prevent priority inversion

- EX: QNX Neutrino, Vx Works, MicroC/OS-II,RT Linux

Embedded OS: **3M**

These operating systems are suitable for non-real time applications. They use a pre-emptive kernel, but strict deadline cannot be met. The stripped down versions of the desktop operating systems can be used as embedded operating systems i.e. in the operating system software, remove all the unnecessary features and the make the kernel occupy a small memory and you have the embedded operating system.

- EX: Embedded NT, Windows XP embedded, Embedded Linux

8b) logic synthesis: Converting logic-level behavior into structural implementation

1. Combinational logic synthesis - 3M
   - Two-level minimization
   - Multilevel minimization
2. FSM synthesis- 2M
   - State minimization
   - State encoding

9a) **Handheld OS:** **2M**

Handheld operating systems are present in all handheld devices like Smartphones and tablets. It is also called a Personal Digital Assistant. The popular handheld device in today's world is Android and iOS. These operating systems need a high-processing processor and are also embedded with various types of sensors.

EX:Palm OS, Symbian OS,Windows CE,Windows CE.NET

RT Linux: **3M**

- RT Linux is a hard real time RTOS microkernel that runs the entire Linux operating system as a fully preemptive process.
- It has support for many processors such as x86,pentium,power PC etc.
- This OS is an excellent choice for 32-bit processor based embedded systems.
- RT Linux -RT LinuxPro, RT Linux Free

9b) Priority Inversion Problem-Definition **2M**

In any real time embedded system, if a high priority task is blocked or waiting and a low priority task is running or under execution ,this situation is called Priority Inversion.

Explanation with example - 3M