Bapatla Engineering College
(Autonomous)
Affiliated to Acharya Nagarjuna University, Guntur, Andhra Pradesh.

A Two Day
Student Workshop
On

Micro Architecture Design: Deep Dive into RISC V

(10th & 11th July 2023)

Organized by

Department of

Electronics and Communication Engineering

For more details contact:

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ABOUT THE COLLEGE

Bapatla Engineering College (Autonomous) was established by Bapatla Education Society in the year 1981 and is reckoned for its academic excellence in engineering & sciences. It is a constituent institution of Acharya Nagarjuna University and is one of the best private engineering institutions in the southern region. BEC offers graduate courses in 8 disciplines with total intake of above 1000 students, 5 post-graduate courses in CSE, CAD/CAM (Mech), PE (EEE), SE (CIVIL) and CESP (ECE). The College is a little away from the din and bustle of Bapatla, a town with a historic and hoary past, about 75 Km. south of Vijayawada on Chennai-Vijayawada rail route. All departments have well equipped laboratories in addition to the common facilities of workshops, central library, state-of-art central computing facility, sports facilities and Innovation Centres that houses research and testing facilities for industrial projects and technology labs to promote inter-disciplinary research activities.

ABOUT THE DEPARTMENT

The Department of Electronics & Communication Engineering is established in 1981 and have experienced, well-qualified, committed, and motivated faculty with specializations in various streams. Currently ECE Department offers a 4 year Graduate Program (B.Tech) in Electronics & Communication Engineering (ECE) and Post-Graduate (M.Tech.) Program in Communication Engineering & Signal Processing (CESP), The Department was accredited thrice by NBA of AICTE and NAAC.

OBJECTIVES OF THE WORKSHOP

The main objective of this Two-day student workshop is to familiarize the participants with Microarchitecture Design of RISC V based devices using latest development tools and hardware programming language. The RISC V architecture is the latest standard employed in the design of microprocessors, microcontrollers and FPGAs. This workshop on microarchitecture design will be beneficial to the students, faculties and researchers working in the allied areas of VLSI design of Processors & Controller for processing and networking applications. Therefore, considering the importance of design and programming using latest tools, this student workshop is planned to enlighten up-to-date review of RISC V based processor/controller design.

The workshop mainly focuses:

- Introduction to Chip Design Technology
- RISC V features & Overview
- Micro architecture Design
- Verilog overview & RTL coding
- Skills required for the Job Market and Current Trends

Chief Patrons
Sri. Muppalaneni Srinivasa Rao, President, BES
Sri. Doppalapudi Rama Mohan Rao, Vice-President I, BES
Sri. Gelli Dileep Kumar, Vice-President II, BES
Sri. Manam Nageswara Rao, Secretary, BES
Sri. Kommineni Hari Padma Prasad, Joint Secretary, BES
Sri. Thalluri Ramakrishna Rao, Treasurer, BES

Patrons
Dr. Nazeer Shaik, Principal
Dr. B. Chandra Mohan, Professor & Dean-Academics
Dr. N. Venkateswara Rao, Professor & HOD

Conveners & Coordinators
Dr. P.Vinod Babu, Assoc. Prof.
Dr. Ch.V.M.S.N.Pavan Kumar, Asst.Prof.
Mr. M. Srikanth, Asst.Prof.

Resource Person

Sri. S. Sagar
Principal Engineer,
Custom CPU Architecture & Design Group
Qualcomm Technologies Inc., USA

Target Audience

Faculty Members
II & III B.Tech Students

Free Registration & e-Certificate will be issued to all participants.

Register using the following link:
https://forms.gle/yveqXbWWU5rwq6pg8