20EE402

Hall Ticket Number:

II/IV B.Tech (Regular\Supplementary) DEGREE EXAMINATION

July/August, 2022 — **Electrical and Electronics Engineering**

Fourth Semester — **Digital Electronics**

Time: Three Hours — **Maximum:** 70 Marks

Answer Question No.1 compulsorily. (1X14 = 14 Marks)

Answer ONE question from each unit. (4X14=56 Marks)

1	a)	Represent 248_{10} in BCD	CO1	L1	1
	b)	What is ODD parity.	CO1	L1	1
	c)	State distributive law.	CO1	L2	1
	d)	Obtain Truth Table for EX-OR gate.	CO2	L2	1
	e)	Write the truth table of Full Adder.	CO2	L2	1
	f)	What is comparator	CO2	L1	1
	g)	What is decoder	CO2	L1	1
	h)	What are the applications of Multiplexer	CO3	L2	1
	i)	Define race around condition.	CO3	L1	1
	j)	What is toggling.	CO3	L3	1
	k)	Draw the circuit of SR flip flop.	CO4	L3	1
	l)	What are the different types of shift registers?	CO6	L2	1
	m)	What are the different types of A/D converters?	CO5	L2	1
	n)	What is PLD?	CO6	L2	1
		Unit-I			
2	a)	Obtain the 1's complement and 2's complement of the binary numbers i. 1010111 ii. 0111001 iii. 1001 iv. 00010	CO1	L2	7M
	b)	Construct the hamming code for 7 bit data bits 1011011.	CO1	L4	7M
		(OR)			
3	a)	Briefly explain different logic circuits with Truth tables and logic symbols.	CO1	L2	7M
	b)	Briefly explain TTL logic family with neat sketches.	CO1	L2	7M
		Unit-II			
4	a)	Simplify the following using K-Map F=m(0,1,2,3,8,9,10,14,15)	CO2	L4	7M
	b)	Design 3 bit excess 3 code to gray code converter.	CO2	L2	7M
		(OR)			
5	a)	Design 4 bit serial adder/subtractor with control input M?	CO3	L3	7M
	b)	Design and explain 8*1 MUX.	CO3	L2	7M
		Unit-III			
6	a)	Convert the following flip-flops with excitation table a) SR to D flip - flop b) JK to D flip – flop	CO4	L4	14M
		(OR)			
7	a)	Design a 4 bit synchronous counter with D flip - flops and explain its working.	CO6	L4	7M
	b)	Design a bidirectional shift register.	CO6	L3	7M
		Unit-IV			
8	a)	Draw and explain about Sample and Hold circuit.	CO5	L2	7M
	b)	Discuss about successive approximation A/D converter.	CO5	L2	7M
		(OR)			
9		Implement the following function using PLA and PAL: a. $f1(A,B,C,D) = \sum(0, 1, 2, 3, 6, 9, 11)$ b. $f2(A,B,C,D) = \sum(0, 1, 6, 8, 9)$.	CO6	L4	14M

1.

a) 248_{10} in BCD 0010 0100 1000

b) If number of ones are odd number in data bits, then it is called odd parity.

c) $A + BC = (A+B)(A+C)$

d)

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

e)

A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

f) which compares magnitude of two bits is called comparator.

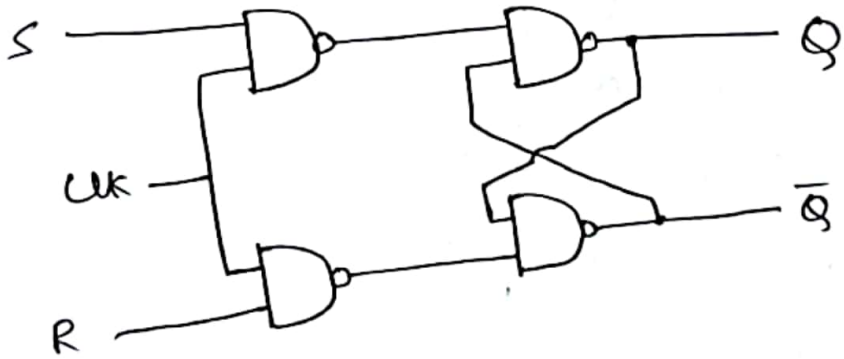
g) A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.

h) 1. data selector device
2. communication systems
3. Telephone Networks

i) When both inputs of JK flip flop are one, the output is uncertain. This condition of JK flip flop is called race around condition.

j) In T flip flop, when the both inputs are 1, the next output state is changed with the complement of the present state output. This process is known as "Toggling".

k)



l) 1) left shift register
2) Right shift register

m) 1. Successive approximation type
2. Dual slope ADC.

n) PLD in programmable logic devices are the integrated circuits. They contain an array of AND gates and another array of OR gates.

UNIT-1

2)

a) i) 1010111

1's complement – 0101000
2's Complement – 0101001
} 2M

ii) 0111001

1's complement – 1000110
2's Complement – 1000111
} 2M

iii) 1001

1's Compliment – 0110
2's Compliment – 0111
} 1M

iv) 00010

1's Compliment – 11101
2's Compliment – 11110
} 2M

b) Given data bits = 1011011

no. of parity bits $\Rightarrow 2^p \geq m+p+1$

Here $m = 7$ (data bits)

∴ for $p = 4$, above equation will satisfy.

∴ no. of parity bits = 4

no. of data bits = 7

∴ length of Hamming code = $m+p$
$= 7+4 = 11$.

2M

0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011
P_1	P_2	m_1	P_3	m_2	m_3	m_4	P_4	m_5	m_6	m_7
1	2	3	4	5	6	7	8	9	10	11
		1		0	1	1		0	1	1
–	–		–				–			

Here i'm considering even parity / odd parity.

$C_1 = P_1\, m_1\, m_2\, m_4\, m_5\, m_7$

$= \_\ 1\ 0\ 1\ 0\ 1$

for even parity, $P_1 = 1$

for odd parity, $P_1 = 0$

$C_2 = P_2\, m_1\, m_3\, m_4\, m_6\, m_7$

$= \_\ 1\ 1\ 1\ 1\ 1$

for even parity, $P_2 = 1$

for odd parity, $P_2 = 0$

2M

$C_3 = P_3 m_2 m_3 m_4$

$= \_ \; 0 \; 1 \; 1$

for even parity, $P_3 = 0$

for odd parity, $P_3 = 1$

$C_4 = P_4 m_5 m_6 m_7$

$= \_ \; 0 \; 1 \; 1$

for even parity, $P_4 = 0$

for odd parity, $P_4 = 1$

} 3M

∴ for even parity, the hamming code is,

1 1 1 0 0 1 1 0 0 1 1

for odd parity, the hamming code is,

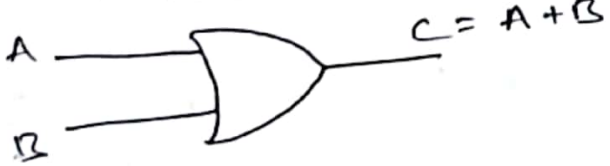
0 0 1 1 0 1 1 1 0 1 1

(OR)

3)

a) 1) OR logic : It performs addition operation. when any one of the input is high, then the output is high. If both the inputs are low, then the output is low.

logic diagram



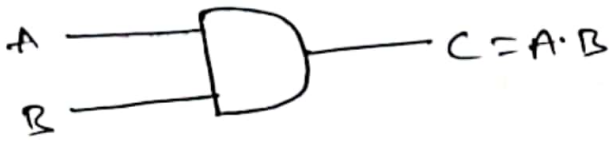
Truth table

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

} 1M

2) AND logic : It performs ~~addition~~ multiplication operation. when any one of the input is low, then the output is low.

Logic diagram



Truth Table } 1M

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

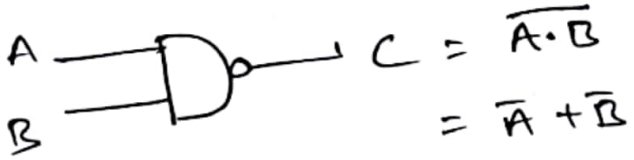
3) NOT logic : it performs Compliment operation.

Logic diagram

Truth Table } 1M

A	C
0	1
1	0

4) NAND logic : The combination of AND gate and NOT gate is called NAND.



Truth Table

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

} 1M

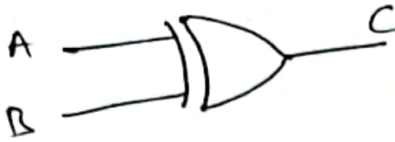
5) NOR logic : The combination of OR gate and NOT gate is called NOR.

Truth Table

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

} 1M

6) Ex-OR logic : If the both inputs are same then only output is high.



$C = A \oplus B$

$= \bar{A}B + A\bar{B}$

Truth table

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

} 1M

7) Ex-NOR logic : If the both inputs are different, then only output is high.

$C = A \odot B$

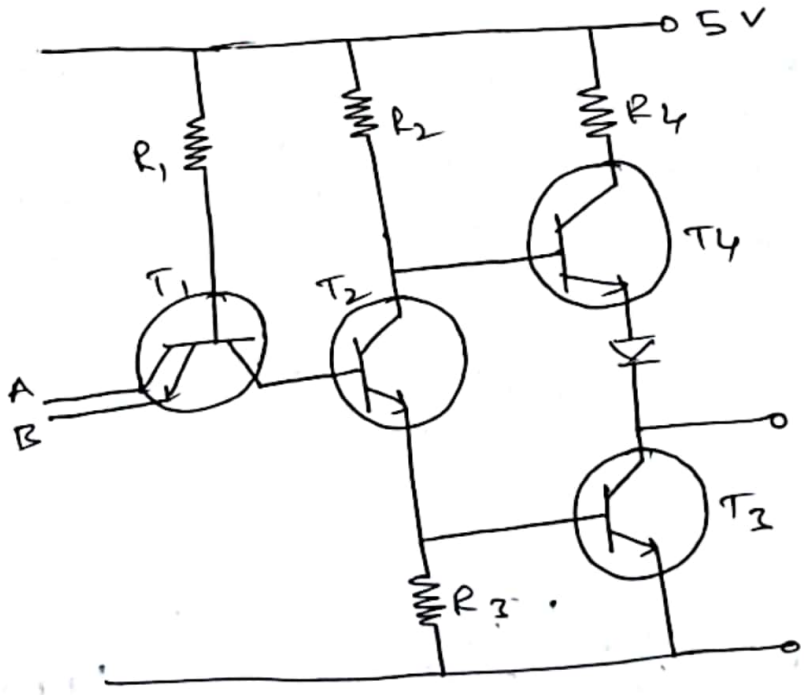
$= \bar{A}\bar{B} + AB$

Truth table

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

} 1M

b)



} 1M

TTL stands for transistor transistor logic. From the above diagram, the transistor T_1 has two emitters to allow two inputs into the transistor. } 2M

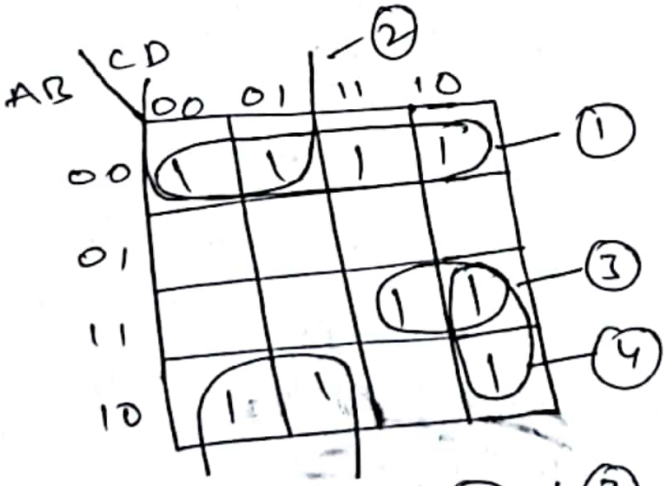
Now, as connected the base voltage will be at 5V. if both the inputs are at logic 1, the potential difference across the base and emitter would be zero or nearly. Hence no current will flow

and the transistor is turned off. So the collector voltage would also be equal to about 5V. Hence this potential can drive current through the emitter of the transistor T_2. This then allow the Collector voltage of the transistor T_2 to fall. Now due to the current flowing through the emitter, there would be a voltage drop accross the resistor R_3. The desired voltage drop would be 0.7V. As seen this is the input of transistor T_1. Hence the transistor is turned on. Due to saturation the Collector voltage will fall about 0.2V which is logic 0. } 2M

for the transistor T_4, Observe that the Emitter voltage is made up of the entire voltage of the transistor T_2 plus the voltage drop accross the diode D about 0.7V. Now the base voltage of transistor T_4 would be the voltage accross base Emitter of the T_1 and the voltage of the entire transistor accross Emitter Collector.

UNIT - II

4) a)



} 4M

$f_{min} = (1) + (2) + (3) + (4)$

$= \bar{A}\bar{B} + \bar{B}\bar{C} + ABC + AC\bar{D}$ } 3M

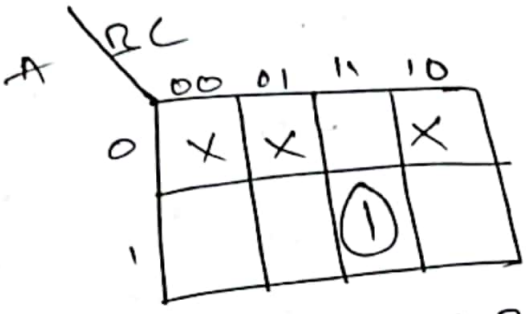
b) XS-3 code. Binary Gray code

A	B	C	$B_3B_2B_1$	$G_3G_2G_1$
0	1	1	0 0 0	0 0 0
1	0	0	0 0 1	0 0 1
1	0	1	0 1 0	0 1 1
1	1	0	0 1 1	0 1 0
1	1	1	1 0 0	1 1 0

2M

1	0	1
1	1	0
1	1	

Don't cares.



$G_3 = \sum m(4) + d(5,6,7)$

$G_3 = \sum m(7) + d(0,1,2)$

$G_3 = ABC$

$G_2 = \sum m(5,6,7) + d(0,1,2)$

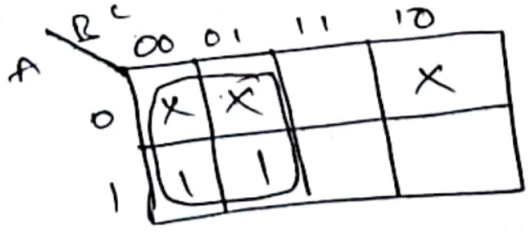
$G_2 = AC + B\bar{C}$

(or)

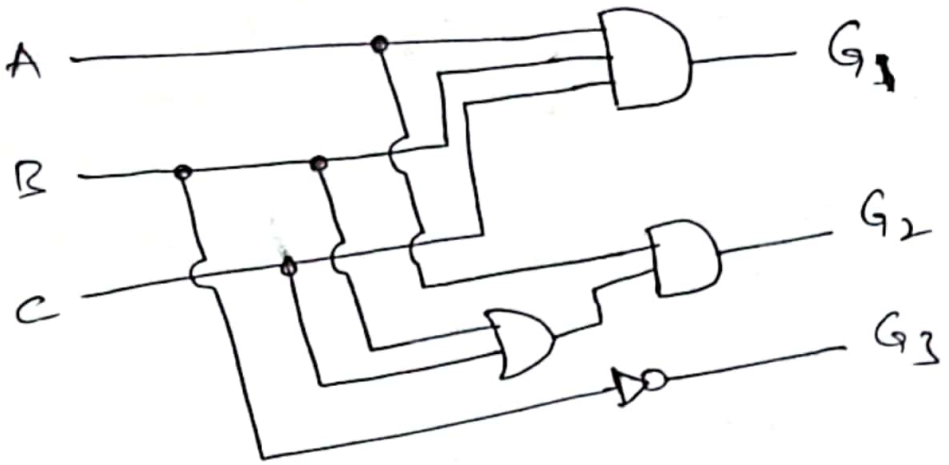
$AC + AB$

3M

$G_3 = \sum m(4,5) + d(0,1,2)$



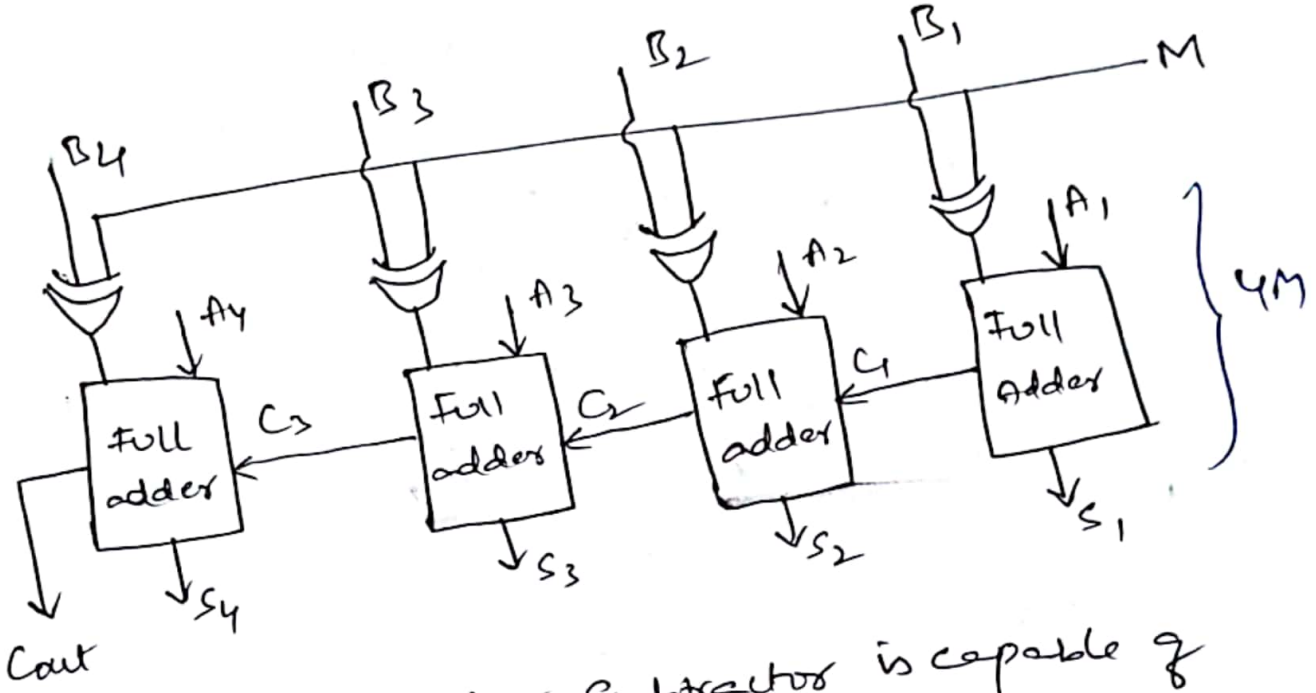
$G_3 = \bar{A}$



2M

(OR)

5) a)



4M

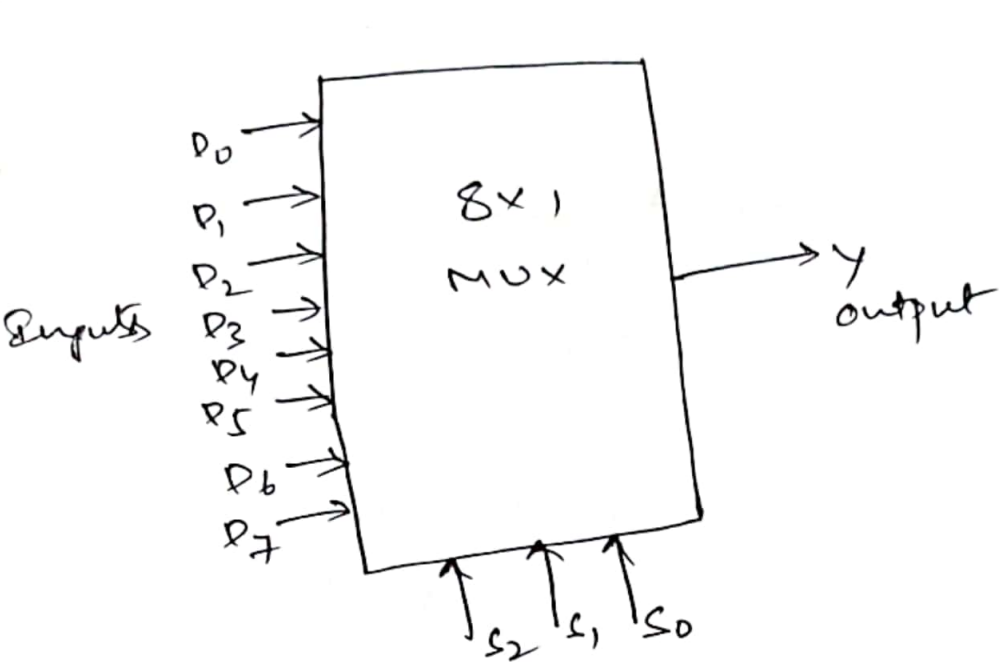
A Binary adder Subtractor is capable of both the addition and subtraction of binary numbers in one circuit itself.

Here we are using one extra input called Mode Control input. when mode Control input is 1, circuit acts as adder and when it is 0, circuit acts as subtractor. the final output of the circuit is $S_{out} S_4 S_3 S_2 S_1$.

3M

5)

b) An 8×1 MUX consists of eight data inputs D_0 through D_7, three input select lines S_0 through S_2 and a single output line Y. Depending on the select lines combinations, multiplexer selects the inputs. } 1M



} 3M

The truth table of 8×1 MUX is,

Selection inputs			output (Y)
S_2	S_1	S_0	
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

} 1M

UNIT - III

6)

a) **SR to D Flip flop :**

available flip flop = SR

Required = D

Characteristic table of D flip flop is,

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

} 3M

Excitation table of SR flip flop is,

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

from Excitation table extend the characteristic table.

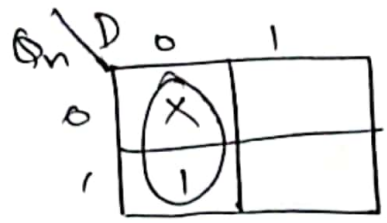
Q_n	D	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	1	0
1	0	0	0	1
1	1	1	X	0

} 3M

$S = \Sigma m(1) + d(3)$

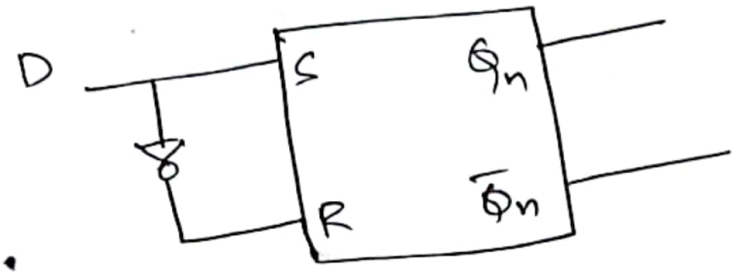
$S =$ D

$R = \Sigma m(2) + d(0)$



$R = \bar{D}$

Required D flip flop is,



1M

JK to D flip flop

Available flip flop = JK

Required = D

Characteristic table of D flip flop is,

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

3M

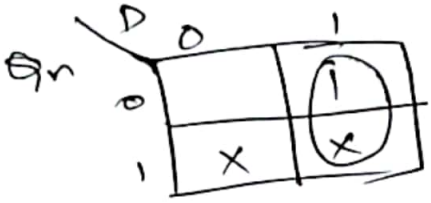
Excitation Table of JK flip flop is,

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

From Excitation table, Extend the characteristic table,

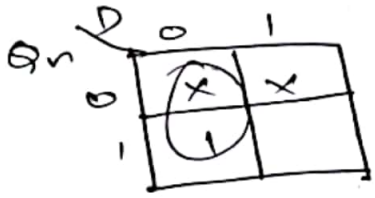
Q_n	D	Q_{n+1}	J	K
0	0	0	0	x
0	1	1	1	x
1	0	0	x	1
1	1	1	x	0

$J = \sum m(1) + d(2,3)$



$J = D$

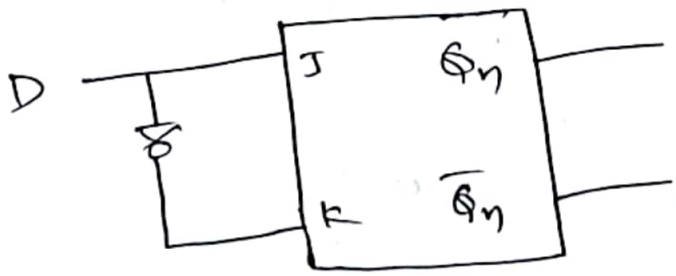
$K = \sum m(2) + d(0,1)$



$K = \bar{D}$

3M

∴ Required ~~FF~~ flip flop is,



1M

(OR)

7) a) Here 4 bits ⇒ 4 flip flops required.

Excitation table of D-flip flop is,

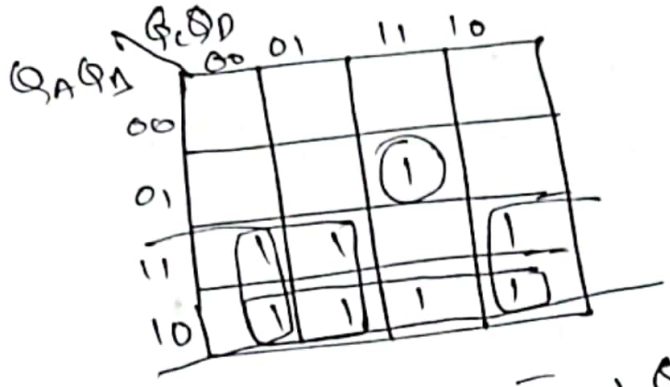
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

} 1M

Q_A	Q_B	Q_C	Q_D	Q_A^+	Q_B^+	Q_C^+	Q_D^+	D_A	D_B	D_C	D_D
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	1	0	0	1	1	0	0
1	1	0	0	1	1	0	1	1	1	0	1
1	1	0	1	1	1	1	0	1	1	1	0
1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	0	0	0	0	0	0	0	0

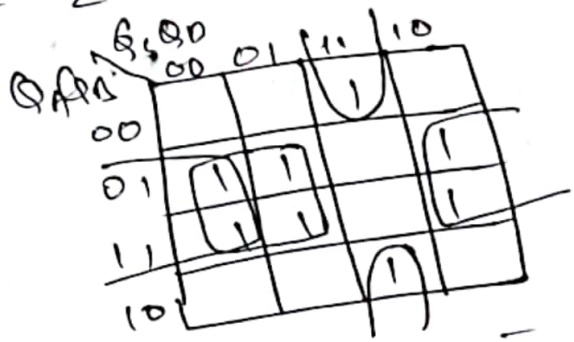
} 2M

$D_A = \sum m(7, 8, 9, 10, 11, 12, 13, 14)$



$D_A = Q_A \bar{Q}_B + Q_A \bar{Q}_C + Q_A \bar{Q}_D + \bar{Q}_A Q_B Q_C Q_D$

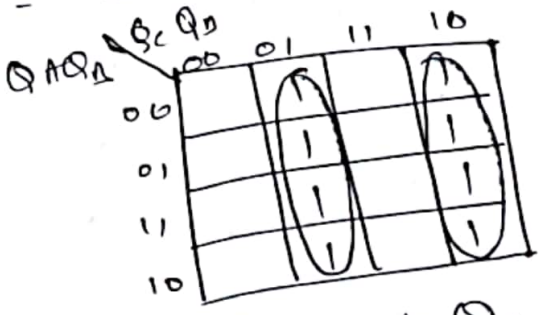
$D_B = \sum m(3, 4, 5, 6, 11, 12, 13, 14)$



$D_B = Q_B \bar{Q}_C + Q_B \bar{Q}_D + \bar{Q}_B Q_C Q_D$

2M

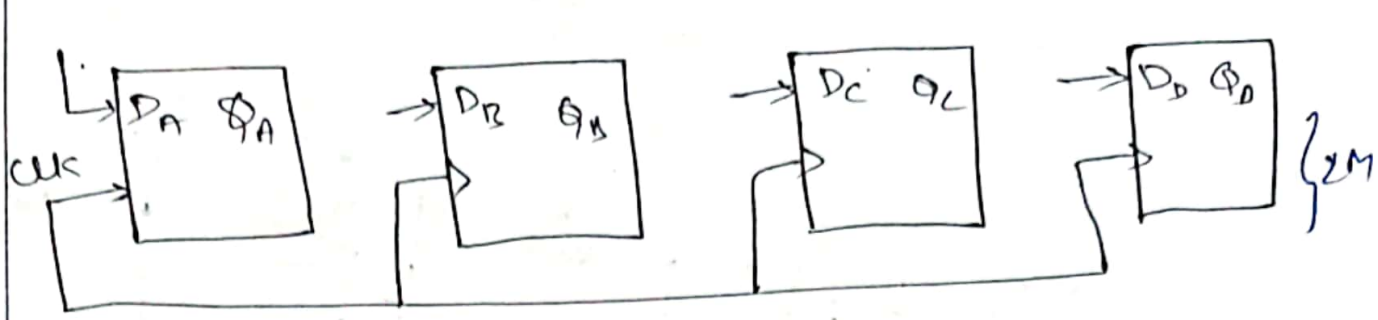
$D_C = \sum m(1, 2, 5, 6, 9, 10, 13, 14)$



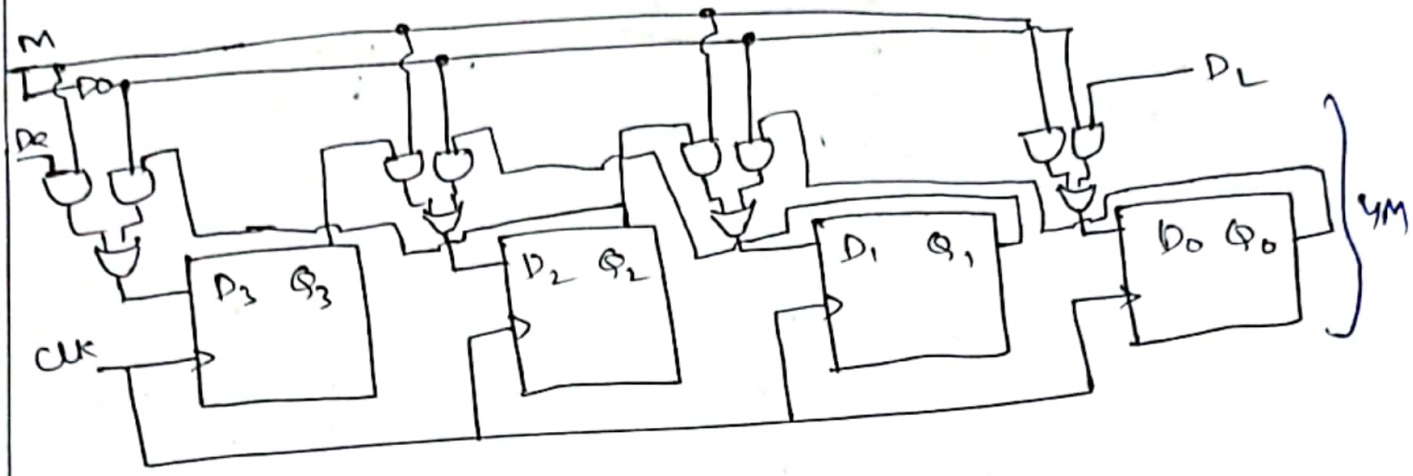
$D_C = \bar{Q}_C Q_D + Q_C \bar{Q}_D$

$D_D = \sum m(0, 2, 4, 6, 8, 10, 12, 14)$

$D_D = \bar{Q}_D$



b)

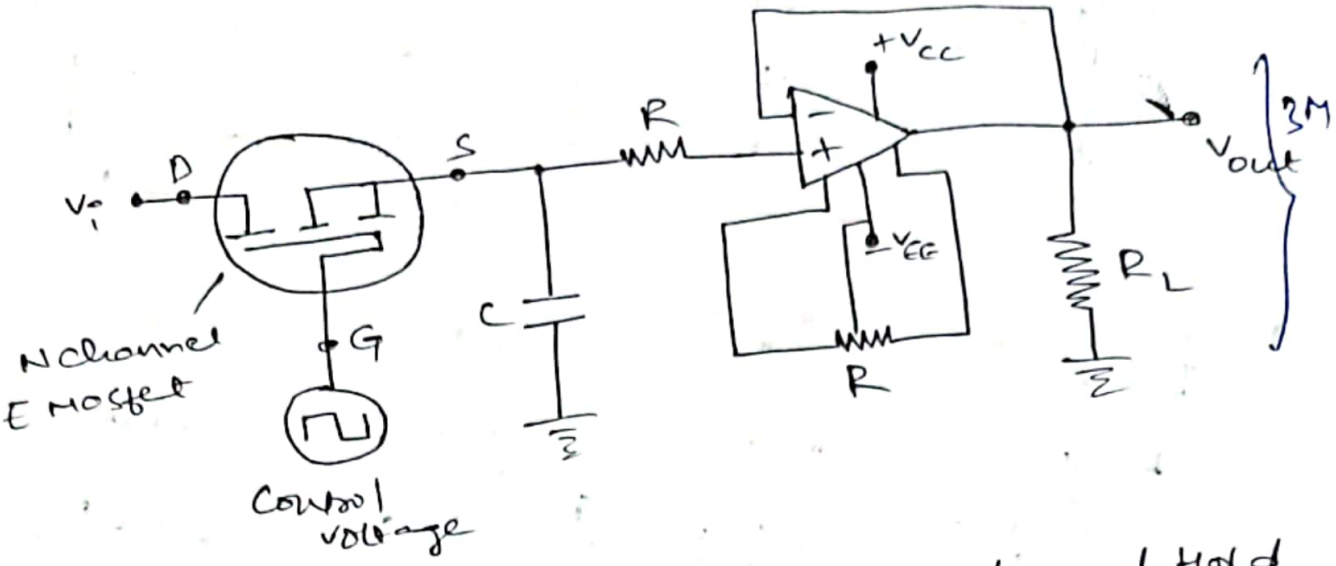


A Bidirectional shift register is used for shifting the data in either left or right side based on the input. This register can be implemented through a D flip flop and logic gates which allow the data bit transfer from one stage to next stage to any side either right or left based on an input signal. Here the direction of data shifting depends upon the mode control input. 3M

Mode control input is a extra input used to choose the operation as left shift or right shift. If the mode control input is 1, then the register operates as right shift whereas if mode control input is zero, the register operates as left shift register.

Unit - IV

8) a)

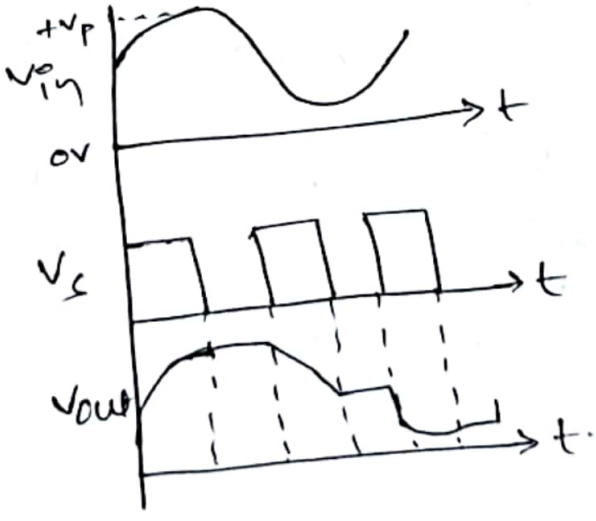


3M

The main components which a sample and Hold circuit involves is an N-channel Enhancement type MOSFET, a capacitor to store and hold electric charge and a high precision operational amplifier.

The N channel Enhancement MOSFET will be used a switching element. The input voltage applied through its drain terminal and Control voltage will be applied through its gate terminal. When the positive pulse of the control voltage is applied, the MOSFET will be switched to ON state and it acts as a closed switch. When the control voltage is zero then the MOSFET will be switched to off state and acts as open switch.

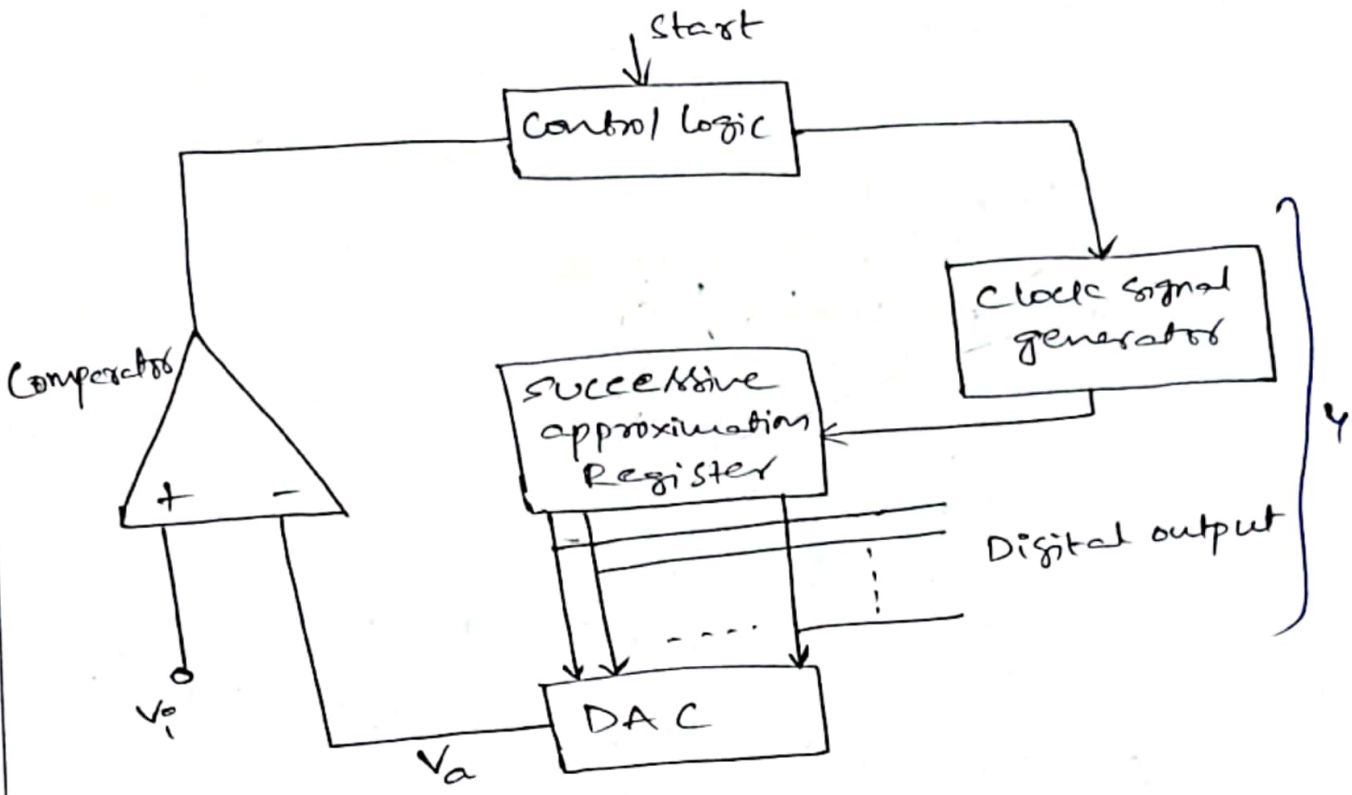
2M



→ Input and output waveforms.

2M

b)



A successive approximation type ADC produces a digital output which is, approximately equal to the analog input by using successive approximation technique internally.

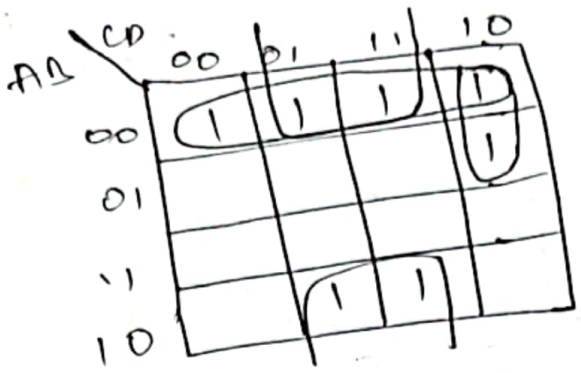
The successive approximation type ADC mainly consists of 5 blocks — clock signal generator, successive approximation register (SAR), DAC, comparator and control logic. 3M

The control logic resets all the bits of SAR and enables the clock signal generator inorder to send the clock pulses to SAR. The binary data present in SAR will be update for every clock pulse. The DAC converts the received digital input into an analog output. The comparator compares this analog value V_a with the external input value V_i. The output of comparator will be 1 as long as V_i is greater than V_a. The output of comparator is zero, when V_i is less than V_a.

10

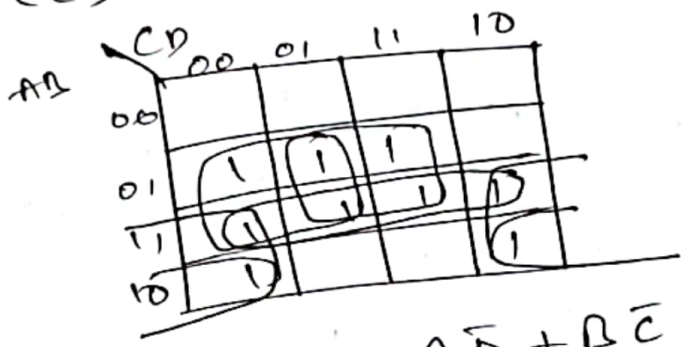
(OR)

9) $f_1(G)(A,B,C,D) = \Sigma m(0,1,2,3,6,9,11)$



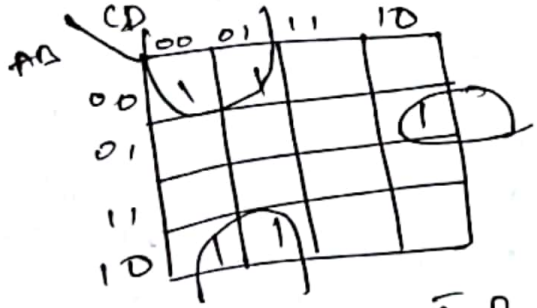
$f_1(T) = \bar{A}\bar{B} + \bar{B}D + \bar{A}C\bar{D}$

$F_1(C) = \Sigma m(4,5,7,8,10,12,13,14,15)$ } 3M



$f_1(C) = A\bar{D} + B\bar{C} + BD$

$F_2(T) = \Sigma m(0,1,6,8,9)$



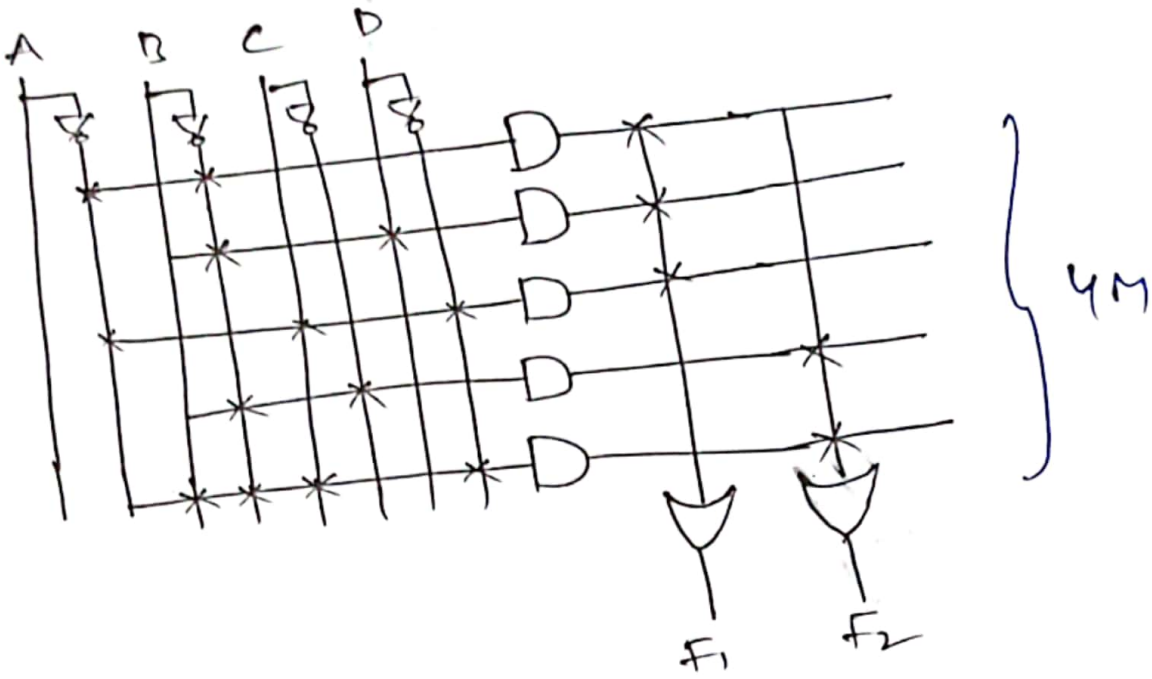
3M

$F_2(T) = \bar{B}\bar{C} + \bar{A}BC\bar{D}$

$f_2(C) = \Sigma m(2,3,4,5,7,10,11,12,13,14,15)$

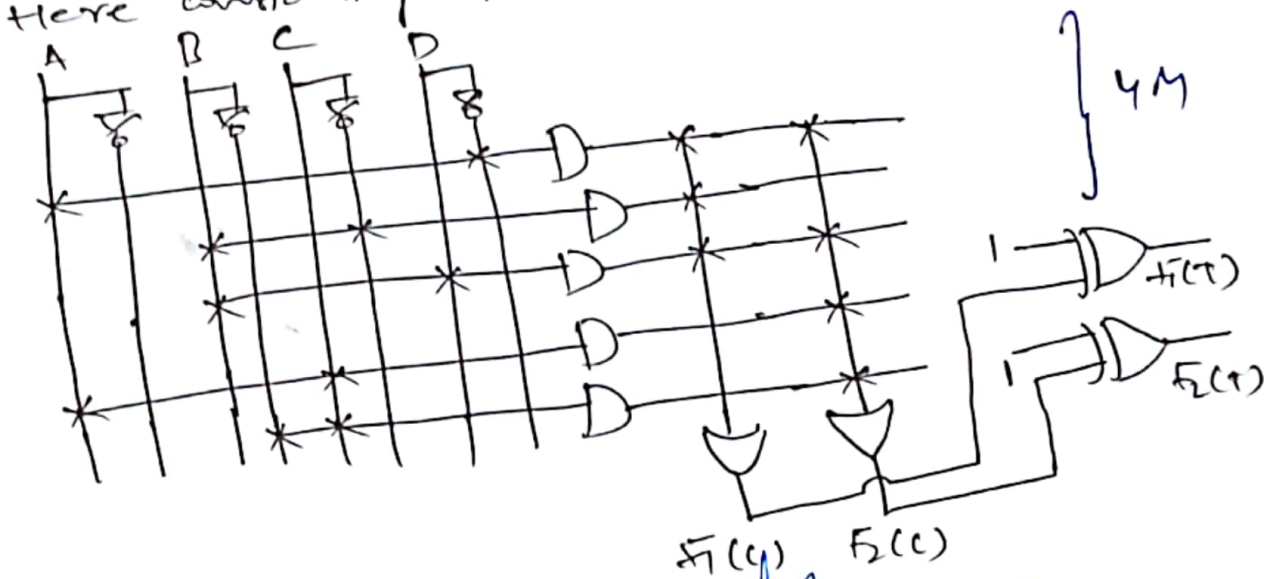
$f_2(C) = B\bar{C} + AC + \bar{B}C + BD.$

PLA Table



PAL Table

Here considering $F_1(c)$ & $F_2(c)$



Scene prepared by

1. Sai Goutham Gollu
(8500588472)

2. M. Siva Ramakrishna
(9700801417)

M Ravikumar
HOD, EEE Dept