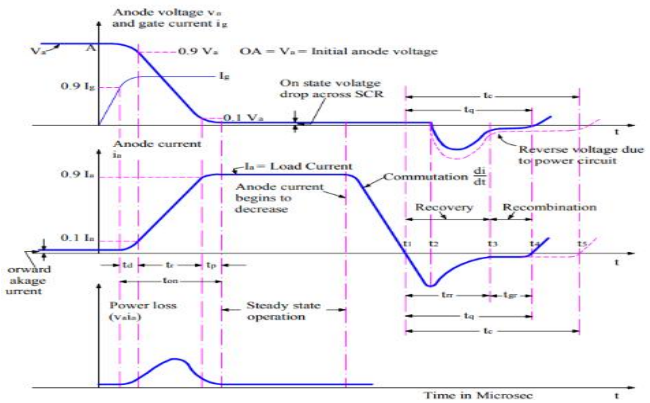
III/IV B.Tech Supplementary Examination Juy/August 2023
Power Electronics (20EE504)

1

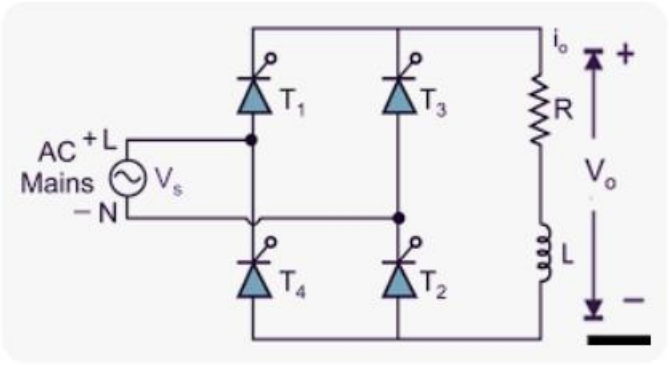
a



b It is the minimum value of anode current at which the SCR is in ON position

c he output voltage reduces as the load current reduces. In addition, the input current and output voltage waveforms change significantly.

d



e Turning OFF of the SCR is called Commutation, the process in which the reverse current flows in the SCR, then it comes to reverse bias condition.

f

Forward Voltage Triggering.

Temperature Triggering.

dv/dt Triggering.

Light Triggering.

Gate Triggering. DC Gate Triggering. AC Triggering. Pulse Triggering.

g a Snubber circuit is the combination of resistor and capacitor. Capacitor, used in Snubber circuit, is able to prevent the device from unwanted dv/dt triggering of the Thyristor or SCR. As the voltage is applied to the circuit a sudden voltage appears across the switching device.

h It is the angle at which the SCR gets turned on and starts conducting. This is the angle where the designers apply the gate pulse to control SCR/Thyristor.

i

Power Switching Circuit.

Controlled Rectifier.

AC power control circuits.

Speed control of DC shunt motor.

SCR Crowbar.

Computer logic circuits.

Timing Circuits.

Inverters.

J Modulation index is defined as the ratio of the amplitude of the modulating wave to that of the carrier wave.

k A buck converter or step-down converter is a DC-to-DC converter which steps down voltage (while stepping up current) from its input (supply) to its output (load). It is a class of switched-mode power supply.

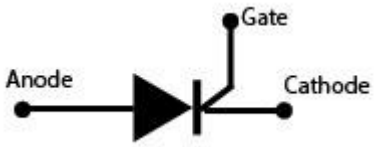
l The ratio of ON time to total time is defined as duty cycle.

m An inverter is an electrical device, and it is capable of changing a DC current to an AC current at a given frequency as well as voltage. Single phase, three phase inverters.

n Which converts from DC to AC , It takes power from an electric current and converts it to DC current, which is then sent to an electrical panel. The end result is that the stored energy is available to you whenever you need it.

UNIT-I

2 a SCR stands **for Silicon-controlled rectifier**. The SCR is a very important member of the thyristor family. It is more popular than other thyristor family members like TRIAC, and DIAC even though that thyristor is used interchangeably with SCR.



The three terminals of the SCR are named **anode, cathode, and gate**. For proper working, connect the anode of the SCR with positive and cathode with negative of the battery. A positive pulse for a short duration is required at the gate to kick start the conduction.

SCR has four layers of extrinsic semiconductor materials. These four-layer form three PN junctions named J1, J2, and J3. The layers are either NPNP or PNPN. The anode and cathode terminals are placed at the end layers and where the gate terminal is placed with the third layer. The outer layers are heavily dopped and the inner two layers are lightly dopped. The **SCR Construction** is illustrated here below.

1. Forward Blocking Mode
2. Forward Conduction Mode
3. Reverse Blocking Mode

When anode of SCR connects to the positive and cathode of SCR with the negative of the battery terminal. And no pulse is applied at the gate terminal. The SCR work in the forward blocking mode. This means that SCR will not conduct even though the polarity of SCR is forward bias.In forward blocking mode, the J1 and J3 PN junctions are forward biased. But the middle junction J2 is reverse biased, therefore, the SCR will not conduct in the forward blocking mode.

Forward Conduction Mode of SCR

Forward conduction mode is the only mode of SCR for conduction. The SCR can be set into the forward conduction mode in two ways. First by providing the gate pulse to forward bias the J2 junction. Second by increasing the anode to cathode voltage to break down the J2 junction. The gate pulse method is preferred and suitable for many applications. The breakdown method reduces the SCR lifetime. The SCR will remain in conduction mode even after the removal of the gate

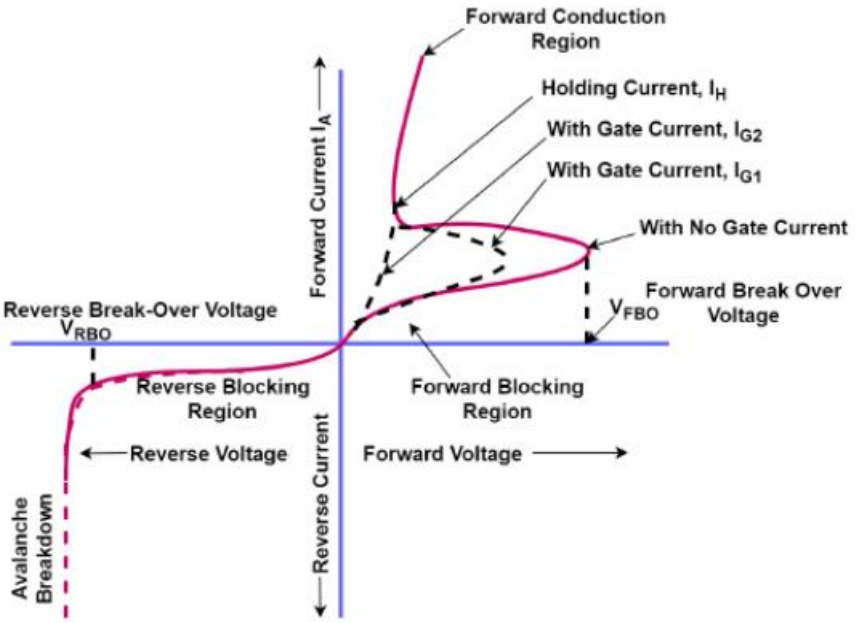
pulse or reducing the applied voltage. If the anode current of the SCR drops below the holding current the SCR will stop falling back to forward blocking mode.

Reverse Blocking Mode in SCR

If the anode terminal of the SCR connects to the negative and cathode terminal of SCR connects to the positive of battery terminals. The SCR is in reverse blocking mode. In this mode, J1 and J3 junctions are reverse biased. Where the middle junction J2 is forward bias. As two junctions are reverse bias, so there is no current flowing through it but only a small leakage current due to the drift charge carrier.

VI Characteristics of SCR

The curve of **VI characteristics of SCR** is obtained by chang



V I Characterstics of SCR

When the voltage reaches the VBO point, the SCR starts the current flow. Alternatively, the SCR can be put into the forward conduction mode by applying the gate that will increase the anode current above the latching current. A higher gate current can put SCR faster in the forward conduction mode as in the graph Ig3>Ig2>Ig1. The SCR will remain in the **forward conduction mode** if the anode current is above the **holding current**.

b) Commutation in Power Electronics refers to the process of commutation of SCR. Whenever we talk of commutation in power electronics, we simply mean the process to turn off an SCR. This article details about the commutation of SCR, Natural Commutation, Forced Commutation and various types of Forced Commutation techniques.

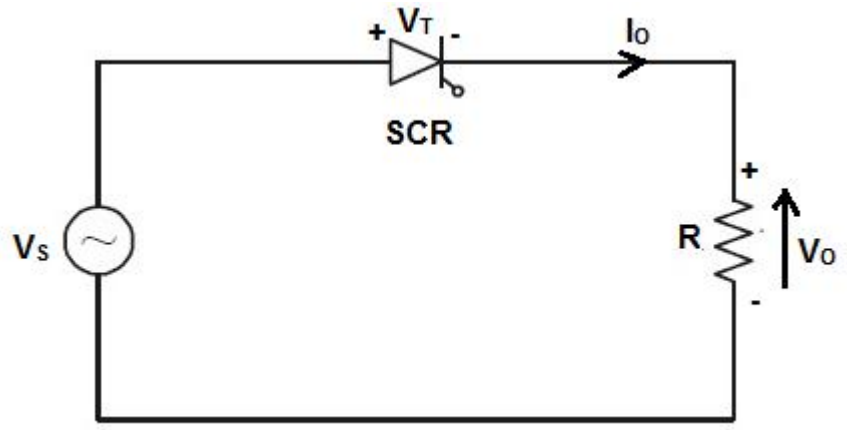
Commutation of SCR is defined as the process of turning off an SCR / thyristor. It is the process by which an SCR or thyristor is brought to OFF state from ON state. We know that, an SCR is turned on by applying a gate signal to a forward biased SCR. Please read "Required Conditions to Turn-on an SCR" for better understanding. But for the purpose of power control or power conditioning,

it is required to turn off SCR as and when required. Turn off of a thyristor means bringing it to forward blocking mode from forward conduction mode. We also know that, once an SCR goes in forward conduction mode, gate loses its control. This means, some external techniques / circuit must be employed to turn off SCR. This external circuit is known as commutation circuit.

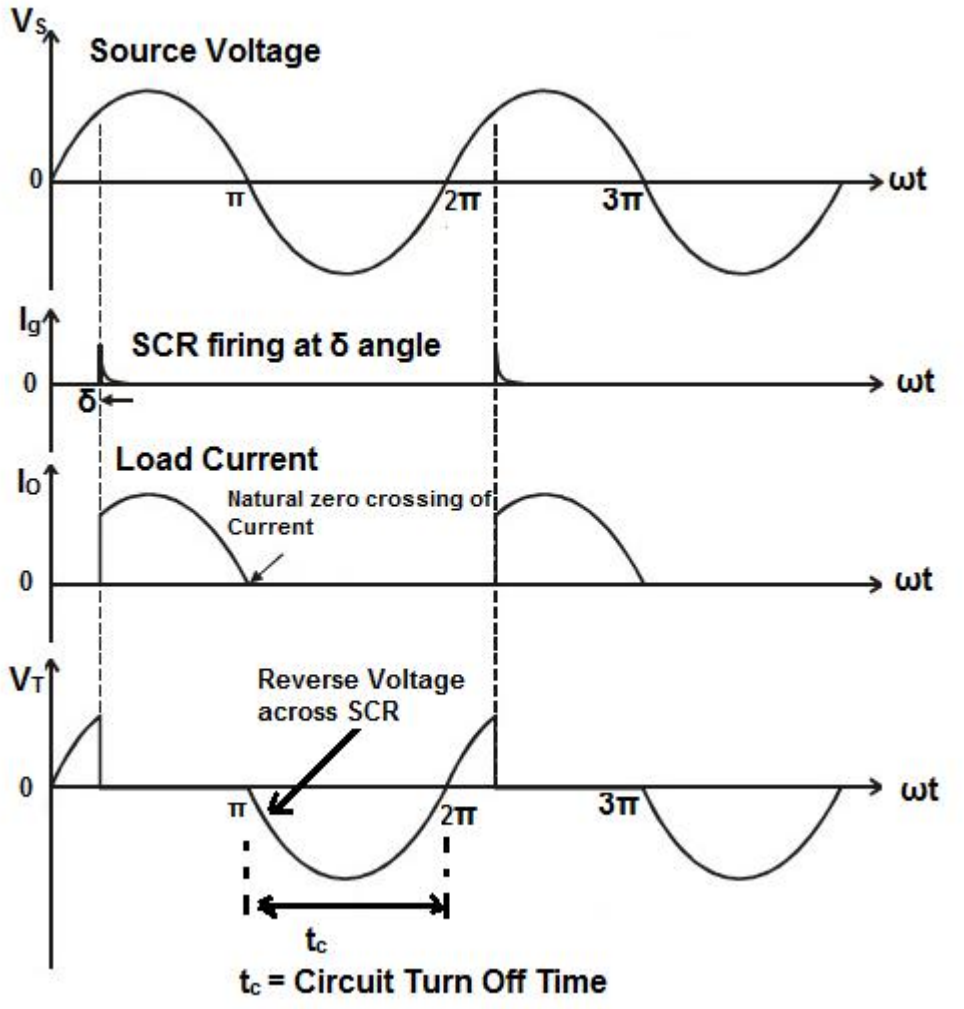
To turn off an SCR / thyristor, it is required that its anode current should fall below the holding current and a reverse voltage should be applied across the SCR for the sufficient time so that it regains to forward blocking mode from forward conduction mode. Thus, to turn off an SCR some methods must be applied so that the above mentioned conditions can be met to turn off SCR as per requirement. This method of turning off an SCR / thyristor is called commutation process.There are mainly two types of SCR commutation techniques: Natural Commutation and Forced Commutation.

Natural Commutation of SCR:

Natural Commutation of SCR is the process of turning off an SCR without using additional commutation circuitry. This commutation technique only occurs in AC circuit. For better understanding, let us consider an SCR circuit energized from AC source.



When SCR is conducting, the current will pass through zero after every positive half cycle. After that, the AC source then applies a reverse voltage across the terminals of SCR till the beginning of second cycle. If the time of application of reverse voltage applied by the AC source is more than the SCR turn-off time, then SCR will get turned off.



From the above waveform, following points can be noted:

a. SCR is fired or gated at an angle of δ on the Source Voltage.
b. The waveform of output current or SCR anode current (Io = Vo / R) is sinusoidal as the load is resistive load.
c. When the AC Source Voltage reaches zero at ωt = π, the load current or SCR anode current becomes zero.
d. After ωt = π, the source voltage becomes negative and hence, the voltage across SCR also becomes negative. Thus SCR is reversed biases from ωt = π to ωt = 2π i.e. for a time period of tc = (π / ω). This time tc is called ***Circuit Turn Off time***.
e. ***If tc is more than the SCR turn off time, then SCR will get turned off***.

Thus we see that, the SCR is getting turned off due to the natural tendency of AC. This is the reason, this type of commutation technique is called Natural Commutation. It should also be noted that, no additional circuitry is required in this commutation technique. This commutation technique is basically the Class-F commutation (you might encounter in many literature) technique which is also known as Line Commutation of SCR.

Forced Commutation of SCR:

Unlike natural commutation, an external circuitry is required to forcibly bring the SCR andoe current below holding current and keeping SCR reversed biased for a period more than the SCR / thyristor turn off time. This technique is applied for DC circuit. The commutation circuitry for forced commutation comprises of Inductor and capacitor. Forced commutation is applied to Choppers and Inverters.

There are several forced commutation techniques. They are as follows:

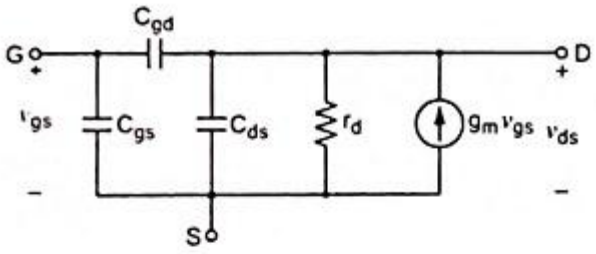
- Class-A Commutation (also known as Load Commutation)
- Class-B Commutation (also known as Resonant Pulse Commutation)
- Class-C Commutation (often called Complimentary Commutation)
- Class-D Commutation or Impluse Commutation
- Class-E Commutation or External Pulse Commutation

OR

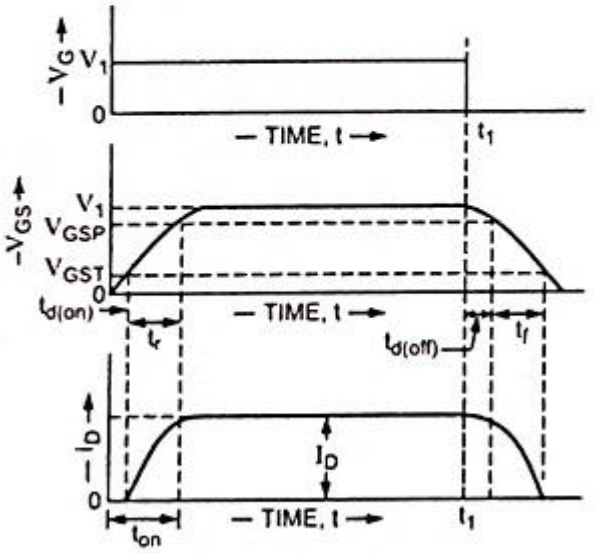
3 a Power MOSFET is an enhancement mode device modified to handle much large currents and voltages than a conventional MOSFET. Prior to the invention of the power MOSFETs, MOSFETs could not compete with the power ratings of larger BJTs. But now the power MOSFETs are better than the power BJTs in many applications requiring high load power.
one main advantage of power MOSFETs is that they are inherently temperature stable and cannot go into thermal runaway. Another advantage of power MOSFETs is that they can be operated in parallel while power BJTs cannot.

In addition to above, Switching Characteristics of Power MOSFET have the advantage of switching a large current off faster than a BJTs can because a power MOSFET does not have minority carriers. They are 10 to 100 times faster than with comparable BJTs.

During cut-off the gate-to-source vgs is less than threshold value. To turn on, vgs is to be increased to well above the threshold value. The drain-to-source voltage must be less than vgs – VGST. The Switching Characteristics of Power MOSFET are influenced to a large extent by the internal capacitances of the device and the internal impedance of the gate drive circuit.



(a) Switching Model of MOSFETs



(b) Switching waveforms

Fig. 31.15

The Switching Characteristics of Power MOSFET is shown in Fig. 31.15(a). The three internal capacitances are gate-to-source capacitance Cgs, gate-to-drain capacitance Cgd and drain-to-source Cgd. During turning on Cgd and Cgs are to be charged through gate. This charging takes a finite time. So, the turn on cannot be instantaneous. Moreover, these capacitances are nonlinear and are not constant but dependent on dc bias voltage.

The typical switching waveforms of Power MOSFETs are shown in Fig. 31.15(b).

The **turn-on delay td(on)** is the time that is required to charge the input capacitance to threshold voltage level. The **rise time tr** is the gate charging time from the threshold level to the full-gate voltage VGSP. During rise time, drain current rises from zero to full-on current ID. Thus, the total turn-on time ton = td(on) + tr. The turn-on time can be reduced by using low-impedance gate-drive source.

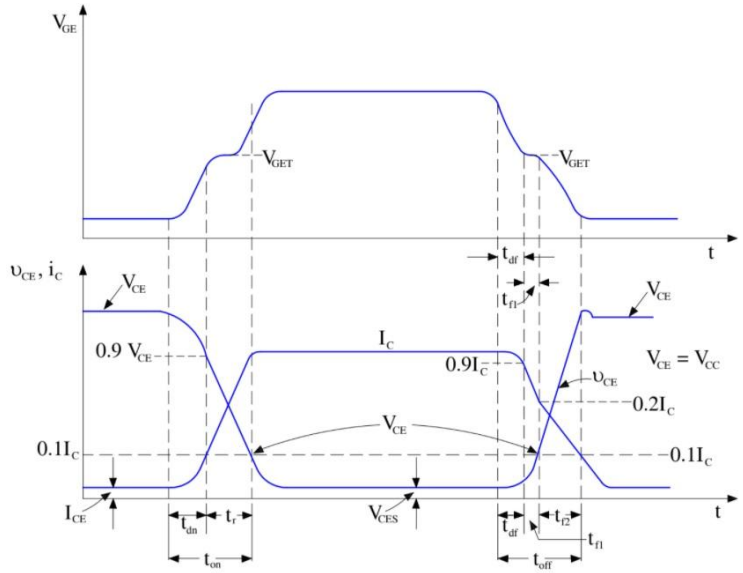
As the MOSFET is the majority carrier device, turn-off process is initiated soon after removal of gate voltage at time t1. The **turn-off delay time td(off)** is the time required for the input capacitance to discharge from the overdrive gate voltage V1 to the pinch-off-region. VGS must decrease significantly before VDS begins to rise. The **fall time**, tf is the time that is required for the input

capacitance to discharge from the pinch-off region to threshold voltage VGST. If VGS ≤ VGST, the transistor turns off. During fall time, drain current reduces from ID to zero.
Switching Characteristics of IGBT is basically the graphical representation of behavior of IGBT during its turn-on & turn-off process.
The turn-on time is defined as the time between the instant of forward blocking to forward conduction mode. Here, forward conduction means the device conducts in forward direction. Turn-on time (ton) is basically composed of two different times: Delay time (tdn) and Rise time (tr). Therefore, we can say that ton = tdn + tr.

The delay time is defined as the time for the collector-emitter voltage (VCE) to fall from VCE to 0.9VCE. This simply means that, the collector-emitter voltage drops to 90% in delay time and hence the collector current rises from initial leakage current to 0.1IC (10%). Thus, delay time may also be defined as the time period during which collector current rises from zero (in fact a small leakage current) to 10% of the final value of collector current IC.

The rise time tr is the time during which collector-emitter voltage falls from 0.9VCE to 0.1 VCE. This means, during rise time collector-emitter voltage falls to 10% from 90%. Therefore, the collector current builds up to final value of collector current IC from 10%. After time ton, the collector current becomes IC and the collector-emitter voltage drops to very small value called conduction drop (VCES).

A typical Switching Characteristics of an IGBT is shown below. You may corelate the delay time, rise time and turn-on time.



- Delay Time, tdf
- Initial Fall Time, tf1
- Final Fall Time, tf2

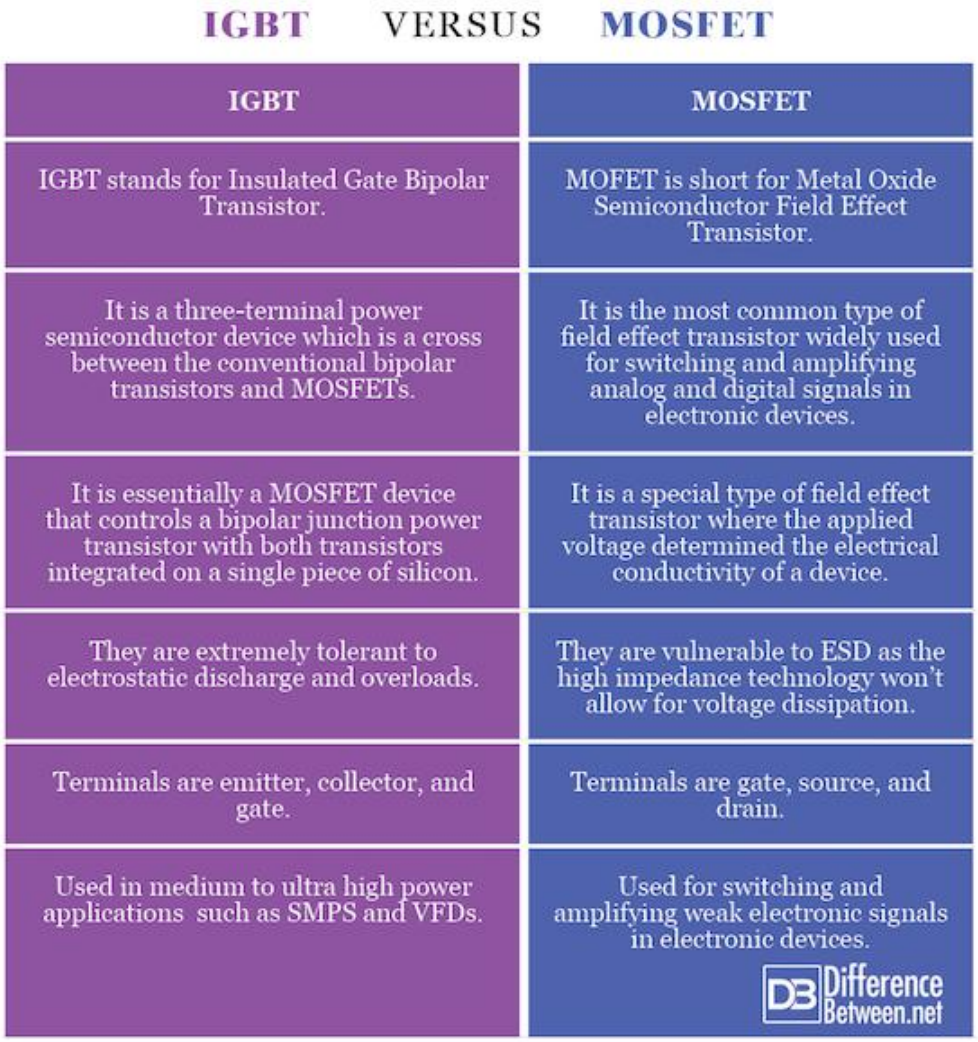
Thus, turn-off time is the sum of above three different time intervals i.e. toff = tdf + tf1 + tf2. Kindly refer the switching characteristics of IGBT for

interpretation of above times.

The delay time is the time during which gate voltage falls from VGE to threshold voltage VGET. As gate voltage falls to VGE during tdf, the collector current falls from IC to 0.9IC. At the end of delay time, collector-emitter voltage begins to rise.

The first fall time tf1 is defined as the time during which collector current falls from 90% to 20% of its final value IC. In other words, it is the time during which collector-emitter voltage rises from VCES to 0.1VCE.

The final fall time tf2 is the time during which collector current falls from 20% to 10% of IC or the time during which collector-emitter voltage rises from 0.1VCE to final value VCE.



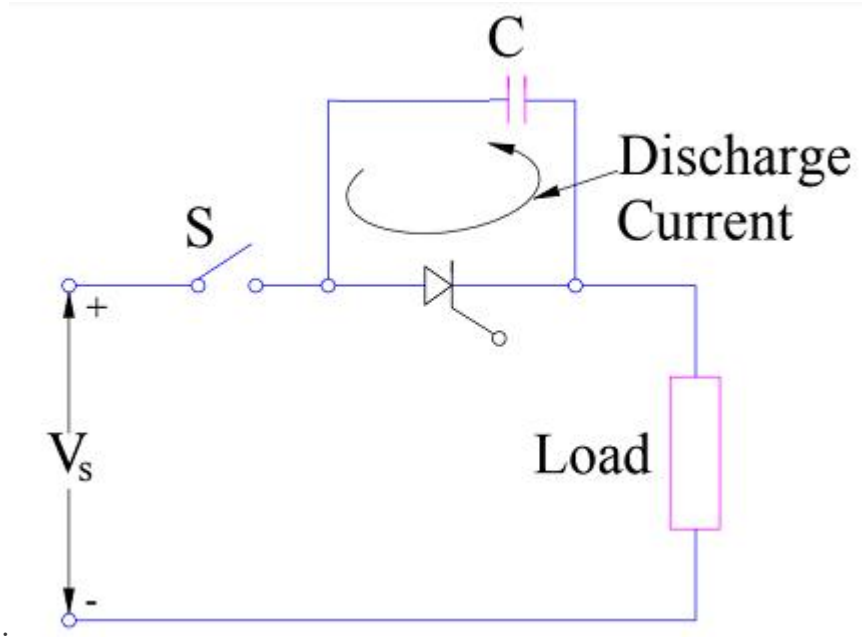
b) a Snubber circuit is the combination of resistor and capacitor. Capacitor, used in Snubber circuit, is able to prevent the device from unwanted dv/dt triggering of the Thyristor or SCR. As the voltage is applied to the circuit a sudden voltage appears across the switching device

Purpose of Snubber Circuit

The main purpose of Snubber Circuit is to prevent the unwanted triggering of SCR or thyristor due to high rate of rise of voltage i.e. dv/dt. We already know that if the rate of rise of anode to cathode voltage of SCR is high then it may lead to false triggering. This is commonly known as dv/dt triggering. Thus we need to have some arrangement to protect SCR from such undesirable turning. Application of Snubber Circuit prevents from such spurious triggering of SCR. Thus it is basically dv/dt protection of SCR.

Design and Working Principle of Snubber Circuit

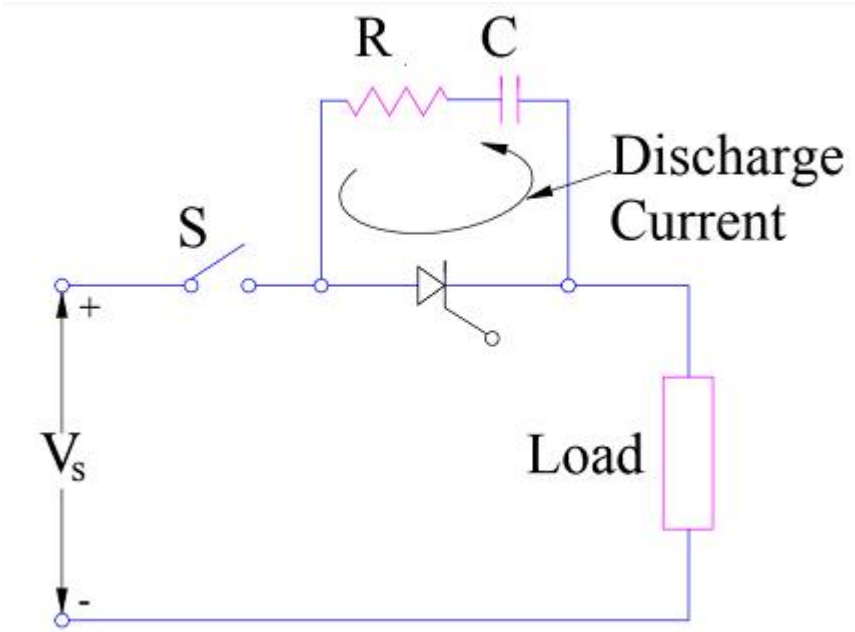
As we need to limit the rate of rise of anode to cathode voltage of SCR during its turn on process, this means we should use a capacitor the SCR terminals. This is because a capacitor limits the rate of rise of voltage whereas an inductor limits the rate of rise of current. Thus a capacitor when connected across the SCR terminals, when limit dv/dt. Lets us now connect the capacitor across the SCR terminals and see how this affects the dv/dt.



As you can see, we have connected capacitor C in parallel with SCR. When switch S is closed, a sudden voltage appears across the circuit. Initially capacitor C behaves like a shorted path and hence the voltage across SCR is zero. But as time passes, voltage starts building up across capacitor C with a slow rate. Thus the rate of rise of voltage dv/dt across SCR terminals will also be slow and less than the specified dv/dt rating of SCR.

But the above circuit design has one problem. Let us go deep into the above circuit to make improvement. As you can see, before SCR is fired or triggered by applying gate pulse, the capacitor C is fully charged up to supply voltage Vs. As soon as SCR is turned on by gate pulse, this charged capacitor C discharges

through SCR. Hence a current having magnitude (***Vs/Resistance of loop formed by SCR and Capacitor C***) flows in the local path formed by SCR and capacitor C. Since the value of resistance of this local path is quite small, the magnitude of discharge current will be quite higher. This will lead to high value of di/dt which may exceed the specified di/dt rating of SCR. In order to limit the magnitude of the discharge current, aa resistance should be connected in series with the capacitor C. This is shown below.



The above circuit is the actual Snubber Circuit. Thus, a snubber circuit comprises of series combination of resistance and capacitance in parallel with SCR or thyristor. Generally, resistance R, capacitance C and load parameters are so chosen that the dv/dt during charging of capacitor C is less than the specified dv/dt rating of SCR and the discharge current at the turn on of SCR is less than the specified di/dt rating. Normally, R, C and load parameter forms an underdamped circuit so that dv/dt is limited to acceptable value as provided by the SCR rating.

UNIT-II

4 a A single phase bridge converter needs 4 thyristors. This configuration leads to two quadrant operation. Such a converter is called the **two-quadrant converter** or **fully controlled converter**. Many times the bridge circuit is modified by replacing two thyristors by two diodes. This configuration leads to one quadrant operation (operation is restricted to first quadrant). Such a converter is called the **one-quadrant converter** or a **semiconverter**.

The load on the converter may be purely resistive, inductive (R-L) load or R-L-E load. An R-L-E load consists of resistance, inductance and motor (E stands for back emf of motor). The load may also have a battery (emf E) instead of motor.

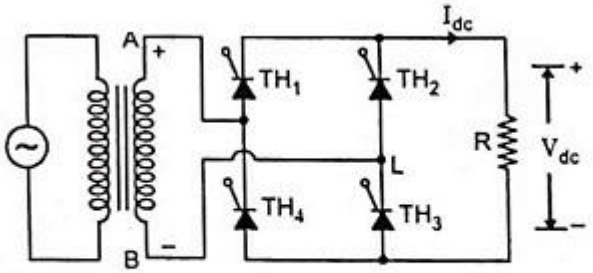


Fig. 27.13 *Single Phase Full-Wave Fully Controlled Rectifier (or Full Converter) With Resistive Load*

1. With Resistive Load: A fully controlled full-wave bridge rectifier is shown in Fig. 27.13. The operation of this circuit is in principle similar to that of the two pulse mid-point circuit shown in Fig. 27.7. All the four devices used in the circuit are thyristors TH1-TH4 for control of output power. In this circuit, diagonally opposite pair of thyristors are made to conduct, and are commutated, simultaneously. During the first positive half cycle, thyristors TH1 and TH3 are forward biased and if they are triggered simultaneously, the current flows through the load via thyristor TH1-load-TH3-source. Thus, during positive half cycle, thyristors TH1 and TH3 are conducting. During the negative half cycle of the ac input, thyristors TH2 and TH4 are forward biased and if they are triggered simultaneously, the current flows through the load via thyristor TH2-load-TH4-source. Thyristors TH1, TH3 and TH2, TH4 are triggered at the same firing angle α in each positive and negative half cycles of the supply voltage respectively. When the supply voltage falls to zero, the current also becomes zero. Thus thyristors TH1, TH3 in positive half cycle and TH2 and TH4 in negative half cycle turn off by natural commutation. The related voltage and current waveforms for this circuit are depicted in Fig. 27.14.

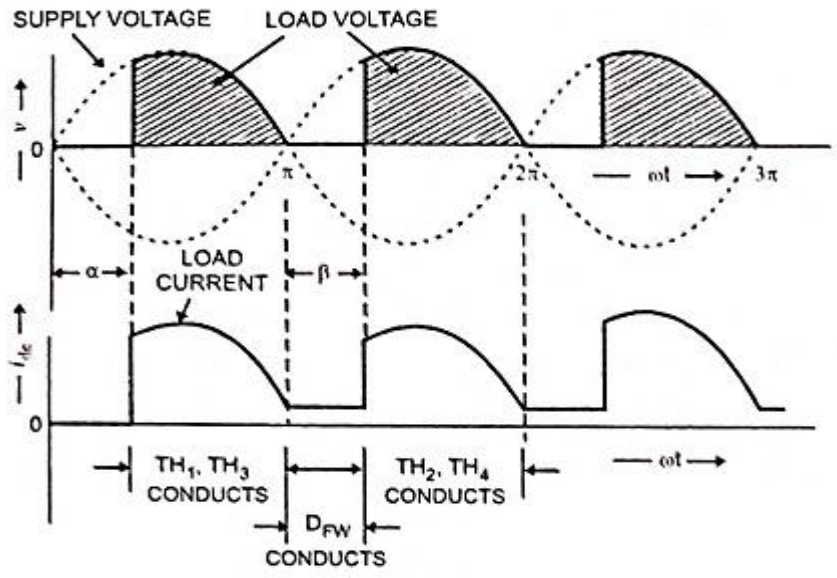


Fig. 27.14 *Waveforms For Full-Wave Converter With Resistive Load*

The relations for Vdc, Idc, VL rms and IL rms for this bridge configuration are
The **output dc voltage** across the resistive load is given by

$$V_{dc} = \frac{1}{\pi}\int_{\alpha}^{\pi} V_{max} \sin \omega t \, d(\omega t) = \frac{V_{max}}{\pi}(1 + \cos \alpha) \qquad ...(27.12)$$

Average load current is given by

$$I_{dc} = \frac{V_{dc}}{R} = \frac{V_{max}}{\pi R}(1 + \cos \alpha) \qquad ...(27.13)$$

The expression for rms value of load voltage for a given firing angle α is

$$V_{L\,rms} = \sqrt{\frac{1}{\pi}\int_{0}^{\pi} V_{max} \sin^2 \omega t \, d(\omega t)}$$

$$= \frac{V_{max}}{\sqrt{2\pi}}\left(\pi - \alpha + \frac{1}{2}\sin 2\alpha\right)^{1/2}$$

$$= V_{max}\left(\frac{\pi - \alpha}{2\pi} + \frac{\sin 2\alpha}{4\pi}\right)^{1/2} \qquad ...(27.14)$$

RMS value of load current is given by

$$I_{L\,rms} = \frac{V_{L\,rms}}{R} = \frac{V_{max}}{R}\left(\frac{\pi - \alpha}{2\pi} + \frac{\sin 2\alpha}{4\pi}\right)^{1/2} \qquad ...(27.15)$$

b)

(4)(b) R = 30Ω

V = 230.

f = 50, α = 0°

Half Controlled Rectifier.

$V_0 = \frac{V_m}{\pi}[1 + \cos\alpha]$

$= \frac{230\times\sqrt{2}}{\pi}[1+1]$

$= 207\,V$

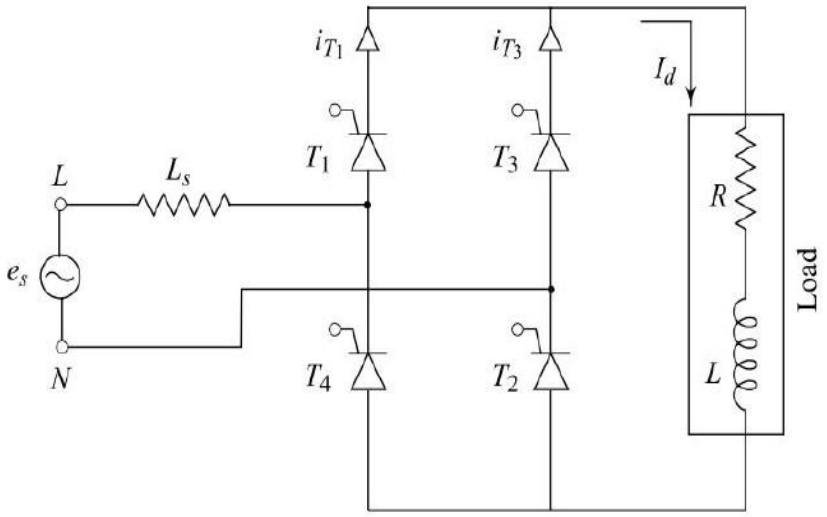
$I_0 = \frac{207}{30} = 6.9\,A.$

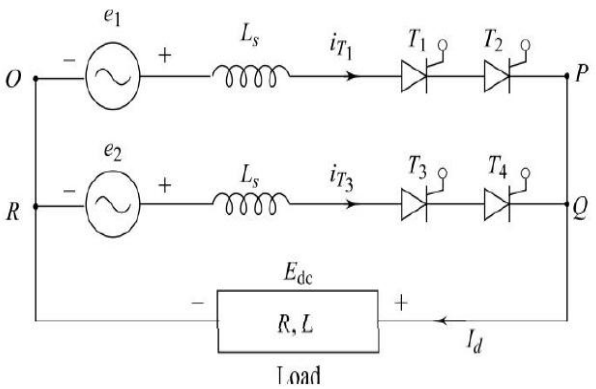
$V_{or} = \frac{V_m}{\sqrt{\pi}}\left[(\pi-\alpha) + \frac{1}{2}\sin 2\alpha\right]^{1/2}$

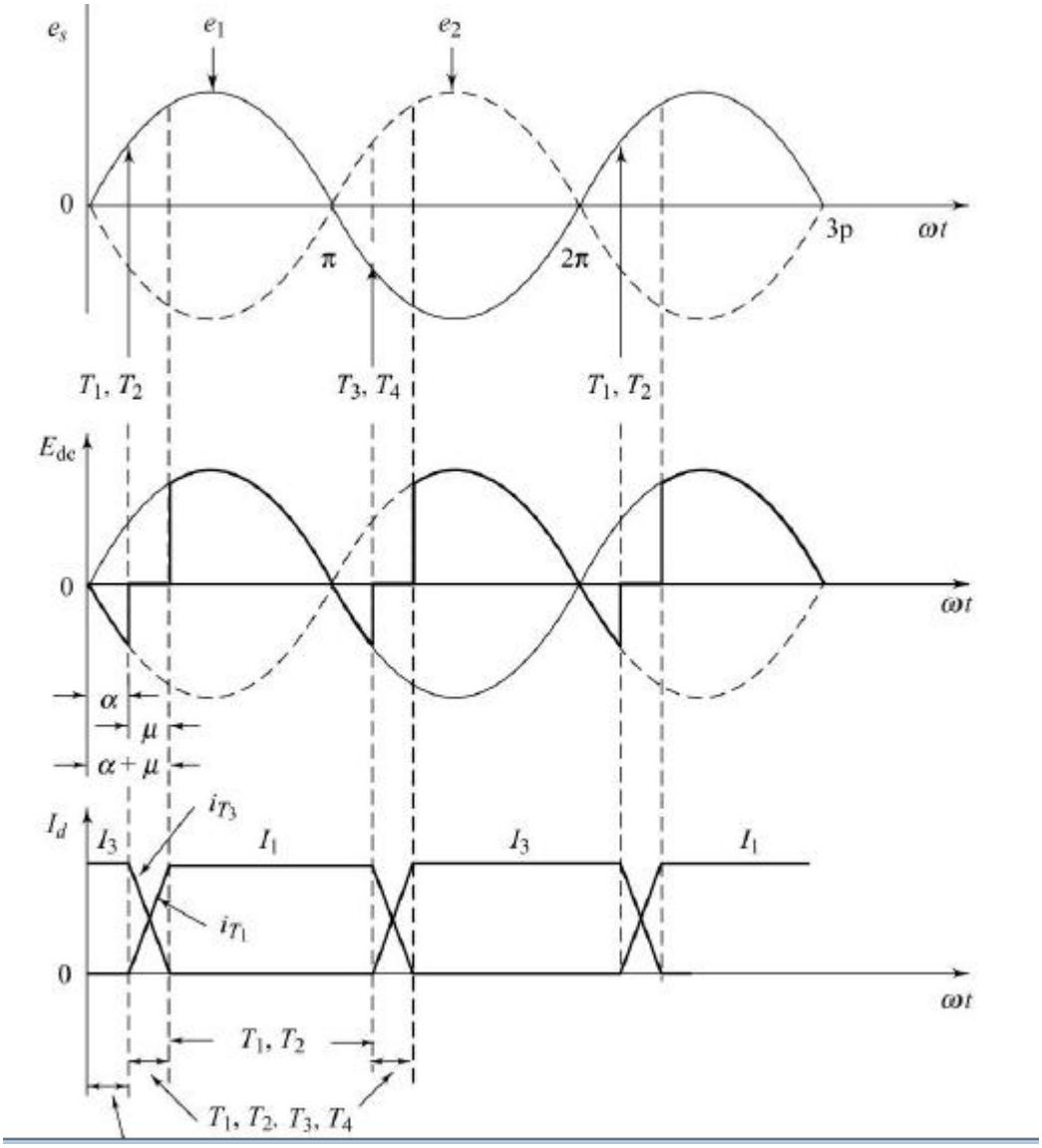
$= \frac{230\times\sqrt{2}}{\sqrt{\pi}}\left[(\pi-0) + \frac{1}{2}\sin 2(0)\right]^{1/2} = 325.269\,V$

OR

5 The commutation overlap is more predominant in full converters than semiconverters. The single-phase fully-controlled bridge converter is shown in Fig. 6.51(a). Ls is the source inductance. The load current is assumed constant. The a.c. supply may be represented by its Thevenin's equivalent circuit, each phase being a voltage source in series with its inductance. The major contributor to the supply impedance is the transformer leakage reactance. The equivalent circuit of fully controlled single phase converter is shown in Fig. 6.51(b). When the terminal L of the source voltage, es , is positive, then the current flows through the path. This is shown as e1, Ls, T1, T2, and load in Fig. 6.51(b). Similarly, when terminal N of source voltage, es , is positive, load current flows through the path N – T3 – load – T4 – Ls – L. This is shown as e2, Ls, T3, T4 and load in Fig. 6.51(b). The related circuit voltage and current waveforms are shown in Fig. 6.51(c).







When T1, T2 are triggered at a firing angle a, the commutation of already conducting thyristors T3, T4 begins. Because of the presence of source inductance

Ls, the current through outgoing thyristors T3, T4 decreases gradually to zero from its initial value of Id, whereas in case of incoming thyristors T1, T2, the current builds up gradually from zero to full value of load current, Id. During the commutation of T1, T2 and T3, T4, i.e. during the overlap angle m, KVL for the loop OPQRO of Fig. 6.51(b) ignoring SCR drops, gives

or $$e_1 - e_2 = L_S \left(\frac{\mathrm{d}_{iT_1}}{\mathrm{d}t} - \frac{\mathrm{d}_{i_3}}{\mathrm{d}t} \right)$$

But from Fig. 6.51(c), we have the relations

$$e_1 = E_m \sin \omega t \text{ and } e_2 = -E_m \sin \omega t.$$

Substituting in Eq. (6.62), we get

$$L_s \left(\frac{\mathrm{d}_{iT_1}}{\mathrm{d}t} - \frac{\mathrm{d}_{i_3}}{\mathrm{d}t} \right) = 2E_m \times \sin \omega t$$

Since the load current is assumed constant, we can write

$$i_{T_1} + i_{T_3} = I_d$$

$\therefore$ Differentiating Eq. (6.64), with respect to t.

$$\frac{\mathrm{d}_{iT_1}}{\mathrm{d}t} = \frac{\mathrm{d}_{iT_3}}{\mathrm{d}t}$$

Substitute Eq. (6.65) in Eq. (6.63), we get

$$L_s \left(2 \frac{\mathrm{d}_{iT_1}}{\mathrm{d}t} \right) = 2 E_m \cdot \sin \omega t$$

$$\therefore \quad \frac{\mathrm{d}_{iT_1}}{\mathrm{d}t} = \frac{E_m}{L_s} \sin \omega t$$

If the overlap angle is μ, then the current through thyristor pair T_1, T_2 builds u from zero to I_d during this interval.

Therefore, at $\omega t = \alpha, i_{T_1} = 0$ and at $\omega t = (\alpha + \mu), i_{T_1} = I_d$

$\therefore$ Therefore, from Eq. (6.66), we can write

$$\int_0^{I_d} d_{iT_1} = \frac{E_m}{L_s} \int_{\alpha/\omega}^{(\alpha+\mu)/\omega} \sin \omega t \, \mathrm{d}(\omega t)$$

$$\therefore \quad I_d = \frac{E_m}{\omega L_s} \left[\cos \alpha - \cos(\alpha + \mu) \right]$$

It can be observed from Fig. 6.51(c) that the output voltage is zero during th interval μ. There are two commutations in each cycle. Thus, the average outpu voltage is given by

$$E_{\mathrm{dc}} = \frac{E_m}{\pi} \int_{\alpha+\mu}^{\pi+\alpha} \sin \omega t \, \mathrm{d}(\omega t) = \frac{E_m}{\pi} \left[-\cos \omega t \right]_{\alpha+\mu}^{\pi+\alpha}$$

$$= \frac{E_m}{\pi} \left[\cos(\alpha + \mu) - \cos(\alpha + \pi) \right]$$

$$\therefore \quad E_{dc} = \frac{E_m}{\pi}[\cos\alpha + \cos(\alpha + \mu)] \qquad (6$$

Now, from Eq. (6.66), we have

$$\cos(\alpha + \mu) = \cos\alpha - \frac{\omega L_s}{E_m} I_d$$

Substituting this value of $\cos(\alpha + \mu)$ in Eq. (6.68), we get

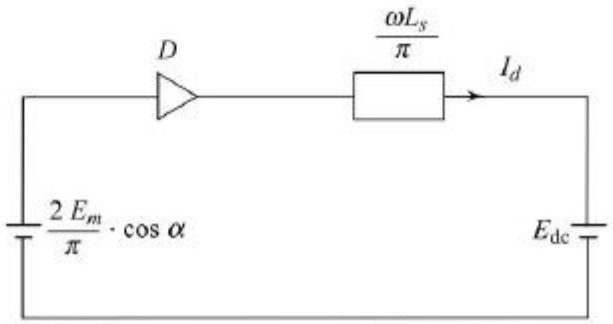
$$E_{dc} = \frac{E_m}{\pi}\left[\cos\alpha + \cos\alpha - \frac{\omega L_s}{E_m} I_d\right] \quad E_{dc} = \frac{2E_m}{\pi}\cos\alpha - \frac{\omega L_s}{E_m} I_d \qquad (6$$

Also, from Eq. (6.67), we have $\cos\alpha = \frac{\omega L_s}{E_m} I_d + \cos(\alpha + \mu)$

Substituting this value of $\cos\alpha$ in Eq. (6.68), we get

$$E_{dc} = \frac{2E_m}{\pi}\cos(\alpha + \mu) + \frac{\omega L_s}{\pi} I_d \qquad (6$$

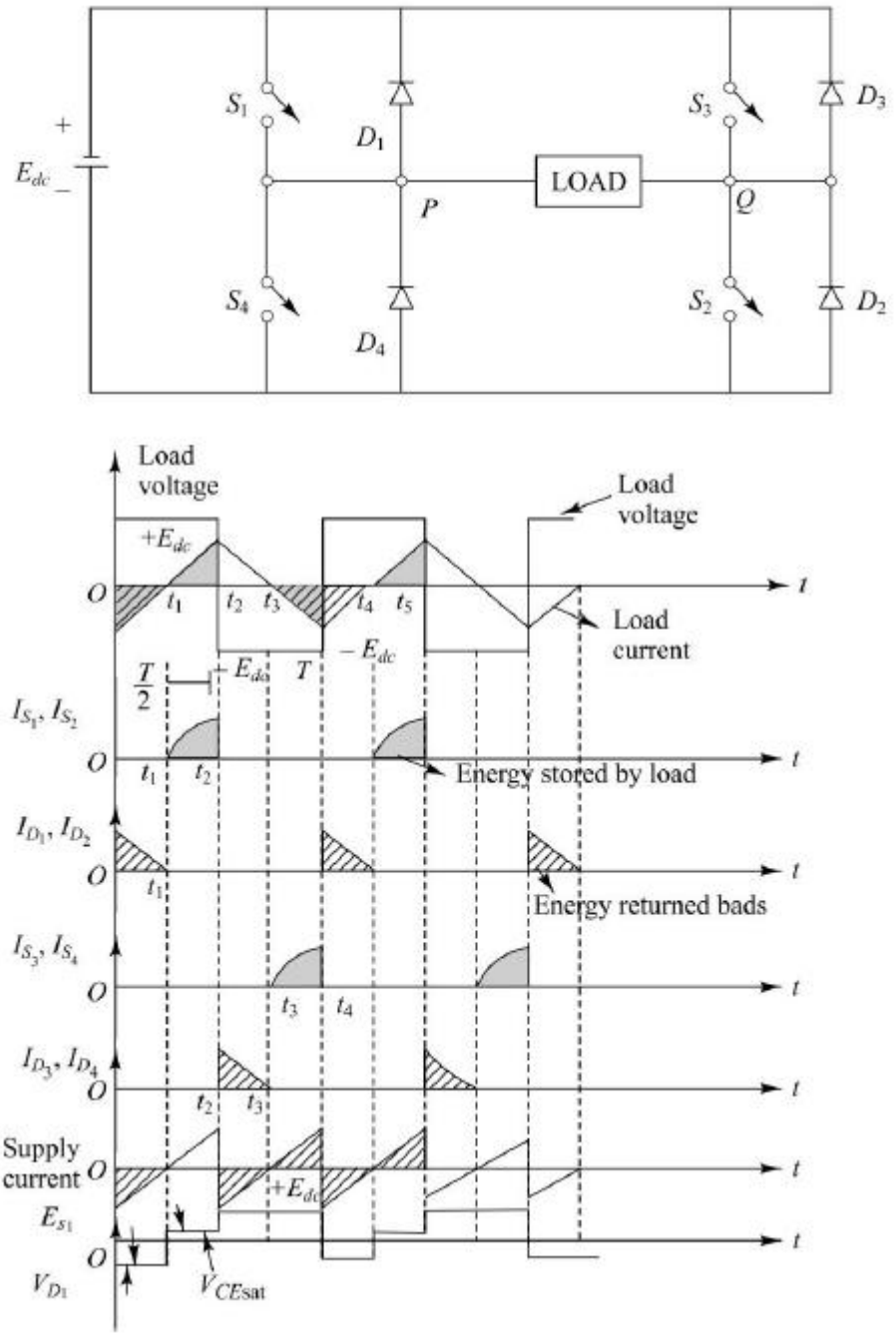
With the help of Eq. (6.69), a d.c. equivalent circuit for a two-pulse single-pl fully-controlled converter can be drawn, as shown in Fig. 6.51(d).



Diode D in Fig. 6.51(d) indicates that load current is unidirectional. This equivalent circuit shows that the effect of source inductance is to present an equivalent resistance of magnitude in series with interval voltage of rectifier . With the load current Id, the voltage drop is wLs Id . Hence it becomes clear that with source inductance, the output voltage of a converter is reduced by wLs Id value. The variation of output-voltage with output-current is shown in Fig. 6.51(e). From this Fig. 6.51(e), it is also clear that as load current Id (or source inductance) increases, the commutation interval or the overlap angle increases and as a consequence, the average output voltage decreases.

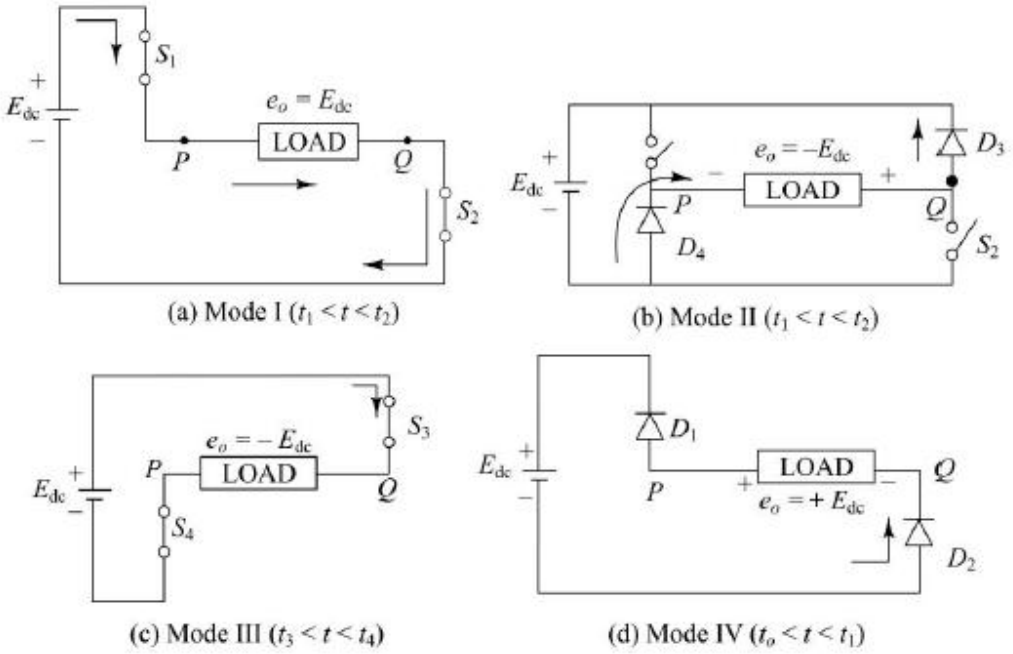
UNIT-III

6 a the power-diagram of the single-phase bridge inverter. The inverter uses two pairs of controlled switches (S1S2 and S3S4) and two pairs of diodes (D1D2 and D3D4). The devices of one pair operate simultaneously. In order to develop a positive voltage (+ E0) across the load, sw itches S1 and S2 are turned-on simultaneously whereas to have a negative voltage (–E0) across the load, we need to turn-on the switches S3 and S4. Diodes D1, D2, D3 and D4 are known as the feedback diodes.



(i) Mode-I (t1 < t < t2): At instant t1, the switch S1 and S2 are turned-on. Switches are assumed to be ideal switches. Point P gets connected to positive point of d.c. Source Edc through S1 and point Q gets connected to negative point of input supply. The output voltage, e0 = + Edc, Fig. 9.9(a). The load current starts increasing exponentially due to the inductive nature of the load. The instantaneous current through S1 and S2 is equal to the instantaneous load current. During this interval, energy is stored in inductive load. (ii) Mode-II (t2 < t < t3): Both the switches Q1 and Q2 are turned-off at instant t2. Due to the inductive nature of the load, the load current does not reduce to zero instantaneously. There is a self-induced voltage across the load which maintains the flow of current in the same-direction. The polarity of this voltage is exactly opposite to that in mode-1, The output voltage becomes –Edc, but the load current continues to flow in the same direction, through D3 and D4 as shown in

Fig. 9.9(b). Thus, in this mode, the stored energy in the load inductance is returned back to the source. Load current decreases exponentially and goes to 0 at instant t3 when all the energy stored in the load is returned back to supply. D3 and D4 are turned-off at t3.



(iii) Mode III (t3 < t < t4): Switches S3 and S4 are turned-on simultaneously at instant t3. Load voltage remains negative (– Edc) but the direction of load current will reverse. The current increases exponentially in the other direction and the load again stores the energy.
(iv) Mode IV (t0 < t < t1): Switches S3 and S4 are turned-off at instant t0 (or t4). The load inductance tries to maintain the load current in the same direction by
inducing the positive-load voltage. This will forward-bias the diodes D1 and D2. The load energy is returned back to the input dc supply. The load voltage becomes
e0 = +Edc but the load current remains negative and decreases exponentially towards 0. At t1 (or t5), the load current goes to zero and switches S1 and S2 can be turned-on again. The conduction period with a very highly inductive load, will be T/4 or 90° for all the switches as well as the diodes. The conduction period of switches will increase towards T/2 or 180° with increase in the load powerfactor.

$$E_{0rms} = \left[\frac{2}{T/2} \int_0^{T/2} E^2 \, dt \right]^{1/2} \quad \therefore \quad E_{0rms} = E_{dc}$$

(ii) The instantaneous output voltage can be expressed in fourier series as

$$e_{0(\omega t)} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4\,E_{dc}}{n\pi} \sin n\omega t \qquad (9.21)$$

The output voltage waveform contains only the odd harmonic components, i.e. 3, 5, 7, ... The even order harmonics are automatically cancelled.

(iii) For $n = 1$, Eq. (9.21) gives the rms value of the fundamental component

$$E_{1(rms)} = \frac{4\,E_{dc}}{\sqrt{2}\cdot\pi} = 0.9\,E_{dc} \qquad (9.22)$$

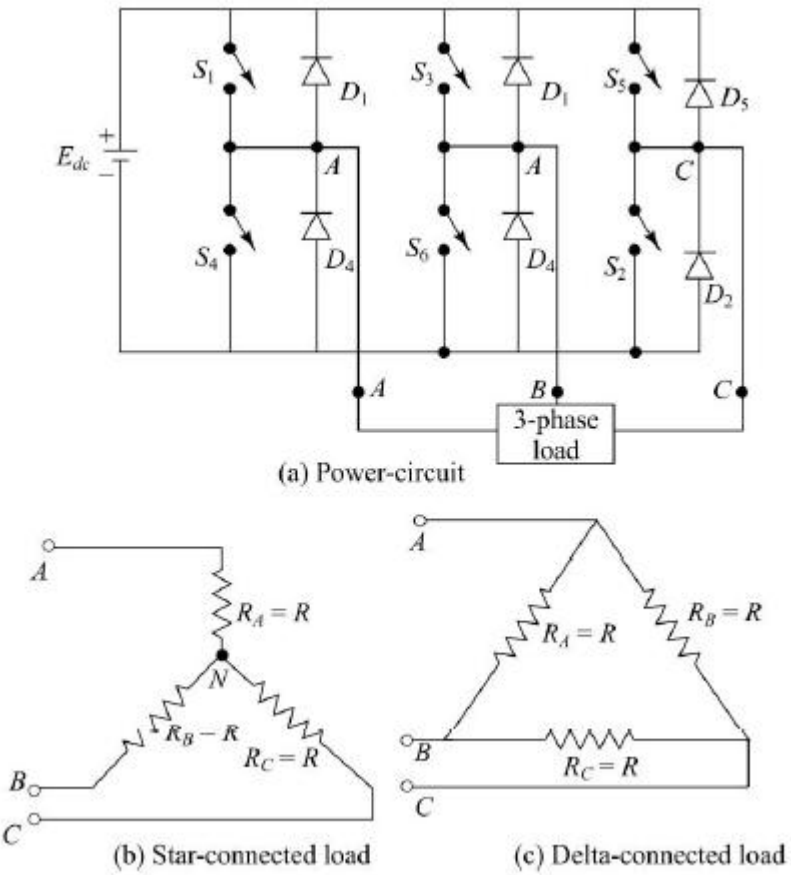
(iv) For RL load, the equation for the instantaneous current i_0 can be found using the Equation (9.21), as

$$i_{0(t)} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4\,E_{dc}}{n\pi\sqrt{R^2 + (n\,\omega L)^2}} \sin(n\omega t - \theta_n) \qquad (9.23)$$

In this equation, $Z_n = \sqrt{R^2 + (n\omega L)^2}$ is the impedance offered by the load to the n^{th} harmonic component and $\frac{4\,E_{dc}}{n\pi}$ is the peak amplitude of n^{th} harmonic voltage, and

$$\theta = \tan^{-1}(n\omega L/R) \qquad (9.24)$$

b) Three-phase inverters are used for high-power applications such as ac motor drives, induction heating, uninterruptive power supplies. A three-phase inverter circuit changes DC input voltage to a three-phase variable frequency, variablevoltage output. The input DC voltage can be from a DC source or a rectified AC voltage. A three-phase bridge inverter can be constructed by combining threesingle- phase half-bridge inverters. Figure 9.24 shows the basis circuit of three-



phase bridge inverter. As shown, it consists of six power-switches with six associated freewheeling diodes. The switches are opened and closed periodically in the proper sequence to produce the desired output waveform. The rate of switching determines the output frequency of the inverter.

Basically, there are two possible schemes of gating the devices. In one scheme, each device (switch) conducts for 180° and in the other scheme, each device conducts for 120°. But in both these schemes, gating signals are applied and removed at 60° intervals of the output voltage waveform. These modes of device conduction are described in the following subsection: 180: In this control scheme, each switch conducts for a period of 180° or half-cycle electrical. Switches are triggered in sequence of their numbers with an interval of 60°. At a time, three switches (one from each leg) conduct. Thus, two switches of the same leg are prevented from conducting simultaneously. One complete cycle is divided into six modes, each of 60° intervals. The operation of the circuit can be understood from the waveforms shown in Fig. 9.25 and the operation Table 9.1.

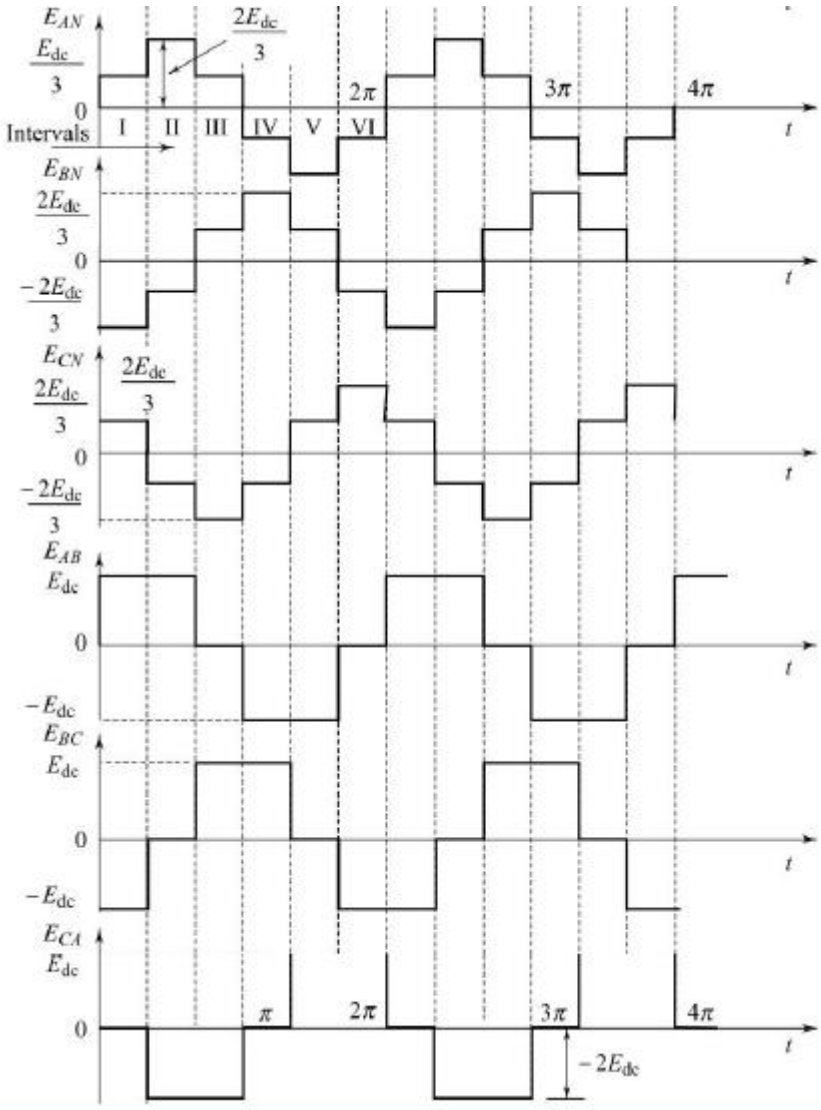
Switch pair in each leg, i.e. S1, S4, S3 S6, and S5, S2 are turned-on with a time interval of 180°. It means that switch S1 conducts for 180° and switch S4 for the next 180° of a cycle. Switches, in the upper group, i.e. S1, S3, S5 conduct at an interval of 120°. It means that if S1 is fired at 0°, then—S3 must be triggered at 120° and S5 at 240°. Same is true for lower group of switches. On the basis of this gating scheme, Table 9.1 is prepared.

The following points can be noted from the wave forms (Fig. 9.25) and the operating Table 9.1,

(i) Each switch conducts for a period of 180°.

(ii) Switches are triggered in the sequence 1, 2, 3, 4, 5, and 6.

(iii) Phase shift between triggering the two adjacent switches is 60°.
(iv) From table, it is observed that in every step of 60° duration, only three switches are conducting—two from upper group and one from the lower group and vice-versa.



(v) The output voltage waveforms (E_{AB}, E_{BC}, E_{CA}) are quasi-square-wave with a peak-value of E_{dc}. The three-line voltages are mutually phase-shifted by 120°.

(vi) The three-phase-voltages E_{AN}, E_{BN}, and E_{CN} are six-step saves, with step heights $\frac{E_{dc}}{3}$ and $\frac{2}{3}E_{dc}$.

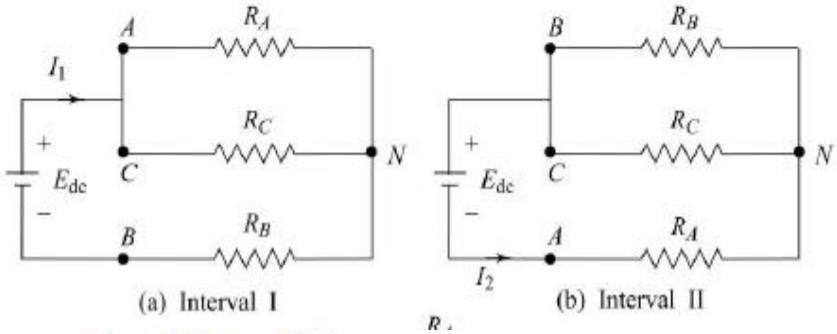
(vii) Line voltage E_{AB} is leading the phase-voltage E_{AN} by 30°.

In Fig. 9.25, phase voltages E_{AN}, E_{BN} and E_{CN} have also been drawn for star-connected resistive load. For a star-connected load, the line-to-neutral voltages must be determined to find the line or phase currents. There are three modes of operation in a half-cycle and the equivalent circuits are shown in Fig. 9.26 for a star-connected load.

From Figs (9.25) and (9.26), it is observed that

(i) During interval I for $0 \le \omega t < \pi/3$,

$$Req = R_B + (R_A \,||\, R_C)$$



(a) Interval I (b) Interval II

$$E_{AB} = \sum_{n=1,3,5...}^{\infty} \frac{4E_{dc}}{n\pi} \cos\frac{n\pi}{6} \sin n(\omega t + \pi/6)$$

$$E_{Ln} = \frac{4E_{dc}}{\sqrt{2}\, n\pi} \cos\frac{n\pi}{6}$$

which, for $n = 1$, gives the fundamental line voltage.

$$E_{L_1} = \frac{4E_{dc} \cos 30}{\sqrt{2}\ \pi} = 0.7797\ E_{dc}$$

The RMS value of line-to neutral voltages can be found from the line

$$E_p = \frac{E_L}{\sqrt{3}} = \frac{\sqrt{2}\ E_{dc}}{3} = 0.4714\ E_{dc}$$

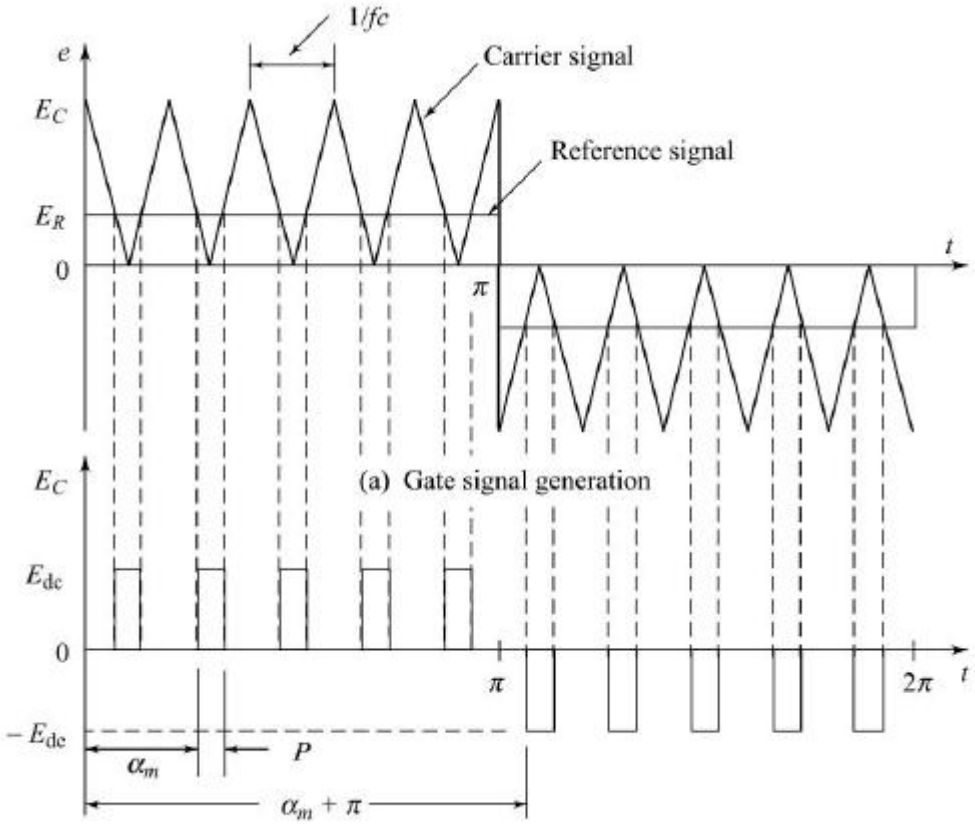
OR

7 a In this method of pulse-width modulation, the harmonic content can be reduced using several pulses in each half-cycle of output voltage. By comparing a reference signal with a triangular carrier wave, the gating signals are generated for turningon and turning-off of a thyristor, as shown in Fig. The carrier frequency, fc, determines the number of pulses per half-cycle, m, whereas the frequency of reference signal sets the output frequency, fo. The modulation index controls the output voltage. This type of modulation is also known as symmetrical pulse

width modulation (SPWM). The number of pulses Np per half-cycle is found from the expression

$$N_p = \frac{f_c}{2f_0} = \frac{m_f}{2}$$

where $m_f = \frac{f_c}{f_0}$ is the frequency modulation ratio. The variation of modulation index (M) from 0 to 1 varies the pulse width from 0 to π/N_P and the output voltage from 0 to $E_{\text{d.c.}}$. For SPWM, the output voltage for single-phase bridge inverters is shown in Fig. 9.15(b).



(b) Output voltage

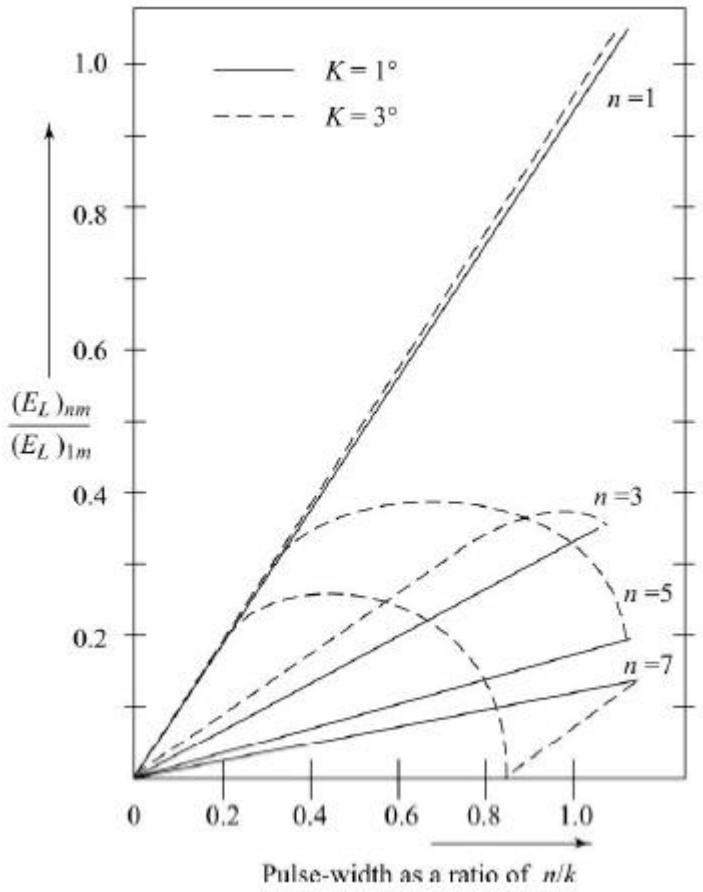
If P is the width of each pulse, the RMS output voltage can be obtained from the following expression:

$$E_{L(\text{rms})} = \left[\frac{2N_p}{2\pi} \int_{(\pi/N_p - P)/2}^{(\pi/N_p + P)/2} E_{\text{dc}}^2 \, \text{d}(\omega L) \right]^{1/2} = E_{\text{dc}} \sqrt{\frac{N_p \, . P}{\pi}}$$

The general expression for various harmonics in the output voltage is obtained by deriving an expression for a general pair of pulses, such that the positive pulse of duration P starts at $\omega t = \alpha$ and the negative one of the same width starts at $\omega t = \pi + \alpha$. This is shown in Fig. 9.15(b). The effects of all pulses can be combined together to obtain the effective output voltage. Thus for this pair of pulses,

$$A_{nm} = \frac{2E_{\text{dc}}}{\pi} \int_{\alpha_{m-p/2}}^{\alpha_{m+p/2}} \sin n \, \omega t \, \text{d}(\omega t)$$

$$= \frac{2E_{\text{dc}}}{2\pi} \left[\cos n \, (\alpha m + p/2) - \cos n \, (\alpha_m - p/2) \right]$$



adjacent pulses, i.e. (P/p/ k). As the number of pulses per half-cycle (i.e. k) is increased, the considerable reduction in lower order harmonics is achieved, as shown in Fig. 9.16. For example, with K = 10, substantial reduction in third, fifth and seventh harmonics is achieved in the complete range of the output voltage.
With larger values of Np, the amplitudes of lower order harmonics would be

lower, but the amplitudes of some higher order harmonics would increase. However, such higher order harmonics produce negligible ripple or can easily be filtered out. With this method, since voltage control is achieved with a simultaneous reduction of lower order harmonics, this scheme is comparatively advantageous over single-pulse modulation. However, due to larger number of pulses per halfcycle, frequent turning-on and turning-off of thyristors is required which increases the switching losses. Also, for this scheme inverter-grade thyristors are required which are costly.

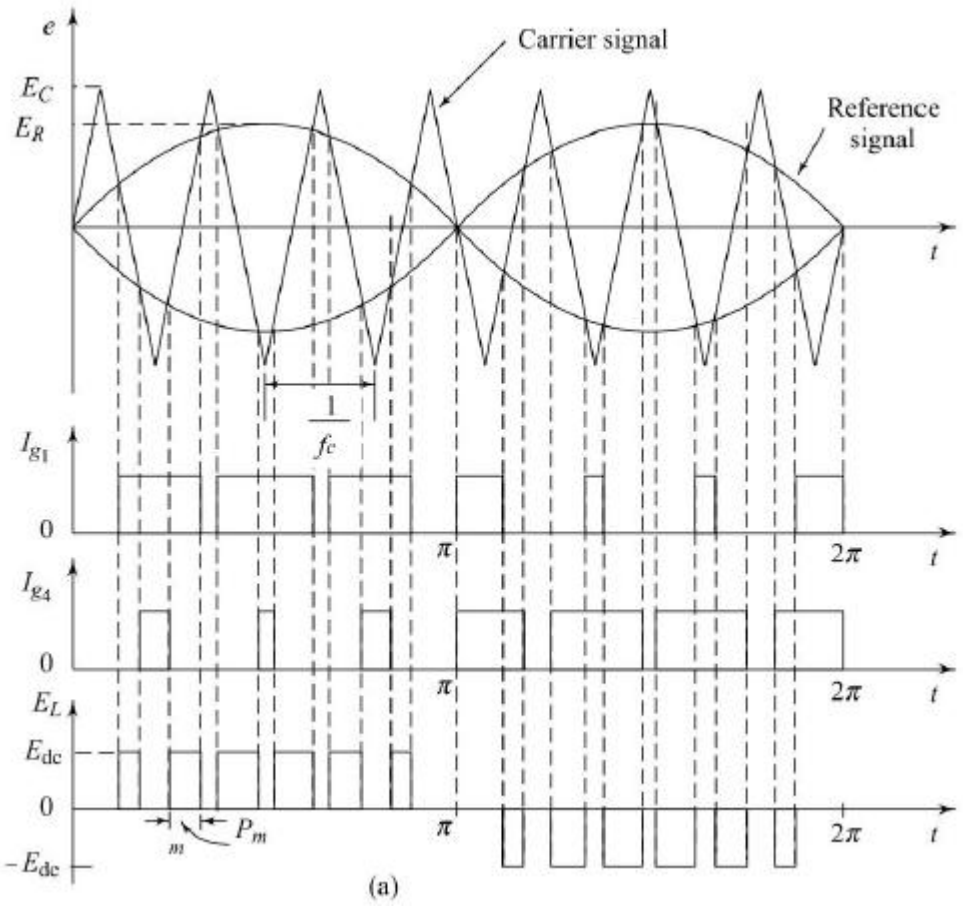
b) In this method of modulation, several pulses per half-cycle are used as in the case of multiple pulse width modulation. Instead of maintaining the width of all pulses the same as in the case of multiple-pulse modulation, the width of each pulse is varied proportional to the amplitude of a sine-wave evaluated at the centre of the same pulse. By comparing a sinusoidal reference signal with a triangular carrier wave of frequency, fc, the gating signals are generated, as shown in Fig. 9.17(a). The frequency of reference signal, fr, determine the inverter output frequency, fo, and its peak amplitude, Er, controls the modulation index, M, and then in turn the RMS output voltage, EL. The number of pulses per halfcycle depends on the carrier frequency. Within the constraint that two thyristors of the same arm (T1, T4) cannot conduct at the sa me time, the instantaneous output voltage is shown in Fig. 9.17(a). The same gating signals can be generated using unidirectional triangular carrier-wave as shown in Fig. 9.17(b).

By varying the modulation index M, the RMS output voltage can be varied. It can be observed that the area of each pulse corresponds approximately to the area under the sine-wave between the adjacent midpoints of OFF periods on the gating signals. If Pm is the width of the mth pulse, Eq. (9.39) can be extended to find the rms output voltage

$$E_L = E_{\text{dc}} \left(\sum_{m=1}^{N_p} \frac{P_m}{\pi} \right)^{1/2}$$

Harmonic analysis of the output modulated voltage wave reveals that SPWM has the following important features:

(i) For modulation index less than one, the largest harmonic amplitudes in the output voltage are associated with harmonics of order fc / fr ± 1 or 2Np ± 1, where Np is the number of pulses per half-cycle. Thus, by increasing the number of pulses per half-cycle, the order of dominant



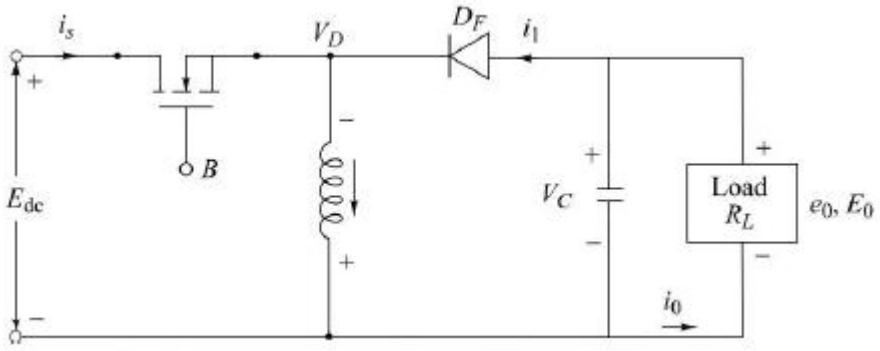
(a)

harmonic frequency can be raised, which can then be filtered out easily. For Np = 5, harmonics of the order of 9 and 11 become significant in the output voltage. It may be noted that the highest order of significant harmonic of modulated voltage-wave is centred around the carrier frequency, fc.

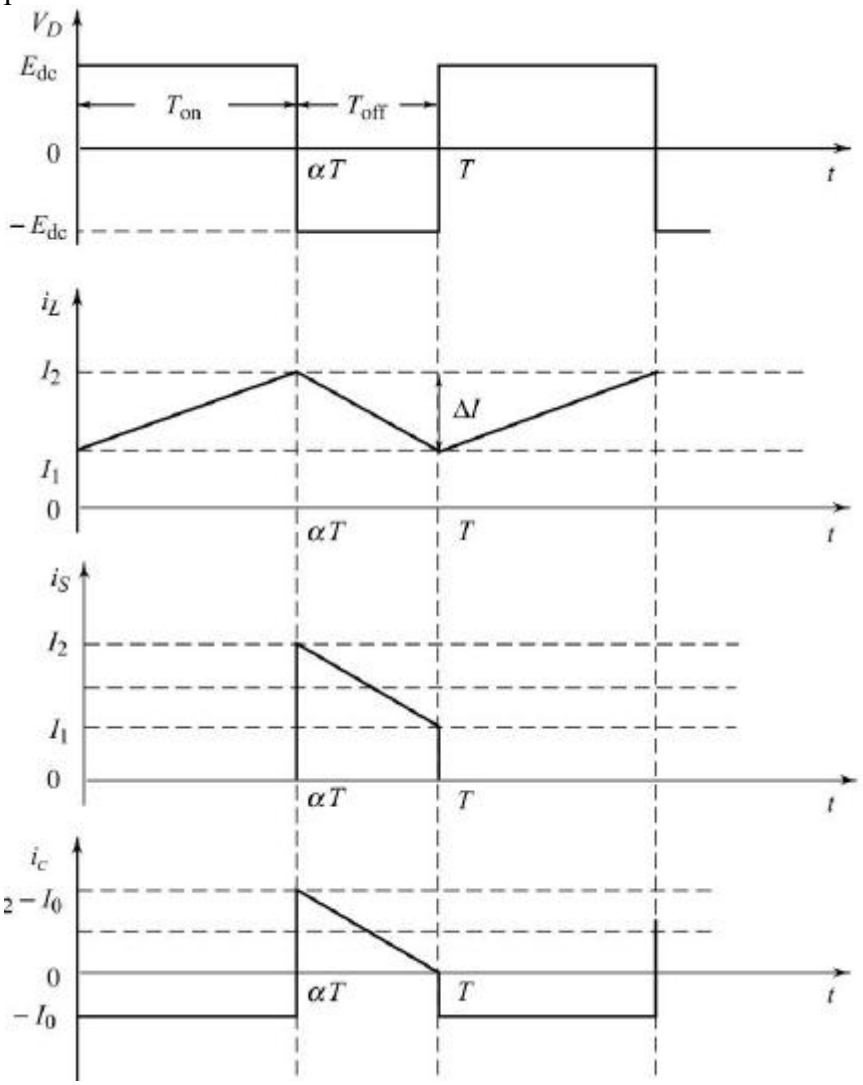
(ii) For modulation index greater than one, lower order harmonics appear since for modulation index greater than one, pulse width is no longer a sinusoidal function of the angular position of the pulse.

UNIT-IV

8 a the circuit diagram of a buck-boost converter. As shown, a buck-boost converter is nothing but cascade connection of the two basic converters: the step-down converter and the step-up converter. The main application of such a converter is in regulated d.c. power supplies, where a negative polarity output may be desired with respect to the common terminal of the input voltage, and the output voltage can be either higher or lower than the input voltage. For a continuous load current, the waveforms for the steady-state voltage and currents are shown in Fig



When the power MOSFET is switched ON, the supply current flows through the path Edc + – T1 – L – Edc– . Hence, inductor L stores the energy during the Ton period.



decrease and as a result, the polarity of the emf induced in L is reversed as shown in Fig. 8.45(a). Thus, the inductance energy discharges in the load through the path L_+ – Load – D – L_-.

During time T_{on}, by assuming that the inductor current rises linearly from I_1 to I_2, we can write, $E_{dc} = L \cdot \dfrac{I_2 - I_1}{T_{on}} = L \cdot \dfrac{\Delta I}{T_{on}}$

or, $$T_{on} = \frac{\Delta I L}{E_{dc}}$$

Now, during time T_{off}, the inductor current falls linearly from I_2 to I_1, therefore, we can write

$$E_0 = -L \cdot \frac{\Delta I}{T_{off}}$$

or $$T_{off} = \frac{-\Delta I \cdot L}{E_0}$$

where the peak-to-peak ripple current of inductor L is given by

$$\Delta I = I_2 - I_1$$

From Eqs (8.161) and (8.163), we can write,

$$\Delta I = \frac{E_{dc} \cdot T_{on}}{L} = \frac{-E_0 \cdot T_{off}}{L}$$

or $$E_0 = -E_{dc} \cdot \frac{T_{on}}{T_{off}} = -E_{dc} \cdot \frac{T_{on}/T}{T_{off}/T} = \frac{-E_{dc} \cdot \alpha}{(T - T_{on})/T}$$

or $$E_0 = -E_{dc} \cdot \frac{\alpha}{(1 - \alpha)}$$

b)

(8) (b) $f = 4 \times 10^3 \Rightarrow \frac{1}{f} = T = 2.5 \times 10^{-4}$

$V_s = 440$

$V_0 = 260$

$V_0 = V_s \cdot \frac{T_{on}}{T} \Rightarrow 440 \times \frac{T_{on}}{\left(\frac{1}{4\times10^3}\right)} = 260$

i) $T_{on} = 1.477 \times 10^{-4}$

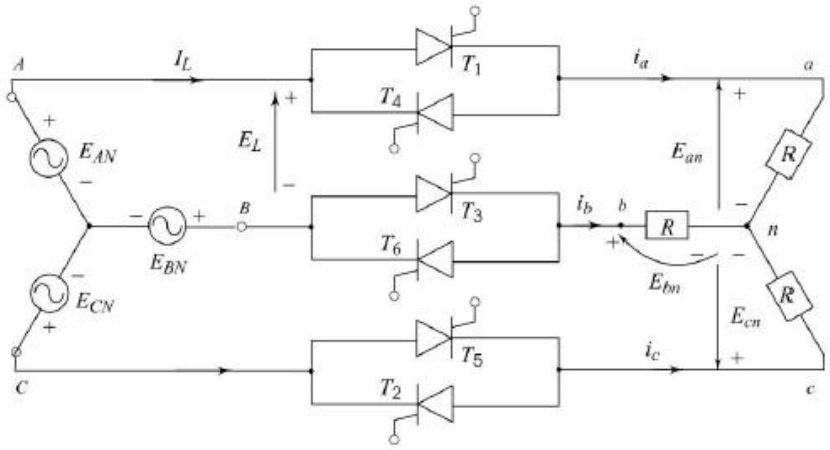
ii) $T_b = 1.023$

iii) $\delta = \frac{1.477}{2.5} = 0.59 < 1$

OR

9 a There are many three-phase versions of a.c. thyristor controllers and Fig. 11.15 shows a selection of them. They all operate in slightly different ways. The following are the important points of comparison between the circu its of Fig.1. In circuits C and D, the individual phase controllers control their own loads independently of the other. They can, therefore, be studied as three single-phase controllers.

In other circuits, the individual phase controllers affect the other phase loads also and they have to be studied as complete three-phase circuits. 3. The peak voltages occur across thyristors at or near to the fully OFF state. In the case of circuits D, E and F the maximum thyristor voltage is

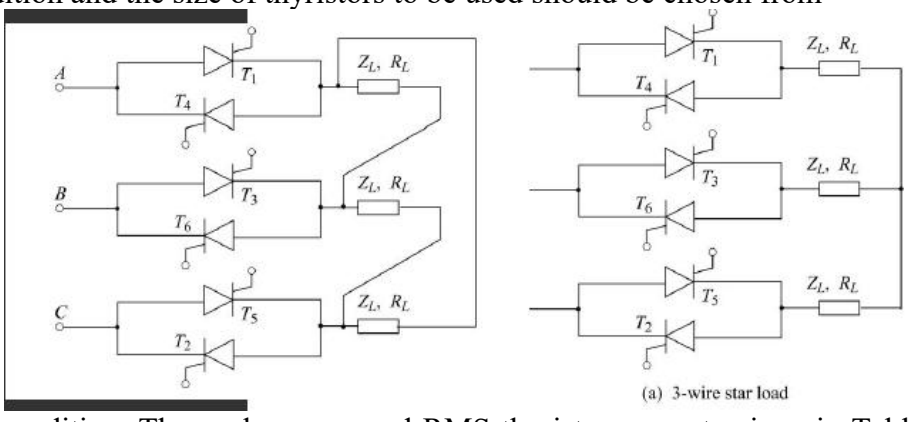


the peak of the line voltage, whereas in circuit C it is the peak of the phase voltage; in circuits A and B the maximum thyristor voltage will be somewhere between the peak of the phase and line voltage depending on the leakage current of the thyristors, the method of firing, and the presence of voltage-sharing resistors across the thyristors.

4. All these circuits can be used under phase control.

5. The range of phase angle required to achieve full output range from zero to maximum varies between the circuits and these are given.

6. The maximum current flow in the thyristors is decided from the fully on condition and the size of thyristors to be used should be chosen from

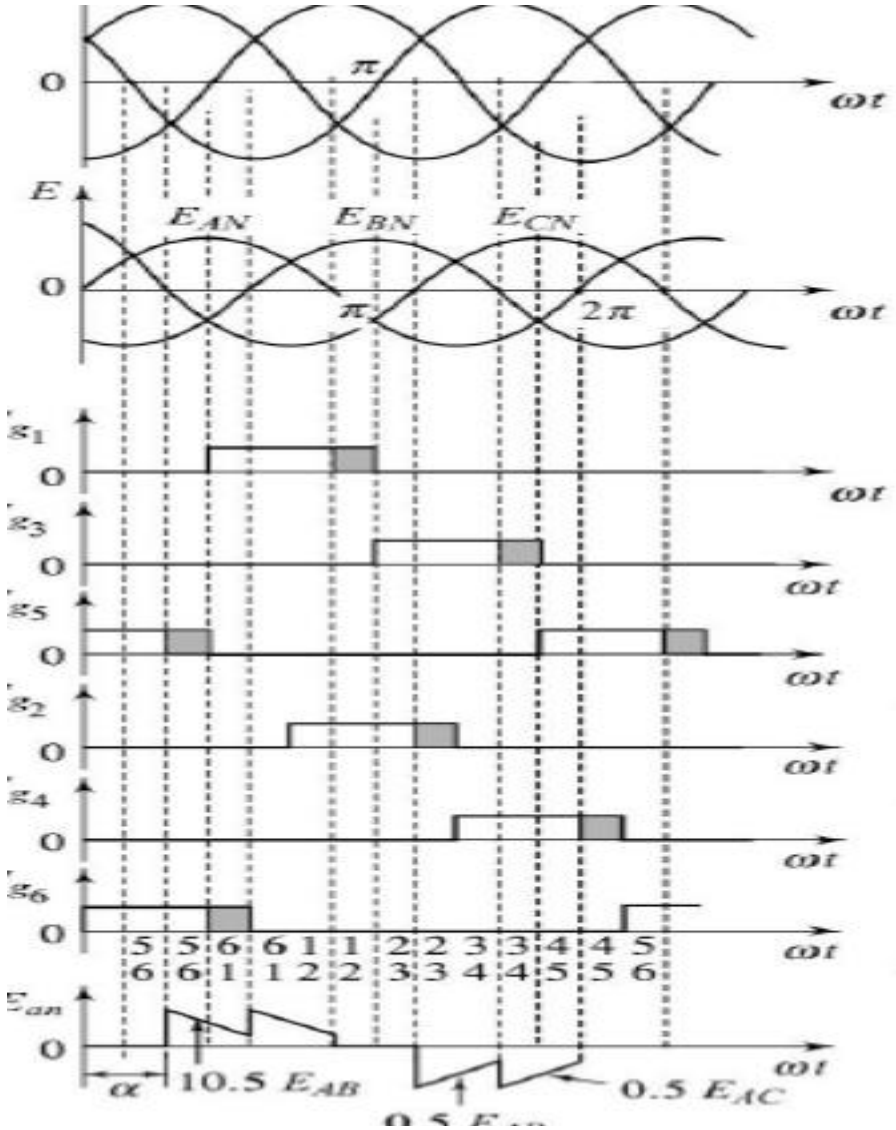


(a) 3-wire star load

this condition. The peak, mean, and RMS thyristor currents given in Table 11.1 are related to the RMS a.c. input current which should be found by applying the full supply voltage to the load-circuit impedances.

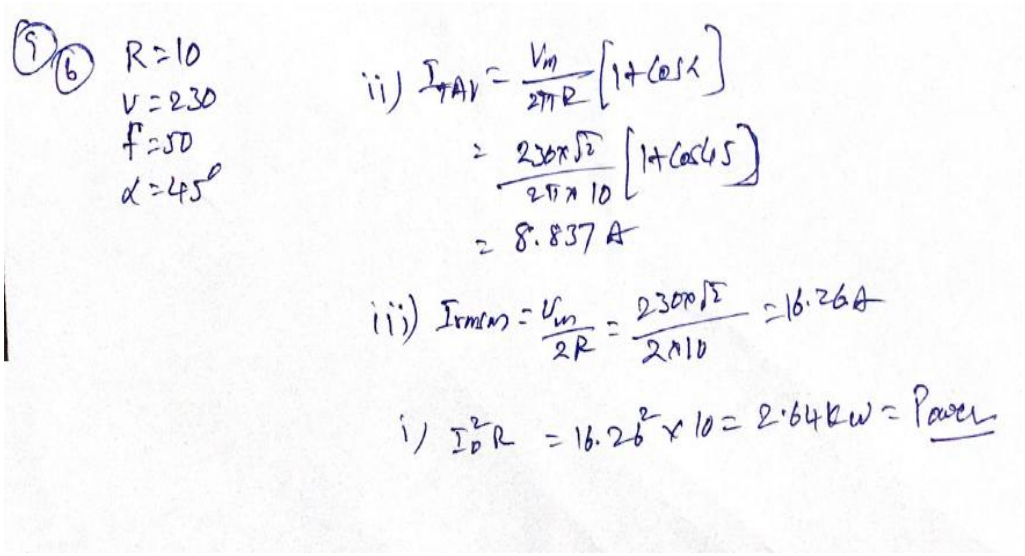
7. Although only three thyristors are required in circuit F, they each have to carry a higher current than the other circuits. Under fully conduction conditions, the

current flows in each thyristor for 240 degrees in every cycle.



$$E_0 = \sqrt{6}E_s\left\{\frac{2}{\pi}\left[\int_{\pi/2-\pi/3+\alpha}^{\pi}\frac{\sin^2\omega t}{4}\,\mathrm{d}(\omega t)+\int_{\pi/2-\pi/3+\alpha}^{\pi}\frac{\sin^2\omega t}{4}\,\mathrm{d}(\omega t)\right]\right\}^{1/2}$$

b)



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