SCHEME OF EVALUATION

II/IV B.Tech., II-Sem. Regular Degree Examination
Electronics and Communication Engineering

Microprocessor &Microcontroller

(20EC405)

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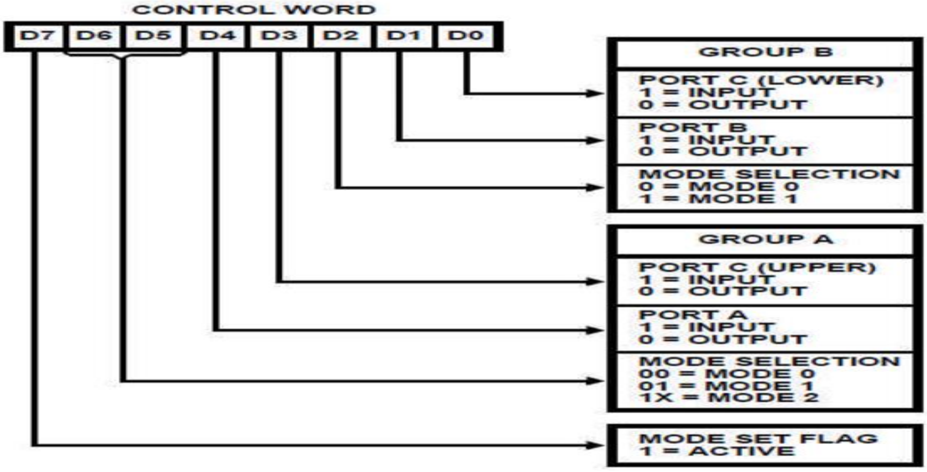
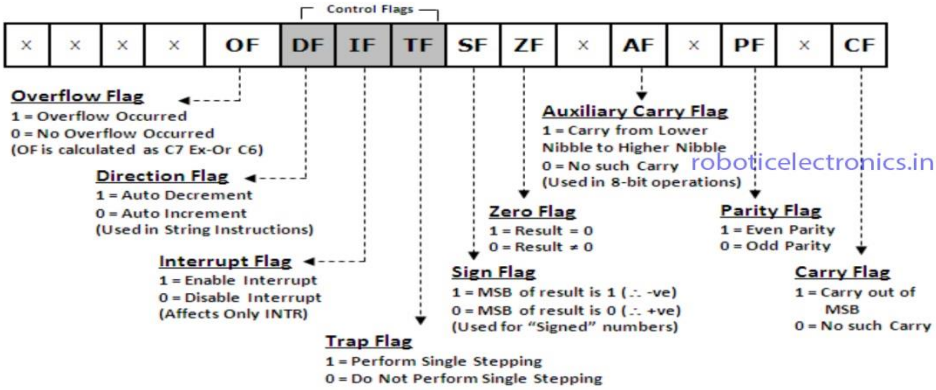
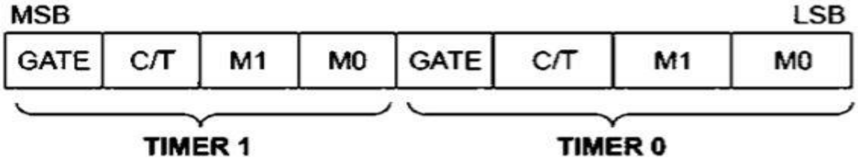
II/IV B.Tech (Regular\Supplementary) DEGREE EXAMINATION

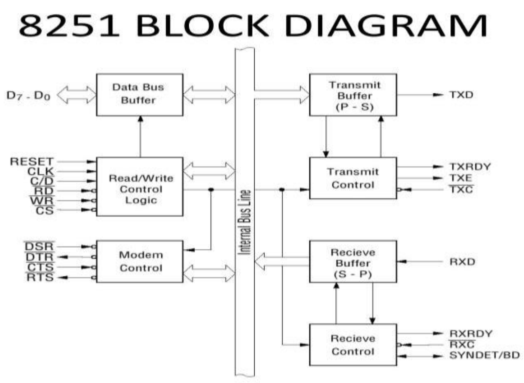
July/August,2023	**Electronics & Communication Engineering**
Fourth Semester	**Microprocessor &Microcontroller (20EC405)**

Scheme of Evaluation

Q. No.			CO	BL	Marks
1	a)	**Control Word Format of 8255A:**  CONTROL WORD D7 D6 D5 D4 D3 D2 D1 D0 GROUP B PORT C (LOWER) 1 = INPUT 0 = OUTPUT PORT B 1 = INPUT 0 = OUTPUT MODE SELECTION 0 = MODE 0 1 = MODE 1 GROUP A PORT C (UPPER) 1 = INPUT 0 = OUTPUT PORT A 1 = INPUT 0 = OUTPUT MODE SELECTION 00 = MODE 0 01 = MODE 1 1X = MODE 2 MODE SET FLAG 1 = ACTIVE	CO1	L2	1M
	b)	**Flag Register Format of 8086:**  Control Flags × × × × OF DF IF TF SF ZF × AF × PF × CF Overflow Flag 1 = Overflow Occurred 0 = No Overflow Occurred (OF is calculated as C7 Ex-Or C6) Direction Flag 1 = Auto Decrement 0 = Auto Increment (Used in String Instructions) Interrupt Flag 1 = Enable Interrupt 0 = Disable Interrupt (Affects Only INTR) Trap Flag 1 = Perform Single Stepping 0 = Do Not Perform Single Stepping Auxiliary Carry Flag 1 = Carry from Lower Nibble to Higher Nibble 0 = No such Carry (Used in 8-bit operations) roboticelectronics.in Zero Flag 1 = Result = 0 0 = Result ≠ 0 Parity Flag 1 = Even Parity 0 = Odd Parity Sign Flag 1 = MSB of result is 1 (∴ -ve) 0 = MSB of result is 0 (∴ +ve) (Used for "Signed" numbers) Carry Flag 1 = Carry out of MSB 0 = No such Carry	CO2	L2	1M
	c)	ARM stands for Advanced RISC (Reduced Instruction Set Computer) Machine	CO1	L2	1M
	d)	P.A(20 bit) =Seg.Base Address(16 Bit) *10H + offset (16 Bit) Therefore, P.A(20 bit) =4000H *10H + 40H = 40040H	CO2	L6	1M
	e)	**Assume:** This assembler directives helps to link the name of the logical segment used for a specified segment. **End:** The assembler indicates the end of the program module to the assembler. It is the last line of the main routine.	CO1	L2	0.5M 0.5M
	f)	**DD:** Define Double Word This Assembler directive is used to declare a variable of type double word ((32-bit) or to reserve a memory location which can be accessed as a double	CO1	L2	1M

		word.			
	g)	PUSH and POP instructions updates Stack Pointer by subtracting and adding 2 respectively.	CO1	L1	1M
	h)	**DMA:** Direct Memory Access is fastest scheme of data transfer between memory/input output devices without involvement of CPU	CO3	L2	1M
	i)	**Hardware interrupt pins of 8086:** NMI (Non Maskable Interrupt) INTR (Interrupt Pin) INTA^ (Interrupt Acknowledgement Pin only available in minimum mode)	CO1	L2	1M
	j)	**8051 Ports:** P0,P1,P2,P3 – 4 No. of 8-bit parallel ports and 1 serial port (TX/RX)	CO4	L1	1M
	k)	**TMOD Register:** decides the mode of operation of T0 & T1 timers.  MSB LSB GATE C/T M1 M0 GATE C/T M1 M0 TIMER 1 TIMER 0	CO1	L2	1M
	l)	**SBUF Register:** 8-bit register used for serial communication. It is filled with value to be transmitted serially on TXD pin and it also holds the value received serially on RXD pin.	CO2	L2	1M
	m)	When an interrupt occurs automatically type number is calculated and Program Counter is diverted to Interrupt Vector Table (IVT) for updating the location of special routine called Interrupt Service Routine (ISR).	CO2	L1	1M
	n)	**Timers in 8051:** 8051 contains two 16-bit timers namely T0 and T1. Every timer is combination of two 8-bit SFRs namely TL0,TH0,TL1,TH1.	CO2	L1	1M
		<u>Unit-I</u>			
2	a)	**Architecture of 8086 :** two sub-sections namely BIU and EU Block diagram Function of each block	CO1	L4	1 M 3 M 3 M
	b)	**Instructions of 8086:** **XLAT:** The contents of AL is replaced with a value from the look up table whose base address is DS:BX. The value in AL is treated as offset to browse through the loop up table. **TEST:** It computes bit wise and of two operands without effecting them (the result is discarded). Instead, it changes SF,ZF & PF. **STOSB:** It is a string instruction used to store a string in AL to ES:DI. It automatically updates DI by 1 after storing. It can be used with REP prefix. **ESC:** the instruction with this prefix in memory is meant for execution by the co-processor.	CO1	L2	2 M 2 M 2 M 1 M
		(OR)			
3	a)	**8086 Addressing modes:** (Any 5 with examples) 1. Immediate eg: MOV AX,4004H 2. Register direct eg: MOV AL,BL 3. Direct eg: MOV AX,[4004H] 4. Register indirect eg: MOV AL,[SI] 5. Self/Implicit eg: CLC 6. Relative eg: JNZ 4004H	CO1	L2	7M

	b)	**Elements of Microprocessor Unit:** 1. ALU 2. Registers: General purpose and Special purpose 3. Control Unit 4. I/O units/Buses Explanation of function of each unit	CO1	L1	3 M 4 M
		Unit-II			
4	a)	**DIV instruction:** 86 supports only unmatched divisions i.e. 32/16 or 16/8 1. DIV BX : DX:AX/BX with AX holding quotient and DX holding remainder. 2. DIV BL : AX/BL with AL holding quotient and AH holding remainder **ALP for 8-bit Divison:** using 16/8 MOV SI,4000H MOV AH,00H MOV AL, NUMERATOR MOV BL, DENONOMINATOR DIV BL MOV [SI],AX	CO2	L3	1M 2 M 4 M
	b)	**Interrupt groups/Types:8086:** List of any 5 types Groups with examples – identification of type 1. Hardware interrupts: NMI, INTR 2. Software interrupts: int 0 to int 255 3. Maskable interrupts: all software interrupts 4.Un-maskable interrupts: NMI 5. Vectored interrupts: int 0 to int 255 6. Non-vectored interrupts: INTR	CO2	L1	2M 5 M
		(OR)			
5	a)	**Assembly Language Program development tools**: List 1. Editor 2. Assembler 3. Linker 4. Locator 5.Debugger / Emulator Function of each tool-details	CO2	L1	3 M 4 M
	b)	**Procedure VS Macro**: for modular programming **Procedure:** • Accessed by using CALL and RET instructions • Used for encapsulating large no. of instructions • Involves latencies • Passing paramters: by reg, stack **Macro** • Accessed by name of the macro • Used for less no. of instructions • Passed parameters using dummy variables • Macro expansion gives inline code	CO1	L5	1 M 3 M 3 M
		Unit-III			

6	a)	**Modes of 8086 operation:** Pin no.33 MN/MX^ decides MIN (single processor) & MAX (multi-processor). Pins 24 to 31 has different meanings in different modes. **Any 3 differences** **MIN mode:** - Uni processor mode - 8237 use HOLD, HLDA pins - M/IO^,RD^ & WR^ are control signals **MAX mode:** - Multi processor mode. - Control signals generated by external bus controller using S2^,S1^,S0^ - RQ/GT^ are bus request signals	CO2	L2	1M 3 M 3 M
	b)	**Concept of DMA:** Direct Memory Access is fastest scheme of data transfer between memory/input output devices without involvement of CPU **Block diagram** explaining DMA sequence of steps activating HOLD, HLDA and in between leasing of busses between memory/peripheral to memory/peripheral device requesting them using 8237/8257. **Operation** - Explanation	CO1	L2	2 M 2 M 3 M
(OR)					
7	a)	 8251 BLOCK DIAGRAM D7 - D0 Data Bus Buffer RESET CLK C/D RD WR CS Read/Write Control Logic DSR DTR CTS RTS Modem Control Internal Bus Line Transmit Buffer (P - S) TXD Transmit Control TXRDY TXE TXC Recieve Buffer (S - P) RXD Recieve Control RXRDY RXC SYNDET/BD Explanation of function of each block	CO1	L2	4 M 3 M
	b)	**Diagram:** Key placement at row column intersections of a matrix – eg: hexa key pad using PPI -8255A **Routines in keypad interfacing:** 1. Key press detection –pulling columns & reading rows. 2. Key de-bouncing routine 3.Key identification – obtaining row VS column information of the key 4. Key encoding routine. Importance of each routine	CO2	L2	3 M 2 M 2 M
Unit-IV					
8	a)	TMOD & TCON formats – timer 1 usage in mode-1(16 bit timer mode) **Initial value calculations:**	CO2	L2	1 M

		Fosc=22 MHz, f=fosc/12= 22/12 MHz =1.83 MHz i.e. TMachine cycle=0.546 micro seconds f=100KHz T=1/f = 0.01 Milli seconds where T= Ton+Toff Here considering symmetric square wave Ton =Toff = T/2 = 0.005 Milli seconds d=no. of 0.546 micro seconds to make up 0.005 milli seconds =5000/546=9 Intital value= M-d+1=FFFF-9+1=FFF7H **Assembly code:** CLR P1.3 MOV TMOD,#0001 0000B MOV TL1,#F7H MOV TH1,#FFH SETB P1.3 SETB TR1 Again: JNB TF1 Again CLR TF1 CLR TR1 SJMP back			3 M 3 M
	b)	**8051 Memory organization:** Harvard architecture with duplicate memory maps. Internal RAM: 00-7F H – 128B Internal ROM: 000-FFFH- 4 KB External RAM:0000-FFFFH-64KB External ROM:0000-FFFFH-64KB Types of MOV instructions to work with these memory maps	CO1	L2	2 M 3 M 2 M
(OR)					
9	a)	Stepper motor – Half step/ Full step modes of operation (clock wise/anti clock wise direction) **Diagram:** Interfacing stepper motors 4 windings with any of the port1 pins **Assembly code**	CO2	L2	2 M 2 M 3 M
	b)	**8051 Addressing modes:** list Addressing modes explanation with example instructions 1. Immediate eg: MOV A,#04H 2. Register direct eg: MOV R1,A 3. Register indirect eg: MOV A,@R0 4. Direct eg: MOV R0,42H 5. Indexed eg: MOVC A,@A+PC 6.Implicit eg: RLA	CO1	L1	3 M 4 M