1 a) Describe the Importance of Photo lithography process.
Photolithography is a process used in microfabrication to transfer geometric patterns to a film or substrate. Geometric shapes and patterns on a semiconductor make up the complex structures that allow the dopants, electrical properties and wires to complete a circuit and fulfill a technological purpose.

b) Differentiate diffusion and Ion implantation.
Diffusion is a process of adding impurities atoms from a region with high concentration to a region of low concentration.
Ion implantation is a material surface modification process by which ions of a material are implanted into another solid material, causing a change in the surface physical and chemical properties of the materials.

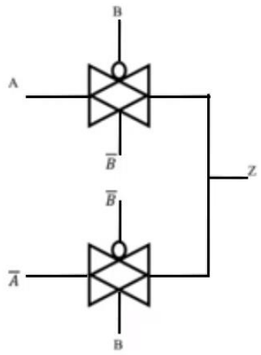
c) Define threshold Voltage.
The minimum gate-to-source voltage (VGS) that is needed to create a conducting path between the source and drain terminals.

d) List out various MOS Layers used in VLSI Design Process.
MOS circuits are formed by three layers i.e. diffusion (n or p diffusion layer), polysilicon and metal, which are isolated from one another by thick or thin (thinox) silicon dioxide insulating layers.

e) Define Stick Diagram.
A stick diagram in VLSI is a type of diagram that is used to lay out a transistor cell. The devices and conductors are represented by “sticks” or lines in stick diagrams.

f) List out different types of scaling.
constant electric field scaling model and the constant voltage scaling model.

g) Draw the transmission gate XOR circuit diagram.



h) List out any 3 applications of Transmission gate Logic.
Electronic (bidirectional switch) switches, analog multiplexers, building blocks for logic circuitry., etc.

i) Define synthesis in ASIC design.
Synthesis is the process of transforming your HDL design into a gate-level netlist.

j) List out the applications of Programmable Logic Devices.
- Digital Systems Design
- Rapid Prototyping:
- Reconfigurability
- Performance
- Cost-effectiveness

k) Write the equation which relates Ids and Vds of MOSFET.
Non-Saturation:

$$I_{ds} = C_0 \mu \frac{W}{L} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

Saturation:

$$I_{ds} = C_0 \mu \frac{W}{2L} (V_{gs} - V_t)^2$$

l) Plot the transfer characteristics of an n-MOS inverter.

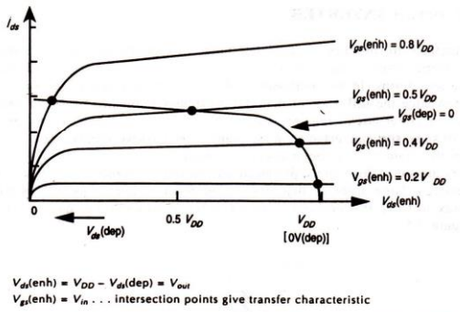


FIGURE 2.6 Derivation of nMOS inverter transfer characteristic.

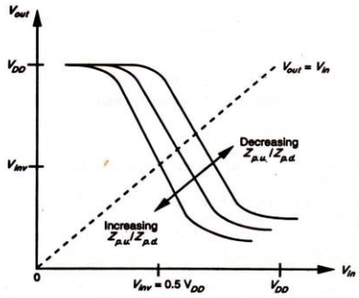


FIGURE 2.7 nMOS inverter transfer characteristic.

m) List out IC fabrication steps.

The IC fabrication starts with the wafer preparation, oxide layer deposition or a protective layer, introducing impurities into the wafer (n-type or p-type), implantation of ions to the surface of the crystal, CVD to produce thin films, photolithography, deposition of the metal for interconnections, and the packaging.

n) Define the time Delay unit.

It is a multiplication of Sheet resistance with Standard unit of capacitance.

Time constant $\tau = (1R_s$ (n channel) $\times 1\square C_g)$ seconds

Unit-I

2 a) Discuss the main Processing steps in C-MOS fabrication using P-well Process.

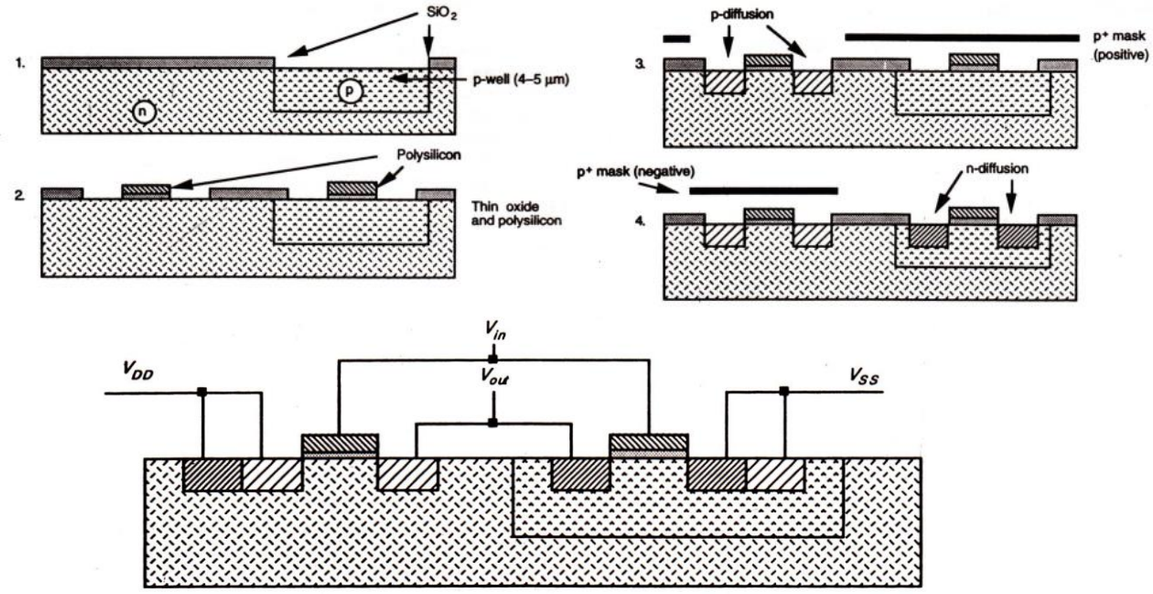


FIGURE 1.10 CMOS p-well inverter showing V_{DD} and V_{SS} substrate connections.

In all other respects—masking, patterning, and diffusion—the process is similar to nMOS fabrication. In summary, typical processing steps are:

- *Mask* 1 — defines the areas in which the deep p-well diffusions are to take place.
- *Mask 2* — defines the thinox regions, namely those areas where the thick oxide is to be stripped and thin oxide grown to accommodate p- and n-transistors and wires.
- *Mask* 3 — used to pattern the polysilicon layer which is deposited after the thin oxide.
- *Mask* 4 — A p-plus mask is now used (to be in effect "Anded" with Mask 2) to define all areas where p-diffusion is to take place.
- *Mask* 5 — This is usually performed using the negative form of the p-plus mask and defines those areas where n-type diffusion is to take place.
- *Mask* 6 — Contact cuts are now defined.
- *Mask* 7 — The metal layer pattern is defined by this mask.
- *Mask* 8 — An overall passivation (overglass) layer is now applied and Mask 8 is needed to define the openings for access to bonding pads.

b) Write a short note on twin tub Structure.

A logical extension of the p-well and n-well approaches is the twin-tub fabrication process. Here we start with a substrate of high resistivity n-type material and then create both n-well and p-well regions. Through this process it is possible to preserve the performance of n-transistors without compromising the p-transistors. Doping control is more readily achieved and some relaxation in manufacturing tolerances results. This is particularly important as far as latch-up is concerned.

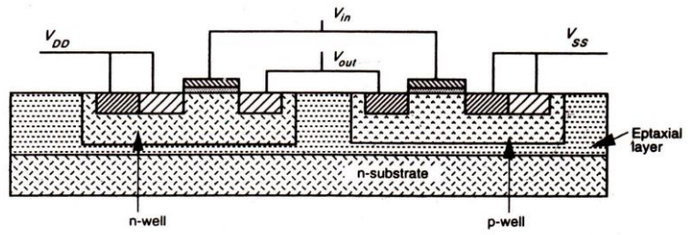


FIGURE 1.14 Twin-tub structure.

3 a) Draw the circuit of n-MOS inverter and explain its operation and characteristics.

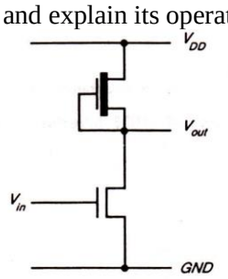


FIGURE 2.5 nMOS inverter.

Operation:

- With no current drawn from the output, the currents I_{ds} for both transistors must be equal.
- For the depletion mode transistor, the gate is connected to the source so it is always on and only the characteristic curve $V_{gs} = 0$ is relevant.
- In this configuration the depletion mode device is called the pull-up (p.u.) and the enhancement mode device the pull-down (p.d.) transistor.
- To obtain the inverter transfer characteristic we superimpose the $V_{gs} = 0$ depletion mode characteristic curve on the family of curves for the enhancement mode device, noting that maximum voltage across the enhancement mode device corresponds to minimum voltage across the depletion mode transistor.
- The points of intersection of the curves as in Figure 2.6 give points on the transfer characteristic, which is of the form shown in Figure 2.7.
- Note that as V_{in}(=V_{gs} p.d. transistor) exceeds the p.d. threshold voltage current begins to flow. The output voltage V_{out} thus decreases and the subsequent increases in V_{in} will cause the p.d. transistor to come out of saturation and become resistive. Note that the p.u. transistor is initially resistive as the p.d. turns on.

Characteristics

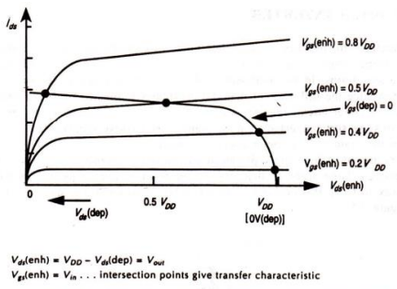


FIGURE 2.6 Derivation of nMOS inverter transfer characteristic.

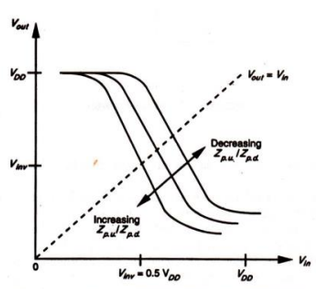
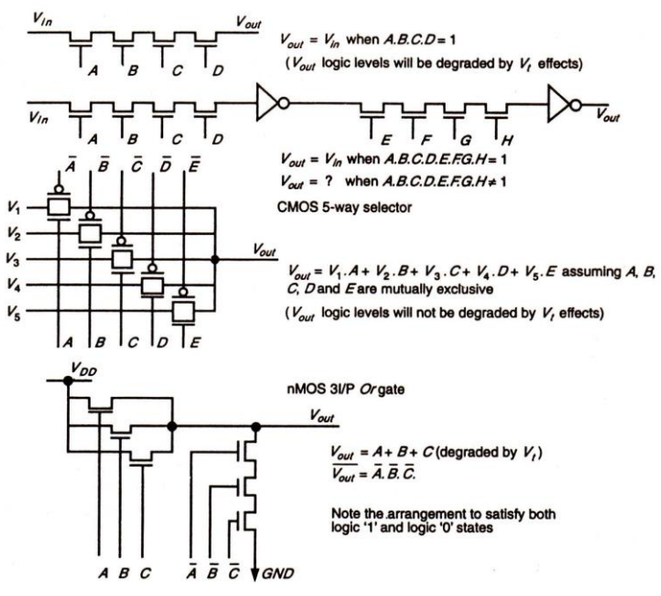


FIGURE 2.7 nMOS inverter transfer characteristic.

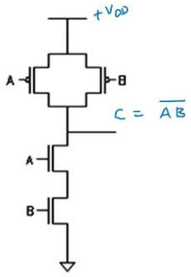
b) Explain about pass Transistor Logic with examples.

Switch (pass transistor) logic is similar to logic arrays based on relay contacts in that the path through each switch is isolated from the signal activating the switch.

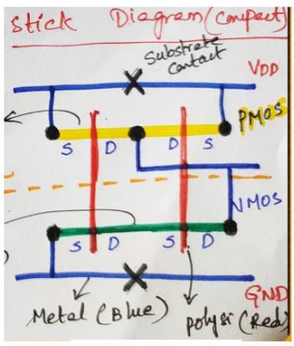


Unit-II

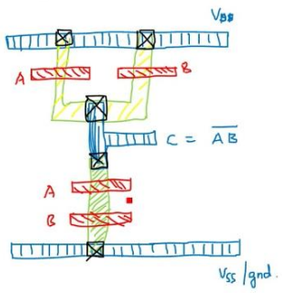
4 a) Design a stick diagram and Layout for two inputs CMOS NAND gate.



Schematic Diagram



Stick Diagram



Layout Diagram

b) Compare n-MOS and CMOS Design styles.

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
	MONOCHROME		MONOCHROME	
GREEN		n-diffusion (n+ active) Thinox *	* Thinox = n-diff. + transistor channels	ND
RED		Polysilicon		NP
BLUE		Metal 1		NM
BLACK		Contact cut		NC
GRAY	NOT APPLICABLE	Overglass		NG
nMOS ONLY YELLOW		Implant		NI
nMOS ONLY BROWN		Buried contact		NB

FEATURE	FEATURE (STICK) (MONOCHROME)	FEATURE (SYMBOL) (MONOCHROME)	FEATURE (MASK) (MONOCHROME)
n-type enhancement mode transistor	D L:W S G L:W S D G	GREEN outline (COLOR) S D G RED line (COLOR)	(L:W = 1:1) S D G
Transistor length to width ratio L:W should be shown but source, drain and gate labeling will not normally be shown.			
n-type depletion mode transistor nMOS ONLY	L:W L:W	GREEN outline (COLOR) S D G YELLOW (COLOR) RED line (COLOR)	(L:W = 1:1)

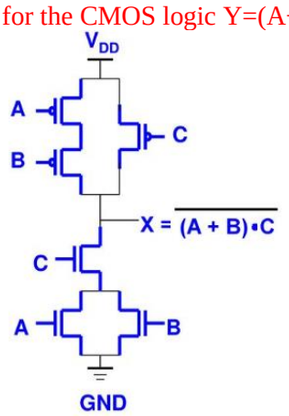
NMOS

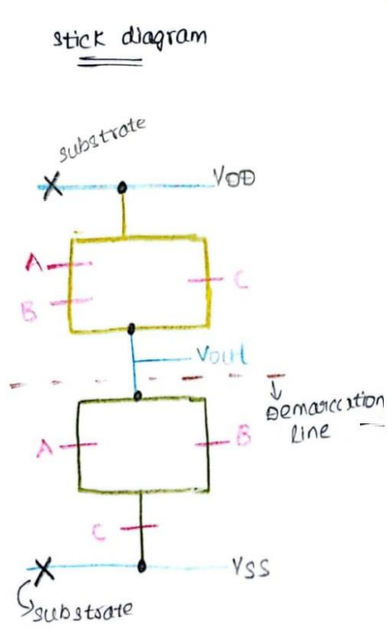
COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
	MONOCHROME		MONOCHROME	
GREEN RED BLUE BLACK GRAY	ENCODING AS IN FIGURE 3–1(a)	n-diffusion (n+ active) Thinox * Polysilicon Metal 1 Contact cut Overglass	* Thinox = n-diff. + p-diff. + transistor channels ENCODING AS IN FIGURE 3–1(a)	CAA or CNA CPF CMF CC COG
GREEN IN P+ (MASK) YELLOW (STICK)		p-diffusion (p+ active)	p+ mask	CAA or CPA
YELLOW	NOT SHOWN IN STICK DIAGRAM	p+ mask		CPP
DARK BLUE OR PURPLE		Metal 2		CMS
BLACK		VIA		CVA
BROWN	DEMARCATION LINE p-well edge is shown as a demarcation line in stick diagrams	p-well		CPW
BLACK		V_{DD} or V_{SS} CONTACT	V_{DD} V_{SS}	CC

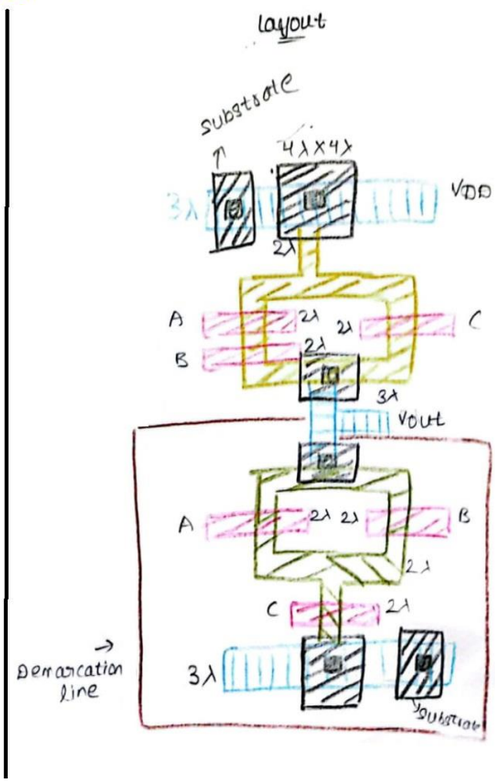
FEATURE	FEATURE (STICK) (MONOCHROME)	FEATURE (SYMBOL) (MONOCHROME)	FEATURE (MASK) (MONOCHROME)
n-type enhancement mode transistor (as in Figure 3–1(a))	DEMARCATION LINE L:W	GREEN RED	S D G
Transistor length to width ratio L:W may be shown.			
p-type enhancement mode transistor	L:W S D G DEMARCATION LINE	YELLOW RED	S D G p+ mask
Note: p-type transistors are placed above and n-type transistors below the demarcation line			

CMOS

5 a) Draw the Stick diagram and layout for the CMOS logic Y=(A+B) C.







b) Explain the effect of scaling factor on Device parameters.

5.2.1 Gate Area A_g

$$A_g = L.W.$$

where L and W are the channel length and width respectively. Both are scaled by $1/\alpha$.

Thus A_g is scaled by $1/\alpha^2$

5.2.2 Gate Capacitance Per Unit Area C_0 or C_{ox}

$C_0 = \frac{\varepsilon_{ox}}{D}$ Thus C_0 is scaled by $\frac{1}{1/\beta} = \beta$

5.2.3 Gate Capacitance C_g

$$C_g = C_0 L.W.$$

Thus C_g is scaled by $\beta \frac{1}{\alpha^2} = \frac{\beta}{\alpha^2}$

5.2.4 Parasitic Capacitance C_x

C_x is proportional to $\frac{A_x}{d}$

Thus C_x is scaled by $\frac{1}{\alpha^2} \cdot \frac{1}{1/\alpha} = \frac{1}{\alpha}$

5.2.5 Carrier Density in Channel Q_{on}

$$Q_{on} = C_0 . V_{gs}$$

where Q_{on} is the average charge per unit area in the channel in the 'on' state. Note that C_0 is scaled by β and V_{gs} is scaled by $1/\beta$.

Thus Q_{on} is scaled by 1

5.2.6 Channel Resistance R_{on}

$$R_{on} = \frac{L}{W} \frac{1}{Q_{on}\mu}$$

where μ is the carrier mobility in the channel and is assumed constant.

Thus R_{on} is scaled by $\frac{1}{\alpha} \frac{1}{1/\alpha} 1 = 1$

5.2.7 Gate Delay T_d

T_d is proportional to $R_{on} . C_g$

Thus T_d is scaled by $\frac{1.\beta}{\alpha^2} \frac{\beta}{\alpha^2}$

5.2.8 Maximum Operating Frequency f_0

$$f_0 = \frac{W}{L} \frac{\mu C_0 V_{DD}}{C_g}$$

or, f_0 is inversely proportional to delay T_d.

Thus f_0 is scaled by $\frac{1}{\beta/\alpha^2} = \frac{\alpha^2}{\beta}$

5.2.9 Saturation Current I_{dss}

$$I_{dss} = \frac{C_0 \mu}{2} \frac{W}{L} (V_{gs} - V_t)^2$$

noting that both V_{gs} and V_t are scaled by $1/\beta$, we have

I_{dss} is scaled by $\beta(1/\beta)^2 = 1/\beta$

5.2.10 Current Density J

$$J = \frac{I_{dss}}{A}$$

where A is the cross-sectional area of the channel in the 'on' state which is scaled by $1/\alpha^2$

So, J is scaled by $\frac{1/\beta}{1/\alpha^2} = \frac{\alpha^2}{\beta}$

5.2.11 Switching Energy Per Gate E_g

$$E_g = \frac{1C_g}{2} (V_{DD})^2$$

So, E_g is scaled by $\frac{\beta}{\alpha^2} \cdot \frac{1}{\beta^2} = \frac{1}{\alpha^2\beta}$

5.2.12 Power Dissipation Per Gate P_g

P_g comprises two components such that

$$P_g = P_{gs} + P_{gd}$$

where the static component

$$P_{gs} = \frac{(V_{DD})^2}{R_{on}}$$

and the dynamic component

$$P_{gd} = E_g f_0$$

It will be seen that both P_{gs} and P_{gd} are scaled by $1/\beta^2$

So, P_g is scaled by $1/\beta^2$

5.2.13 Power Dissipation Per Unit Area P_a

$$P_a = \frac{P_g}{A_g}$$

noting that both V_{gs} and V_t are scaled by $1/\beta$, we have

I_{dss} is scaled by $\beta(1/\beta)^2 = 1/\beta$

5.2.10 Current Density J

$$J = \frac{I_{dss}}{A}$$

where A is the cross-sectional area of the channel in the 'on' state which is scaled by $1/\alpha^2$

So, J is scaled by $\frac{1/\beta}{1/\alpha^2} = \frac{\alpha^2}{\beta}$

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It will be seen that both P_{gs} and P_{gd} are scaled by $1/\beta^2$

So, P_g is scaled by $1/\beta^2$

5.2.13 Power Dissipation Per Unit Area P_a

$$P_a = \frac{P_g}{A_g}$$

So, P_a is scaled by $\frac{1/\beta^2}{1/\alpha^2} = \alpha^2/\beta^2$

5.2.14 Power-speed Product P_T

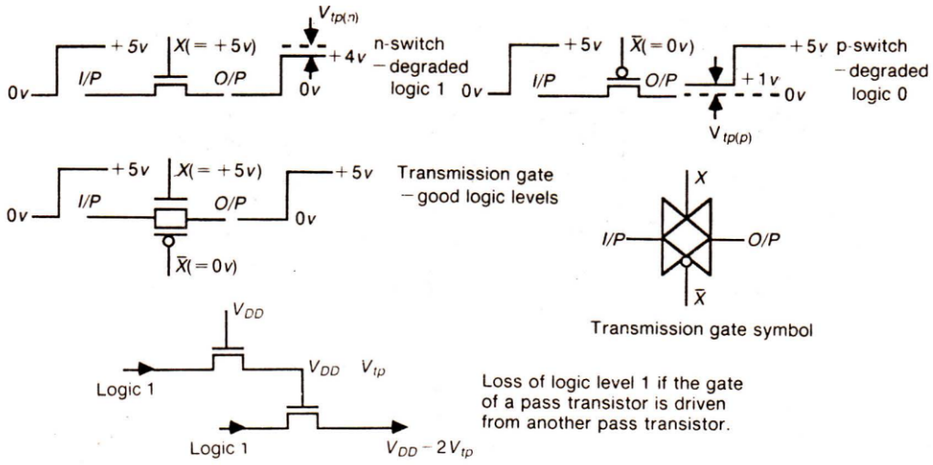
$$P_T = P_g . T_d$$

So, P_T is scaled by $\frac{1}{\beta^2} \cdot \frac{\beta}{\alpha^2} = \frac{1}{\alpha^2\beta}$

Unit-III

6 a) What is switch logic? How switch Logic can be implemented by using Transmission Gate logic.

Switch (pass transistor) logic is similar to logic arrays based on relay contacts in that the path through each switch is isolated from the signal activating the switch.



b) Design 4-bit ALU to implement various logic and arithmetic functions using 4-bit adder.

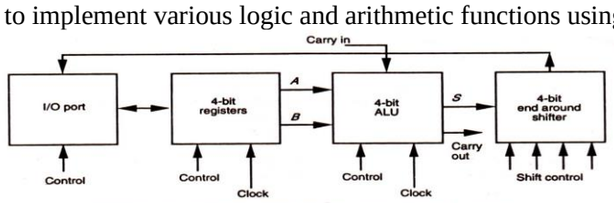


FIGURE 8.1 4-bit data path for processor (block diagram).

TABLE 8.1 Truth table for binary adder

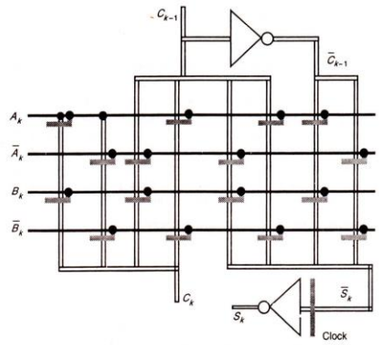
Inputs			Outputs	
A_k	B_k	Previous carry C_{k-1}	Sum S_k	New carry C_k
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Sum $S_k = H_k\bar{C}_{k-1} + \bar{H}_kC_{k-1}$

New carry $C_k = A_kB_k + H_kC_{k-1}$

where

Half sum $H_k = \bar{A}_kB_k + A_k\bar{B}_k$



Multiplexer (*n*-switches)-based adder logic with stored and buffered sum output.

Sum $S_k = \bar{H}_kC_{k-1} + H_k\bar{C}_{k-1}$

New carry $C_k = A_kB_k + H_kC_{k-1}$

where Half sum $H_k = \bar{A}_kB_k + A_k\bar{B}_k$

Consider, first, the *Sum* output if C_{k-1} is held at logical 0, then

$$S_k = H_k.1 + \bar{H}_k.0 = H_k$$

that is $S_k = H_k = A_kB_k + A_k\bar{B}_k$—An *Exclusive-Or* operation

Now, hold C_{k-1} at logical 1, then

$$S_k = H_k.0 + \bar{H}_k.1 = \bar{H}_k$$

that is

$$S_k = \bar{H}_k = \bar{A}_k\bar{B}_k + A_kB_k$$—An *Exclusive-Nor* (*Equality*) operation

Next, consider the *carry* output of each element, first if C_{k-1} is held at logical 0.

Then

$$C_k = A_k.B_k + H_k.0 = A_k.B_k$$— An *And* operation

Now, if C_{k-1} is held at logical 1, then

$$C_k = A_k.B_k + H_k.1 = A_k.B_k + \bar{A}_k.B_k + A_k.\bar{B}_k$$

Therefore

$C_k = A_k + B_k$ — An *Or* operation

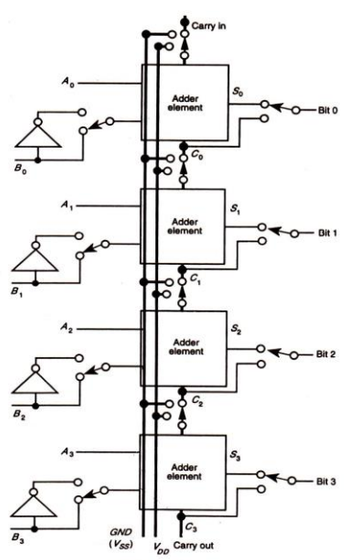


FIGURE 8.12 4-bit ALU.

7 a) Discuss in detail about the other forms of CMOS logic.

1.Pseudo-nMOS logic

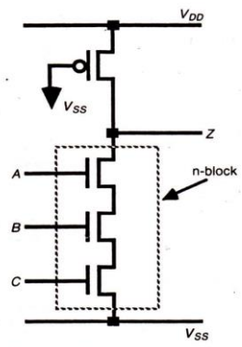


FIGURE 6.9 Pseudo-nMOS *Nand* gate.

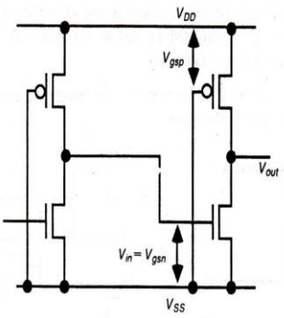
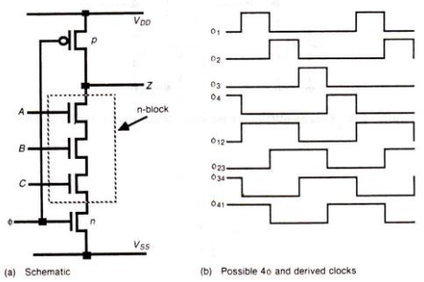


FIGURE 6.10 Pseudo-nMOS inverter when driven from a similar inverter.

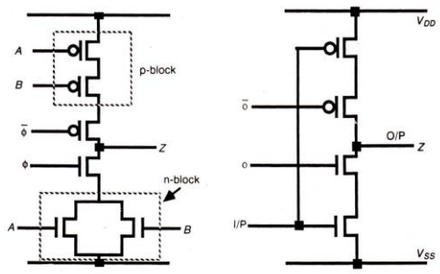
2. Dynamic CMOS logic

1. Charge sharing may be a problem unless the inputs are constrained not to change during the on period of the clock.



(a) Schematic (b) Possible 4ϕ and derived clocks

3. Clocked CMOS (C2M0S) logic



(a) 2 1/P *Nor* gate (b) Inverter

FIGURE 6.12 Clocked CMOS (C^2MOS) logic.

4.(C2M0S) Domino **logic**

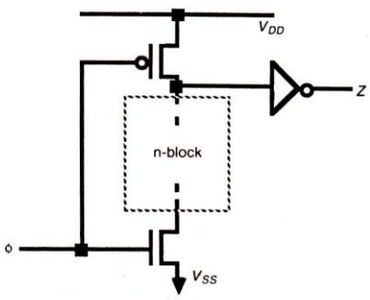


FIGURE 6.13 CMOS domino logic.

5. n-p CMOS logic

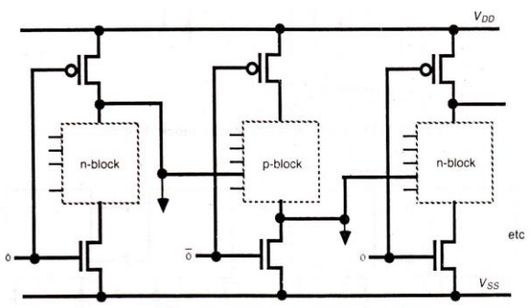
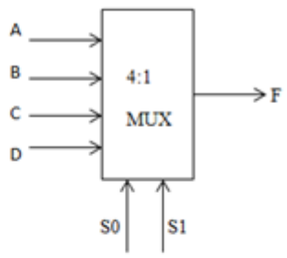
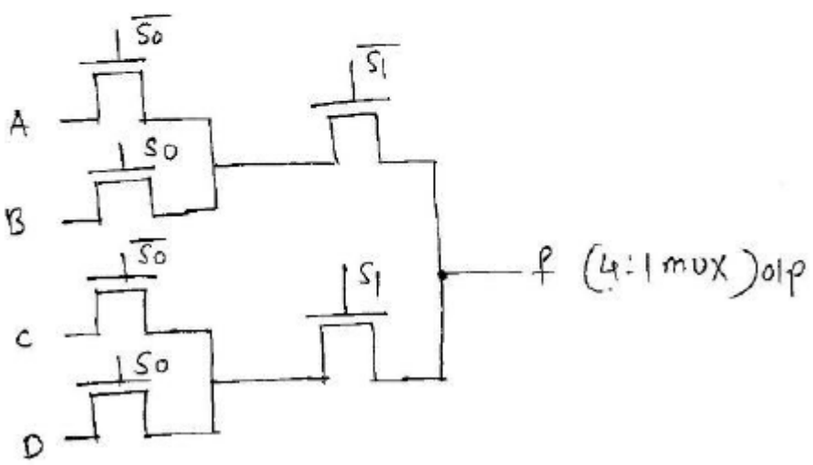


FIGURE 6.14 n-p CMOS logic.

b) Design 4X1 multiplexer using PASS Transistor. Draw STICK diagram for the same.

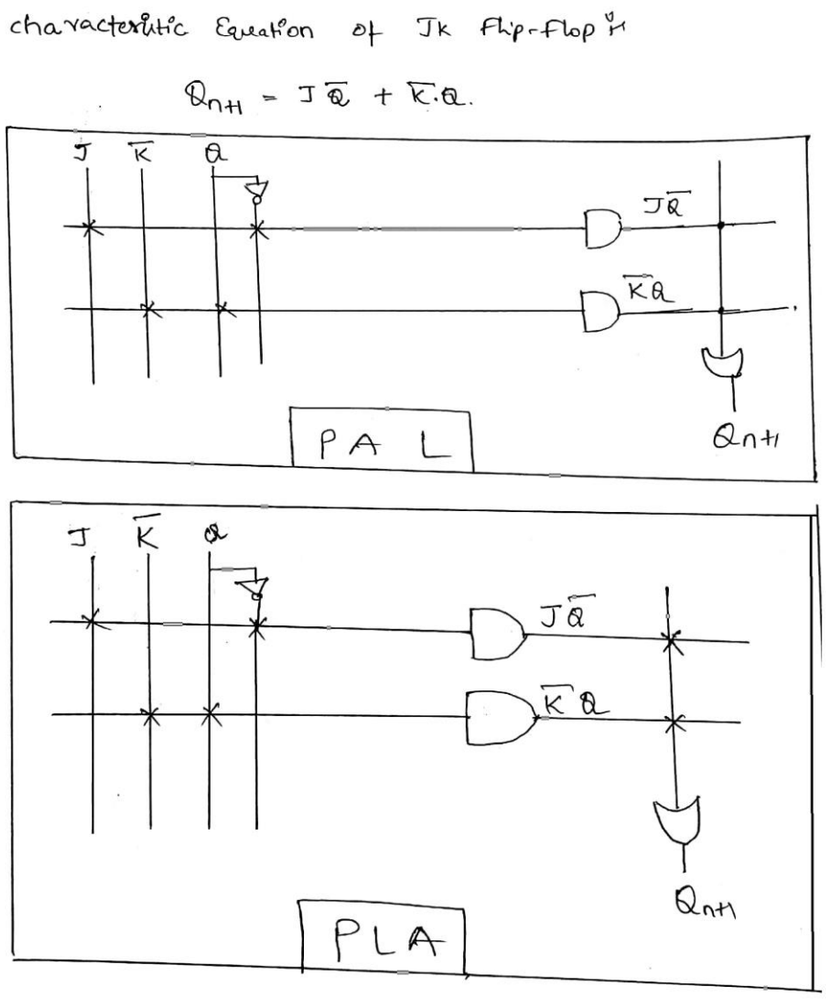
S1	S0	F
0	0	A
0	1	B
1	0	C
1	1	D



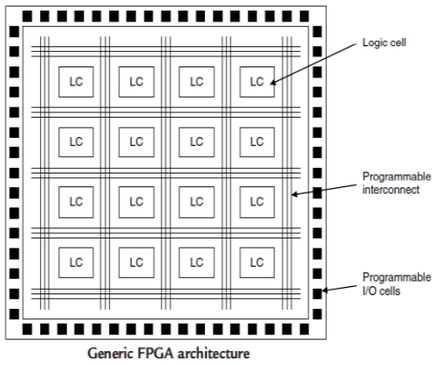


Unit-IV

8 a) Design a J-K Flip Flop using PLA and PAL.



b) Draw the architecture of FPGA And explain about CLB.



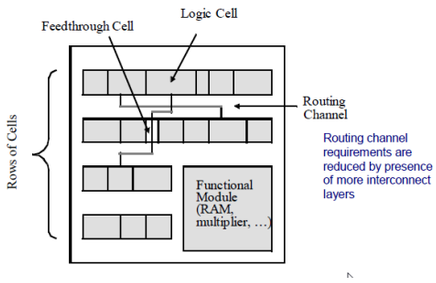
Generic FPGA architecture

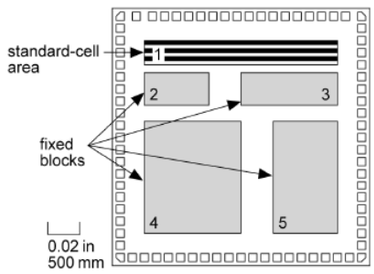
- FPGA consists of a regular array of **programmable logic blocks (CLB)** interconnected by a **programmable routing network**.
- The chip inputs and outputs use special I/O logic cells that are different from the basic logic cells.
- The programming technology in an FPGA determines the type of basic logic cell and the interconnect scheme.

Configurable Logic Block (CLB)

- A CLB is a basic component of an FPGA that provides the **basic logic** and **storage functionality** for a target application design.
- Exact numbers and features vary from device to device, but every CLB consists of a configurable switch matrix with 4 or 6 inputs, some selection circuitry (MUX, etc), and flip-flops.
- The switch matrix is highly flexible and can be configured to handle combinatorial logic, shift registers or RAM.
- The CLB acts as the main logic resource for implementing logic circuits. Generally, the CLBs contain RAM based LUTs (look up tables) to implement logic and storage elements that can be used as flip-flops or latches.
- CLBs can be programmed to perform various logical functions as well as to store data.

9 a) With the help of Block Diagram Explain the Principle and operation of Standard cell Based ASICs.





- The diagram shows a cell-based ASIC (CBIC) die with a single standard-cell area together with four fixed blocks.
- The flexible block contains rows of standard cells.
- The **small squares around the edge** of the die are **bonding pads** that are connected to the pins of the ASIC package.
- Each standard cell in the library is constructed using full-custom design methods. This design style provides the same performance and flexibility advantages of a full-custom ASIC but reduces design time and reduces risk.

The important features are:

- All mask layers are customized-transistors and interconnect-Automated buffer sizing, placement and routing.
- Custom blocks can be embedded.
- Manufacturing lead time is about eight weeks.
- Simpler than full-custom design.
- Standard cells can be placed anywhere in the silicon die.

b) Compare CPLD and FPGA in Detailed.

Features	CPLD	FPGA
Full Forms	CPLD is an abbreviation for Complex Programmable Logic Devices.	FPGA is an abbreviation for Field Programmable Gate Arrays.
Definition	It is an integrated circuit that assists in the execution of digital systems.	It is an integrated circuit that is mainly created to be customized after manufacturing by a customer or a developer.
Ratio of flip-flops	It has a low flip-flop ratio than FPGA.	It has a high flip-flop ratio than CPLD.
Density	It has a low to medium density.	It has a medium to high density.
Structure resembles	It is equivalent to the PAL.	It is similar to a Gate array.
Logic Blocks	It may only store a few thousand logic blocks.	It may include up to 100,000 small logic blocks.
Power Consumption	It has a larger power usage.	It has lower power consumption.
Based on	It is based on EEPROM.	It is based on RAM.
Cost	It is less expensive than FPGA.	It is more expensive than CPLD.
Architecture	It is classified as a coarse grain.	It is classified as fine grain.
Applications	It is better suited for simpler apps.	It is appropriate for complicated apps.
Security	It provides more security than FPGA.	It provides less security than CPLD.
Performance	Its performance depends on the routing.	It provides stable performance that is independent of internal routing.
Volatility	Data will not be lost if the power is turned off.	If the power is off, the data may be lost.

III B.Tech Regular DEGREE EXAMINATION
Electronics &Communication Engineering
Name of the Subject: VLSI Design
Subject Code: 20EC601
Date of Exam: 27-07-2023

Signature of the HOD **Signature of the Faculty**