Lab Code:20ECL302
Electronic Devices
Lab Manual

Department of Electronics & Communication Engineering

Bapatla Engineering College :: Bapatla

(Autonomous)

G.B.C. Road, Mahatmajipuram, Bapatla-522102, Guntur (Dist.)
Andhra Pradesh, India.
E-Mail:bec.principal@becbapatla.ac.in
Web:www.becbapatla.ac.in

Contents

Bapatla Engineering College :: Bapatla
(Autonomous)

Vision

- To build centers of excellence, impart high quality education and instill high standards of ethics and professionalism through strategic efforts of our dedicated staff, which allows the college to effectively adapt to the ever changing aspects of education.

- To empower the faculty and students with the knowledge, skills and innovative thinking to facilitate discovery in numerous existing and yet to be discovered fields of engineering, technology and interdisciplinary endeavors.

Mission

- Our Mission is to impart the quality education at par with global standards to the students from all over India and in particular those from the local and rural areas.

- We continuously try to maintain high standards so as to make them technologically competent and ethically strong individuals who shall be able to improve the quality of life and economy of our country.

Bapatla Engineering College :: Bapatla
(Autonomous)
Department of Electronics and Communication Engineering

Vision

To produce globally competitive and socially responsible Electronics and Communication Engineering graduates to cater the ever changing needs of the society.

Mission

- To provide quality education in the domain of Electronics and Communication Engineering with advanced pedagogical methods.

- To provide self learning capabilities to enhance employability and entrepreneurial skills and to inculcate human values and ethics to make learners sensitive towards societal issues.

- To excel in the research and development activities related to Electronics and Communication Engineering.

Bapatla Engineering College :: Bapatla

(Autonomous)

Department of Electronics and Communication Engineering

Program Educational Objectives (PEO's)

PEO-I: Equip Graduates with a robust foundation in mathematics, science and Engineering Principles, enabling them to excel in research and higher education in Electronics and Communication Engineering and related fields.

PEO-II: Impart analytic and thinking skills in students to develop initiatives and innovative ideas for Start-ups, Industry and societal requirements.

PEO-III: Instill interpersonal skills, teamwork ability, communication skills, leadership, and a sense of social, ethical, and legal duties in order to promote lifelong learning and Professional growth of the students.

Program Outcomes (PO's)

Engineering Graduates will be able to:

PO1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7.Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. Individual and Teamwork: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. Life-long learning: Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Bapatla Engineering College:: Bapatla

(Autonomous)

Department of Electronics and Communication Engineering

Program Specific Outcomes (PSO's)

PSO1: Develop and implement modern Electronic Technologies using analytical methods to meet current as well as future industrial and societal needs.

PSO2: Analyze and develop VLSI, IoT and Embedded Systems for desired specifications to solve real world complex problems.

PSO3: Apply machine learning and deep learning techniques in communication and signal processing.

Electronic Devices Lab
II B.Tech – III Semester (Code: 20ECL302)

Lectures	0	Tutorial	0	Practical	3	Credits	1.5
Continuous Internal Assessment			30	Semester End Examination (3 Hours)			70

Prerequisites: None

Course Objectives: Students will

- Study the V-I characteristics of various semiconductor devices.
- Simulate the V-I characteristics of various semiconductor devices using Software
- Learn the various bias circuits of B.J.T.
- Simulate the various bias circuits of B.J.T using software

Course Outcomes: After studying this course, the students will be able to

CO1	Plot the V-I characteristics of various semiconductor devices
CO2	Simulate the characteristics of various semiconductor devices using software
CO3	Design of fixed, collector to base and self-bias circuits for BJT.
CO4	Simulate fixed, collector to base and self-bias circuits for B.J.T using Software.

Mapping of Course Outcomes with Program Outcomes & Program Specific Outcomes

	PO's												PSO's		
CO	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
CO1	2			3					3				2		
CO2					2				3				2		
CO3	2			3					3				2		
CO4					2				3				2		
AVG	2			3	2				3				2		

LIST OF LAB EXPERIMENTS

1. Characteristics of Silicon and Germanium diode
2. Characteristics of Zener diode and its regulation characteristics
3. Characteristics of BJT in Common Base configuration
4. Characteristics of BJT in Common Emitter configuration.
5. Characteristics of Emitter follower circuit.

6. Output and Transfer Characteristics of JFET
7. Characteristics of UJT
8. Design and verification of self-bias circuit for BJT
9. Design and verification of collector to base bias circuit for BJT
10. Design and verification of Fixed bias circuit for BJT
11. Voltage Regulator using BJT
12. Characteristics of SCR.
13. Study of CRO.
14. Characteristics of Triac
15. Characteristics of Photo Transistor

NOTE: A minimum of 10 (Ten) experiments have to be Performed and recorded by the candidate to attain eligibility for Semester End Examination.

1. Characteristics of Silicon and Germanium diode

Aim:

To find out the V-I characteristics of silicon and germanium diodes in Forward and Reverse bias configurations.

Apparatus required:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	P-N Diodes DR25, BY126	Refer Appendix A	1
2	Resistor	1k	1
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-200 mA, 0-200μA)	2
5	Voltmeter	(0-20 V)	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

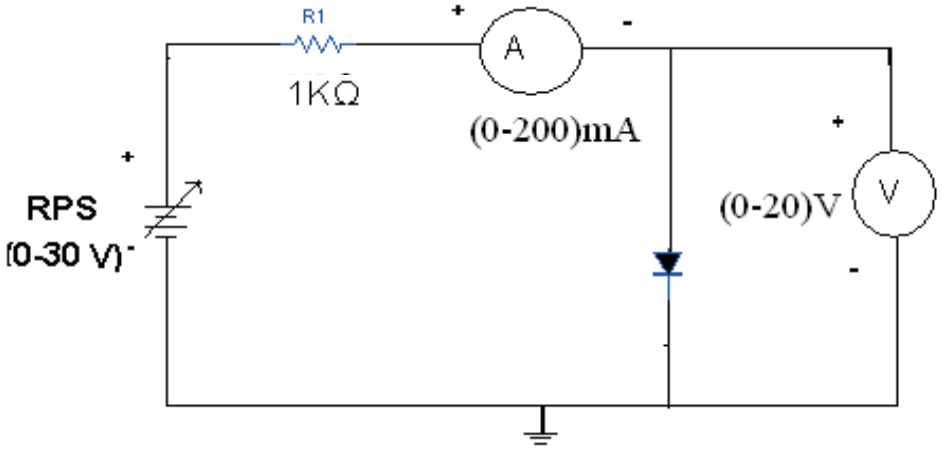
Theory:

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage.

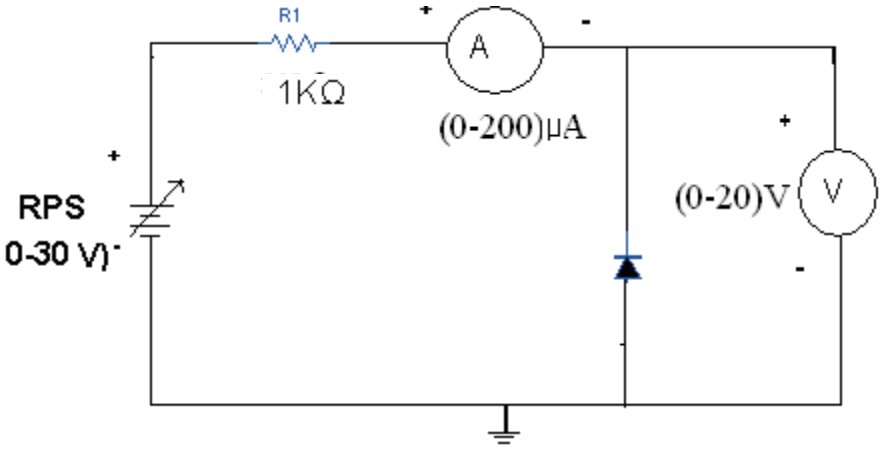
When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected to the –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current is due to minority charge carriers.

CIRCUIT DIAGRAM:-

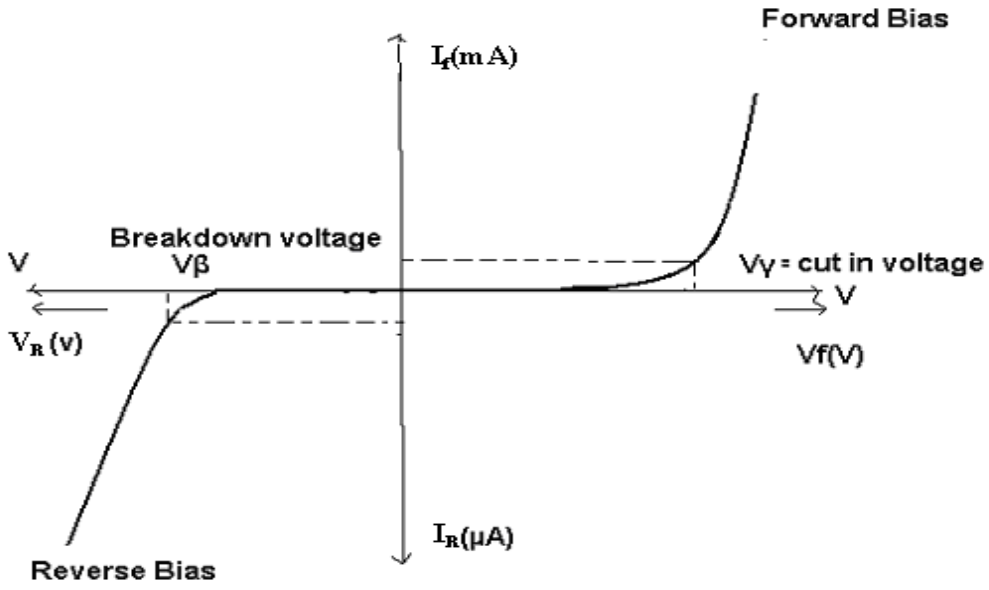
FORWARD BIAS:-



REVERSE BIAS:-



MODEL WAVEFORM:-



PROCEDURE:-

FORWARD BIAS:-

1. Connections are made as per the circuit diagram.
2. For forward bias, the RPS +ve is connected to the anode of the silicon diode and RPS –ve is connected to the cathode of the diode.
3. Switch on the power supply and increases the input voltage (supply voltage) in steps.
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The readings of voltage and current are tabulated and a graph is plotted between voltage and current.
6. Repeat the above procedure for Germanium diode also and tabulate the results.

OBSERVATION:-

S.NO	APPLIED VOLTAGE(V)	VOLTAGE ACROSS DIODE (V)	DIODE CURRENT (mA)

PROCEDURE:-

REVERSE BIAS:-

1. Connections are made as per the circuit diagram

2 . For reverse bias, the RPS +ve is connected to the cathode of the silicon diode and RPS –ve is connected to the anode of the diode.

3. Switch on the power supply and increase the input voltage (supply voltage) in steps.

4. Note down the corresponding current flowing through the diode voltage across the diode for each and every step of the input voltage.

5. The readings of voltage and current are tabulated and graph is plotted between voltage and current.

7. Repeat the above procedure for the given Germanium diode also and tabulate the results obtained.

OBSEVATION:-

S.NO	APPLIED VOLTAGE (V)	VOLTAGE ACROSS DIODE(V)	DIODE CURRENT (µA)

PRECAUTIONS:-

1. All the connections should be correct.

2. Parallax error should be avoided while taking the readings from the Analog meters.

VIVA QESTIONS:-

1. Define depletion region of a diode?
2. What is meant by transition & space charge capacitance of a diode?
3. Is the V-I relationship of a diode Linear or Exponential?
4. Define cut-in voltage of a diode and specify the values for Si and Ge diodes?
5. What are the applications of a p-n diode?
6. Draw the ideal characteristics of P-N junction diode?

2. ZENER DIODE CHARACTERISTICS

Aim:

a) To observe and draw the static characteristics of a zener diode

b) To find the voltage regulation of a given zener diode

Apparatus Required:

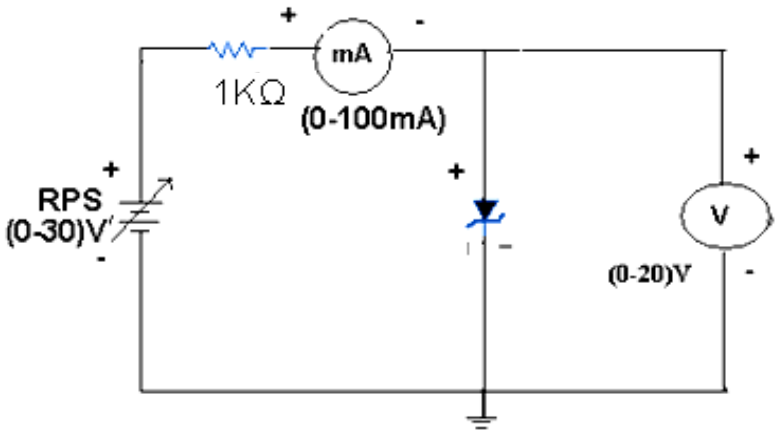
S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Zener Diode BZ7	Refer Appendix A	1
2	Resistor	1KΩ	1
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-200 mA, 0-200μA)	2
5	Voltmeter	(0-20 V)	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

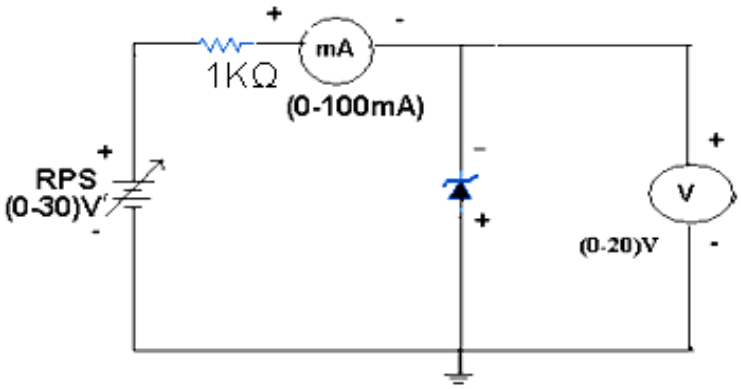
Theory:-

A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device. To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals whatever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

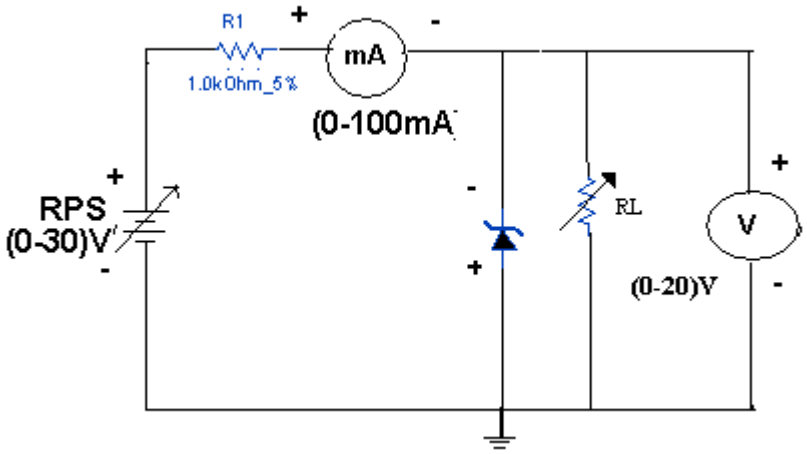
CIRCUIT DIAGRAM:-

STATIC CHARACTERISTICS:-





REGULATION CHARACTERISTICS:-



PROCEDURE:-

Static characteristics:-

1. Connections are made as per the circuit diagram.
2. The Regulated power supply voltage is increased in steps.
3. The zener current (lz), and the zener voltage (Vz.) are observed and then noted in the tabular form.
4. A graph is plotted between zener current (Iz) and zener voltage (Vz).

Regulation characteristics:-

1. The voltage regulation of any device is usually expressed as percentage regulation
2. The percentage regulation is given by the formula

$((V_{NL}-V_{FL})/V_{FL})X100$

V_{NL}=Voltage across the diode, when no load is connected.

V_{FL}=Voltage across the diode, when load is connected.

3. Connection are made as per the circuit diagram
4. The load is placed in full load condition and the zener voltage (Vz), Zener current (lz), load current (I_L) are measured.
5. The above step is repeated by decreasing the value of the load in steps.
6. All the readings are tabulated.
7. The percentage regulation is calculated using the above formula

OBSERVATIONS:-

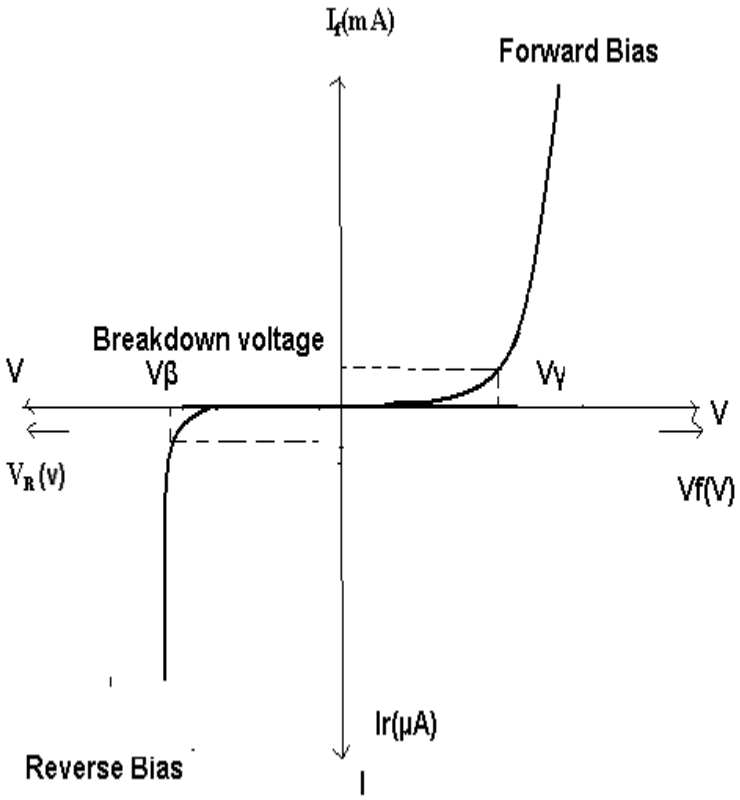
Static characteristics:-

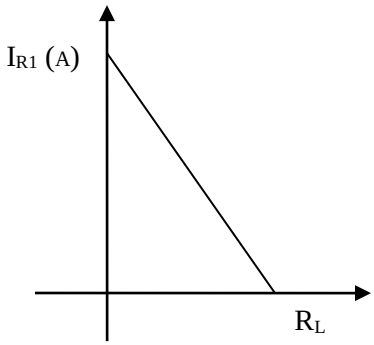
S.NO	ZENER VOLTAGE(V_Z)	ZENER CURRENT(I_Z)

Regulation characteristics:-

S.NO	V_{NL}(VOLTS)	V_{FL} (VOLTS)	R_L (KΩ)	% REGULATION

MODEL WAVEFORMS:-





PRECAUTIONS:-

1. The terminals of the zener diode should be properly identified
2. While determined the load regulation, load should not be immediately shorted.
3. Should be ensured that the applied voltages & currents do not exceed the ratings of the diode.

RESULT:-

a) Static characteristics of zener diode are obtained and drawn.

b) Percentage regulation of zener diode is calculated.

VIVAQUESTIONS:-

1. What type of temp? Coefficient does the zener diode have?
2. If the impurity concentration is increased, how the depletion width effected?
3. Does the dynamic impendence of a zener diode vary?
4. Explain briefly about avalanche and zener breakdowns?
5. Draw the zener equivalent circuit?
6. Differentiate between line regulation & load regulation?
7. In which region zener diode can be used as a regulator?
8. How the breakdown voltage of a particular diode can be controlled?
9. What type of temperature coefficient does the Avalanche breakdown has?
10. By what type of charge carriers the current flows in zener and avalanche breakdown diodes?

3. Characteristics of BJT in Common Base configuration

AIM: 1.To observe and draw the input and output characteristics of a transistor connected in common base configuration.

APPARATUS:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Transistor (BC107 or SL100)	Refer Appendix A	1
2	Resistor	100Ω, 100KΩ	1
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-200 mA, 0-200μA)	2
5	Voltmeter	(0-20 V)	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

Theory:

A transistor is a three terminal active device. The terminals are emitter, base, collector. In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased.

In CB configuration, I_E is +ve, I_C is –ve and I_B is –ve. So,

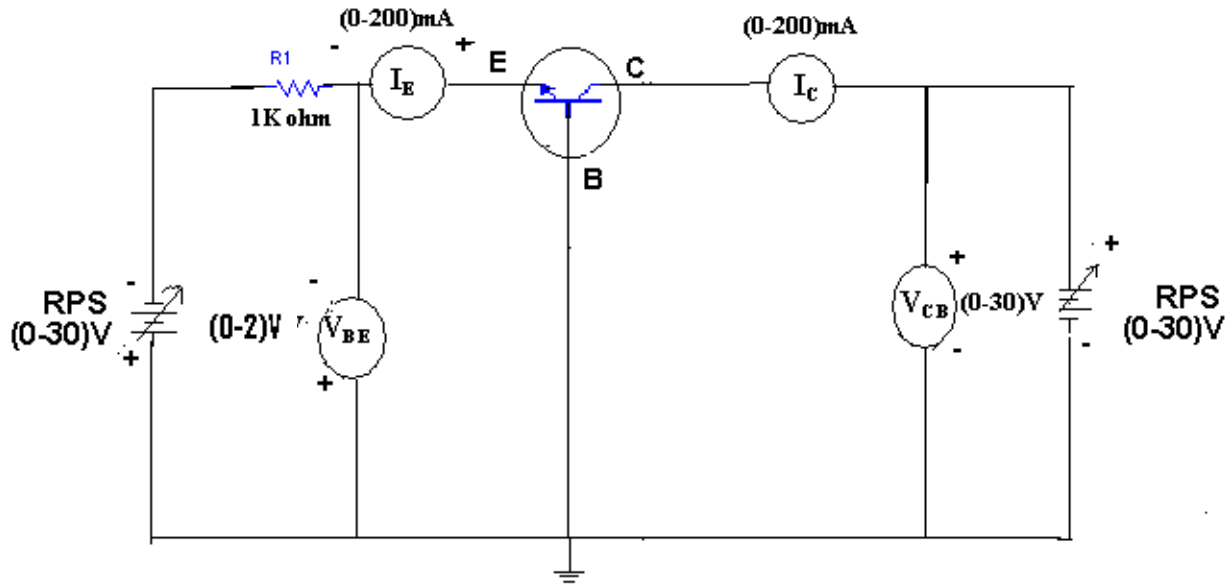
$$V_{EB}=f1\ (V_{CB},I_E) \text{ and}$$

$$I_C=f2\ (V_{CB},I_B)$$

With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width 'W' decreases. This phenomenon is known as "Early effect". Then, there will be less chance for recombination within the base region. With increase of charge gradient with in the base region, the current of minority carriers injected across the emitter junction increases. The current amplification factor of CB configuration is given by,

$$\alpha = \Delta I_C / \Delta I_E$$

CIRCUIT DIAGRAM



PROCEDURE:

INPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the input characteristics, the output voltage V_{CE} is kept constant at 0V and for different values of V_{EB} note down the values of I_E.
3. Repeat the above step keeping V_{CB} at 2V, 4V, and 6V.All the readings are tabulated.
4. A graph is drawn between V_{EB} and I_E for constant V_{CB}.

OUTPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the output characteristics, the input I_E iskept constant at 10m A and for different values of V_{CB}, note down the values of I_C.
3. Repeat the above step for the values of I_E at 20 mA, 40 mA, and 60 mA, all the readings are tabulated.
4. A graph is drawn between V_{CB} and Ic for constant I_E

OBSERVATIONS:

INPUT CHARACTERISTICS:

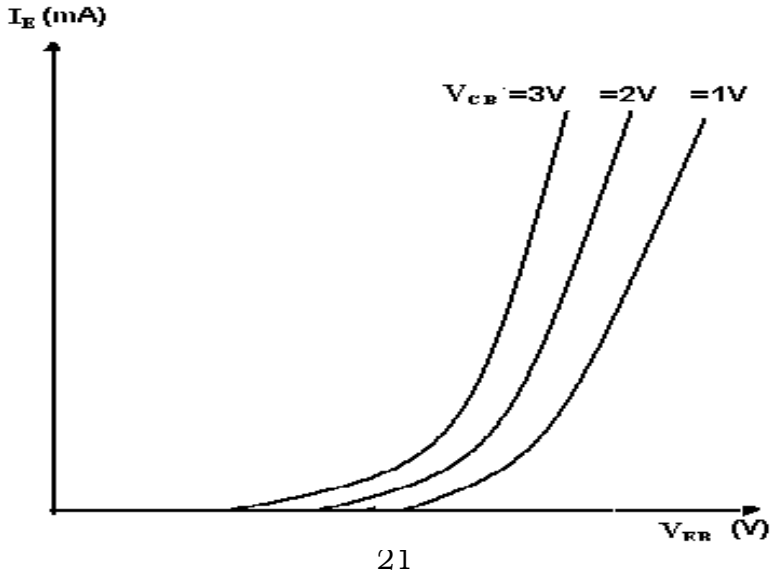
S.No	V_{CB}=0V		V_{CB}=1V		V_{CB}=2V	
	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)

OUTPUT CHARACTERISTICS:

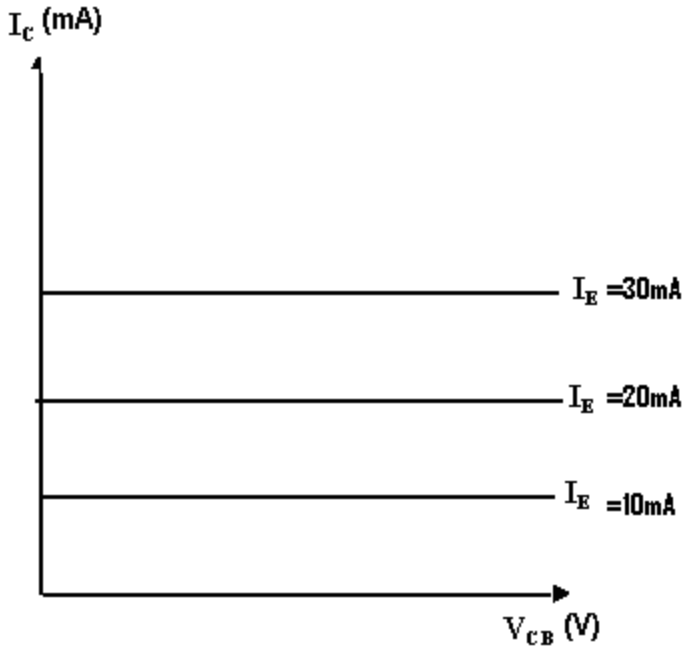
S.No	I_E=10mA		I_E=20mA		I_E=30mA	
	V_{CB}(V)	I_C(mA)	V_{CB}(V)	I_C(mA)	V_{CB}(V)	I_C(mA)

MODEL GRAPHS:

INPUT CHARACTERISTICS



OUTPUT CHARACTERISTICS



PRECAUTIONS:

1. The supply voltages should not exceed the rating of the transistor.
2. Meters should be connected properly according to their polarities.

VIVA QUESTIONS:

1. What is the range of α for the transistor?
2. Draw the input and output characteristics of the transistor in CB configuration?
3. Identify various regions in output characteristics?
4. What is the relation between α and β?
5. What are the applications of CB configuration?
6. What are the input and output impedances of CB configuration?
7. Define α(alpha)?
8. What is EARLY effect?
9. Draw diagram of CB configuration for PNP transistor?
10. What is the power gain of CB configuration?

4. Characteristics of BJT in Common Emitter configuration

AIM: To draw the input and output characteristics of transistor connected in CE configuration

APPARATUS:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Transistor (BC107 or SL100)	Refer Appendix A	1
2	Resistor	100Ω, 100KΩ	1
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-200 mA, 0-200μA)	2
5	Voltmeter	(0-20 V)	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and out put is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output.

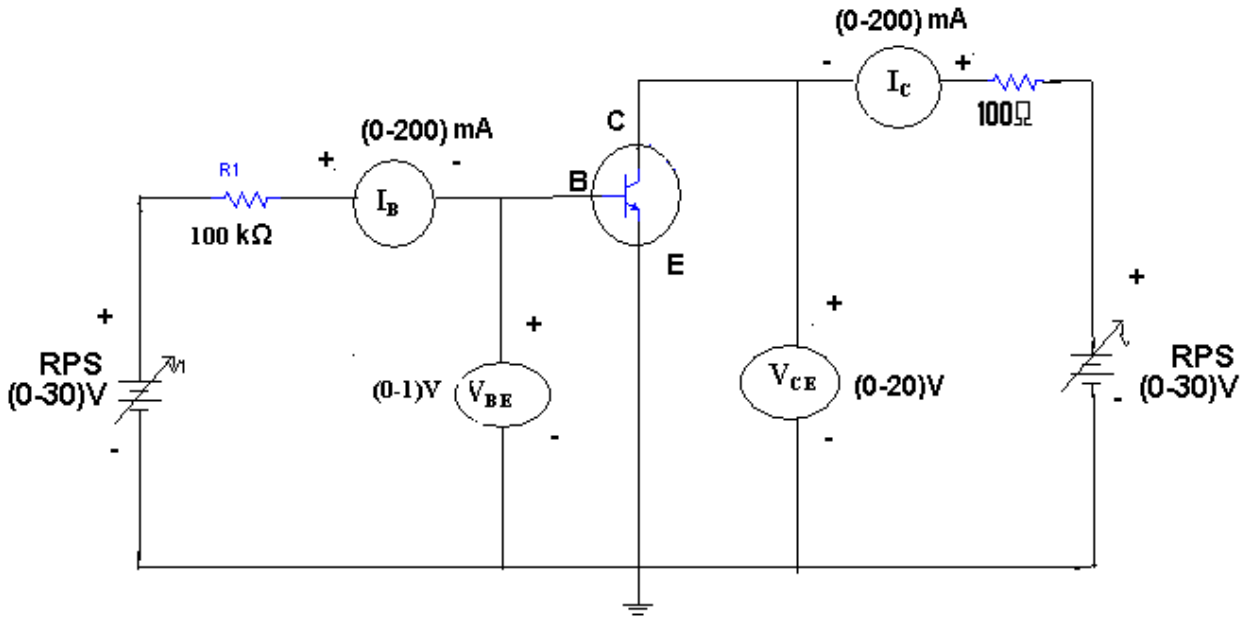
The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE} . Therefore input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between I_c and V_{CE} at constant I_B. the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to I_B.

The current amplification factor of CE configuration is given by

$$B = \Delta I_C / \Delta I_B$$

CIRCUIT DIAGRAM:



PROCEDURE:

INPUT CHARECTERSTICS:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 1V and for different values of V_{BE} . Note down the values of I_C
3. Repeat the above step by keeping V_{CE} at 2V and 4V.
4. Tabulate all the readings.
5. plot the graph between V_{BE} and I_B for constant V_{CE}

OUTPUT CHARACTERSTICS:

1. Connect the circuit as per the circuit diagram
2. for plotting the output characteristics the input current I_B is kept constant at 10μA and for different values of V_{CE} note down the values of I_C
3. repeat the above step by keeping IB at 75 μA 100 μA
4. tabulate the all the readings
5. plot the graph between V_{CE} and I_C for constant I_B

OBSERVATIONS:

INPUT CHARACTERISTICS:

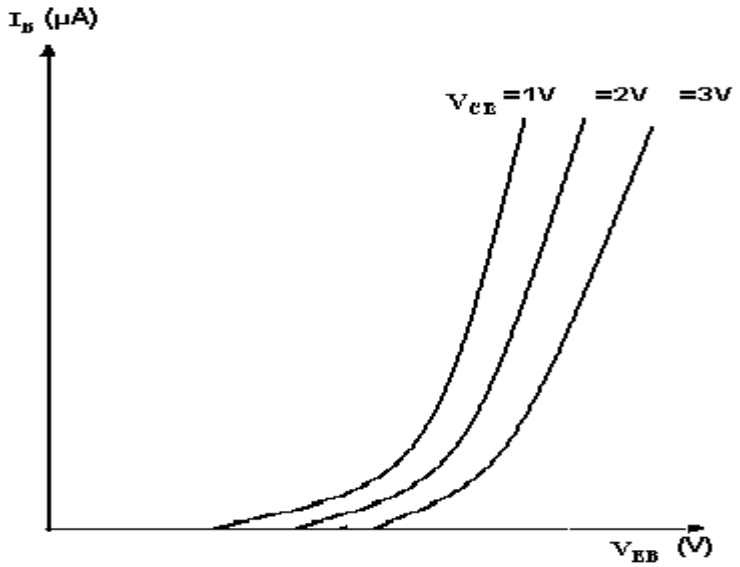
S.NO	V_{CE} = 1V		V_{CE} = 2V		V_{CE} = 4V	
	V_{BE}(V)	I_B(µA)	V_{BE}(V)	I_B(µA)	V_{BE}(V)	I_B(µA)

OUT PUT CHAREACTARISTICS:

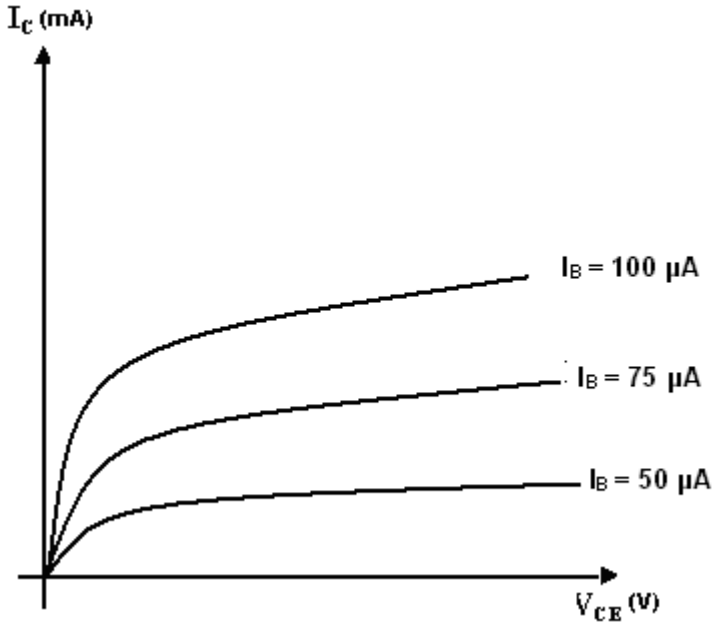
S.NO	I_B = 50 µA		I_B = 75 µA		I_B = 100 µA	
	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_CmA)	V_{CE}(V)	I_C(mA)

MODEL GRAPHS:

INPUT CHARACTERSTICS:



OUTPUT CHARECTERSTICS:



PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor
2. Meters should be connected properly according to their polarities

VIVA QUESTIONS:

1. What is the range of β for the transistor?
2. What are the input and output impedances of CE configuration?
3. Identify various regions in the output characteristics?
4. what is the relation between α and β
5. Define current gain in CE configuration?
6. Why CE configuration is preferred for amplification?
7. What is the phase relation between input and output?
8. Draw diagram of CE configuration for PNP transistor?
9. What is the power gain of CE configuration?
10. What are the applications of CE configuration?

5. CHARACTERSTICS OF EMITTER FOLLOWER CIRCUIT

AIM: To draw the input and output characteristics of transistor connected in CC (Common Collector) or Emitter follower configuration.

APPARATUS:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Transistor (BC107 or SL100)	Refer Appendix A	1
2	Resistor	100Ω, 100KΩ	1
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-200 mA, 0-200μA)	2
5	Voltmeter	(0-20 V)	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

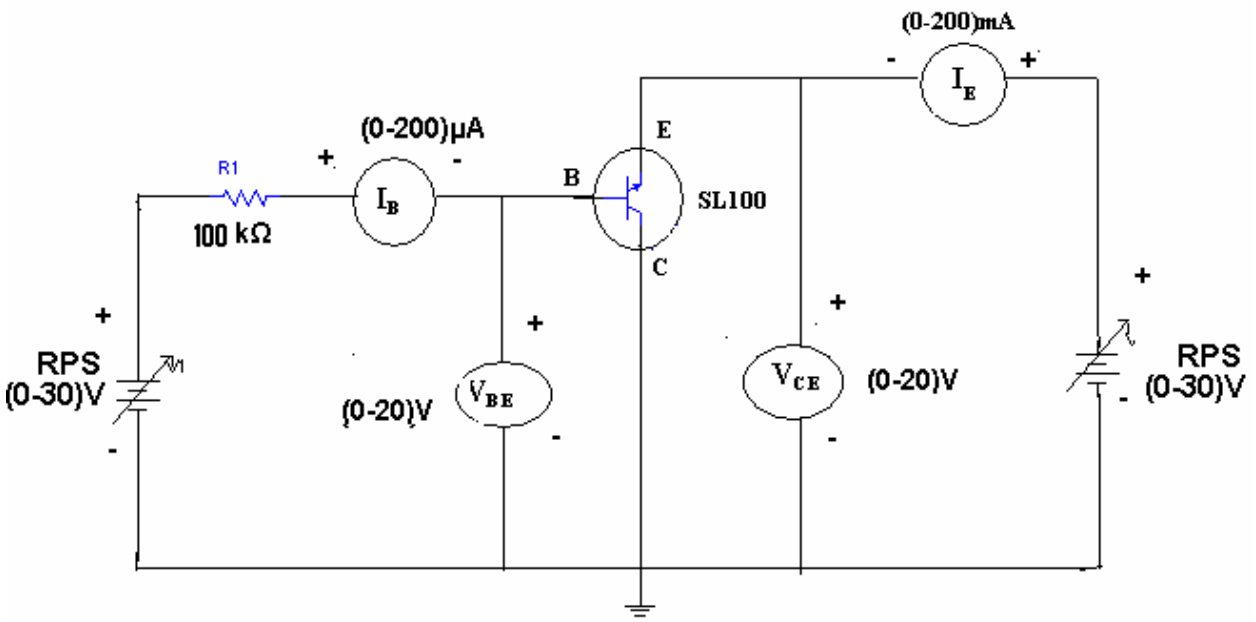
THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In emitter follower configuration, input voltage is applied between base and ground terminals and out put is taken across the emitter and collector terminals.

The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased.

The output characteristics are drawn between I_E and V_{CE} at constant I_B. the emitter current varies with V_{CE} unto few volts only. After this the emitter current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_E is always constant and is approximately equal to I_B.

CIRCUIT DIAGRAM:



PROCEDURE:

INPUT CHARECTERSTICS:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 2V and note down values of V_{CB} for each value of I_B
3. Change V_{CE} to 10 V and repeat the above step.
4. Disconnect the voltmeter from input circuit.
5. plot the graph between V_{CB} and I_B for constant V_{CE}

OUTPUT CHARACTERSTICS:

1. Connect the circuit as per the circuit diagram
2. With I_B set at 0μA, vary V_{CE} and note down the corresponding I_E value.
3. Set I_B at 40μA, 80μA and repeat the above step.
4. Plot the output characteristics between V_{CE} and I_E for constant I_B.

OBSERVATIONS:

INPUT CHARACTERISTICS:

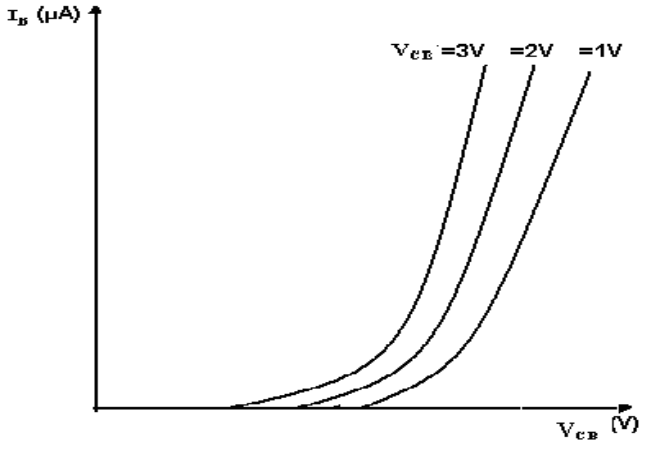
S.NO	V_{CE} = 2V		V_{CE} = 4V		V_{CE} = 10 V	
	V_{CB}(V)	I_B(µA)	V_{CB}(V)	I_B(µA)	V_{CB}(V)	I_B(µA)

OUT PUT CHAREACTARISTICS:

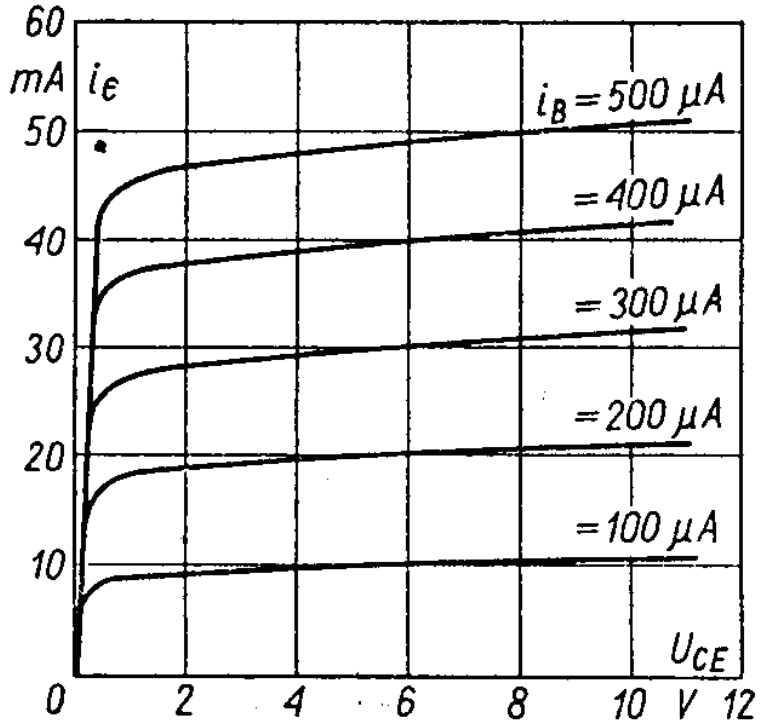
S.NO	I_B = 0 µA		I_B = 30 µA		I_B = 40 µA	
	V_{CE}(V)	I_E(mA)	V_{CE}(V)	I_E(mA)	V_{CE}(V)	I_E(mA)

MODEL GRAPHS:

INPUT CHARACTERSTICS:



OUTPUT CHARECTERSTICS:



PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor
2. Meters should be connected properly according to their polarities

VIVA QUESTIONS:

1. What are the input and output impedances of CC configuration?
2. Identify various regions in the output characteristics?
3. Why CC configuration is preferred for buffering?
4. What is the phase relation between input and output?
5. Draw diagram of CC configuration for PNP transistor?
6. What are the applications of CC configuration?

6. Characteristics of JFET

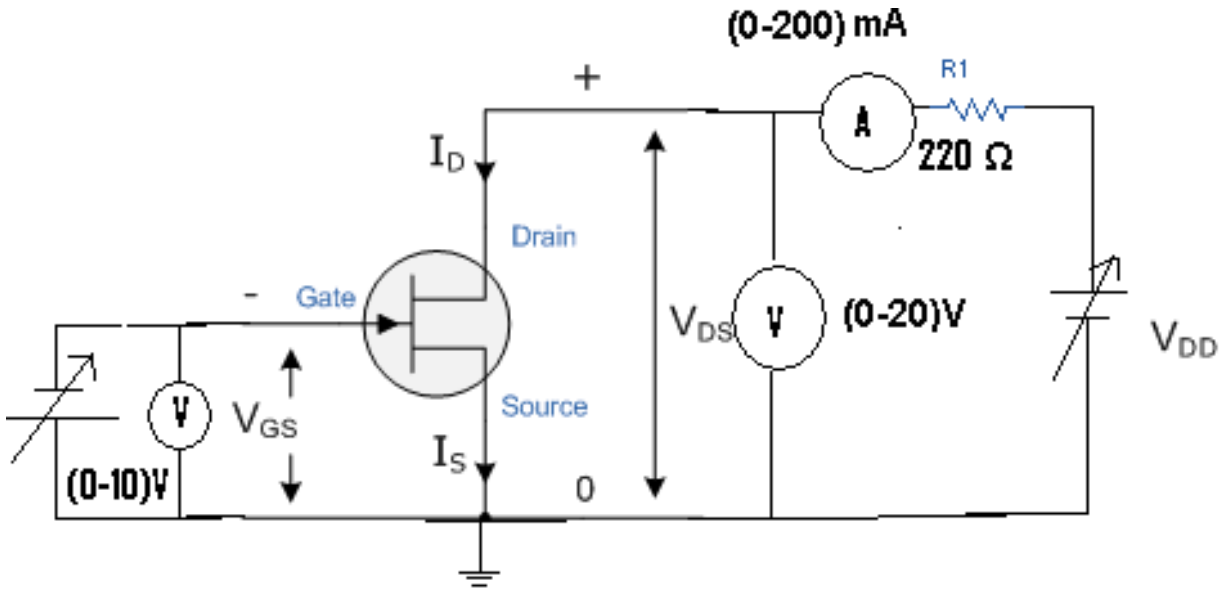
AIM: 1. To obtain the drain and transfer characteristics of the given JFET transistor.

2. To calculate r_d, g_m and μ from the curves obtained.

APPARATUS:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	JFET transistor BFW10	Refer Appendix A	1
2	Resistor	220 ohm	1
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-200 mA)	1
5	Voltmeter	(0-20 V)	2
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Keeping V_{GS} as 0V, vary V_{DS} in steps of 0.1V from 0 to 1 V and in steps of 2V from 1 to 15V.
3. Note down the drain current Id for each step.
4. Now set V_{GS} to -1V, -2V and -3V and repeat the above steps for each V_{GS} value, record the readings in the table.
5. Keep V_{DS} at 4V and vary V_{GS} in steps of -5V till the drain current I_d is 0. Note I_d value for each value of V_{GS}.
6. With V_{DS} at 8V repeat the above step and record the readings in the table.
7. Plot the drain and transfer characteristics from tabulated readings.

OBSERVATIONS:

Drain Characteristics:

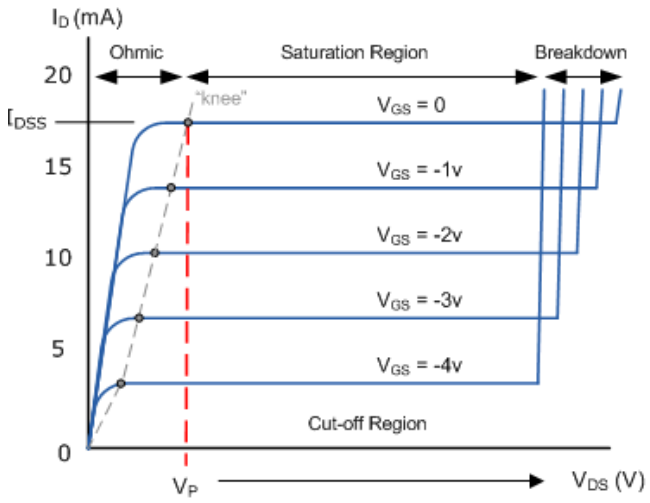
V_{DS}	I_D (V_{GS}=0V)	I_D (V_{GS}=-1V)	I_D (V_{GS}=-2V)

Transfer Characteristics:

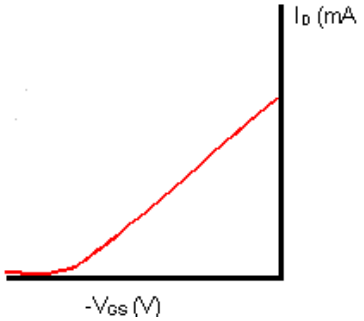
V_{GS}	I_D (V_{DS}=4V)	I_D (V_{DS}=8V)

MODEL GRAPHS:

Drain Characteristics:



Transfer Characteristics:



PRECAUTIONS:

1. The supply voltage should not exceed the rating of the FET.
2. Connections must be tight.

VIVA QUESTIONS:

1. What are the advantages of FET over transistor?
2. Is FET a current controlled device? Explain?
3. What is the operation of a N-channel JFET?
4. Can you compare JFET and a MOSFET?

7. UJT CHARACTERISTICS

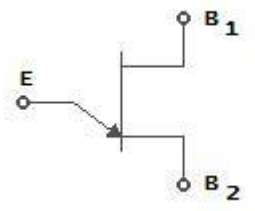
AIM: To observe the characteristics of UJT and to calculate the Intrinsic Stand-Off Ratio (η).

APPARATUS:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	UJT 2N2646	Refer Appendix A	1
2	Resistor	1kΩ, 100Ω	2
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-200 mA)	1
5	Voltmeter	(0-20 V)	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

THEORY:

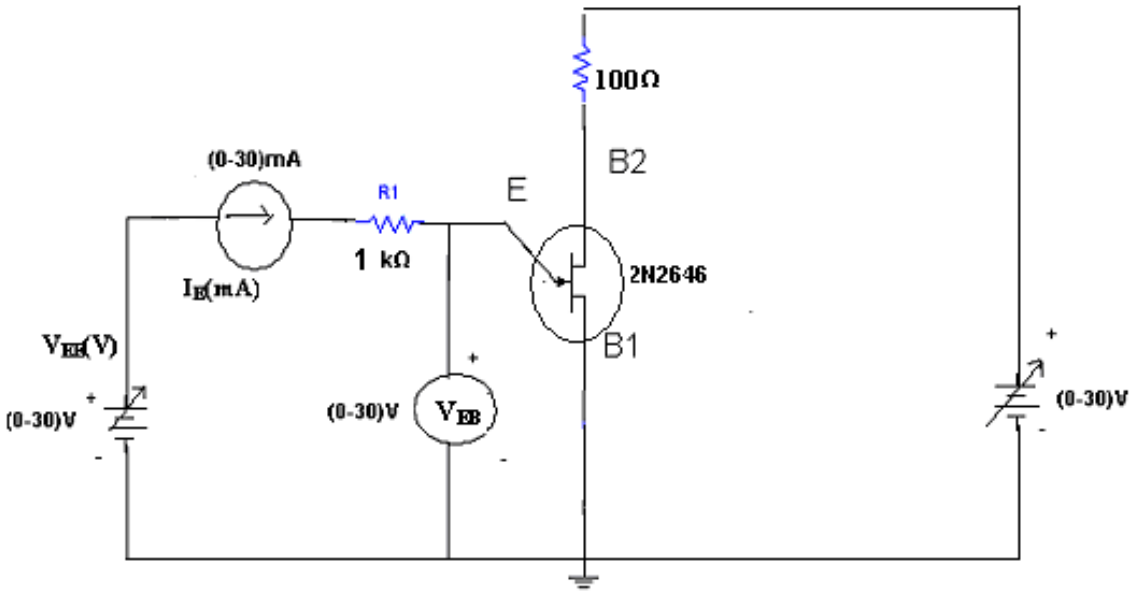
A Unijunction Transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT Unijunction Transistor (UJT) has three terminals an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance.The original unijunction transistor, or UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length. The 2N2646 is the most commonly used version of the UJT.



Circuit symbol

The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits.When the emitter voltage reaches V_p, the current startsto increase and the emitter voltage starts to decrease.This is represented by negative slope of the characteristics which is reffered to as the negative resistance region,beyond the valleypoint ,R_{B1} reaches minimum value and this region,V_{EB} propotional to I_E.

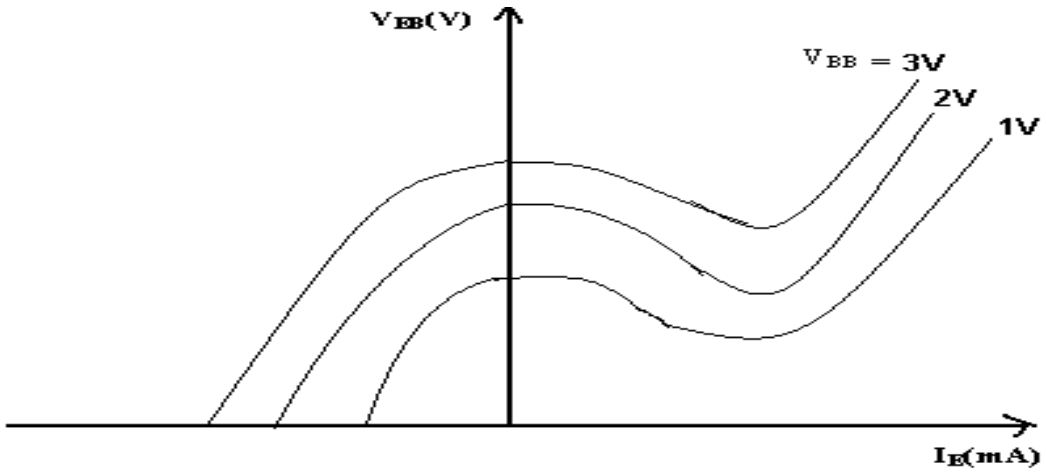
CIRCUIT DIAGRAM



PROCEDURE:

1. Connection is made as per circuit diagram.
2. Output voltage is fixed at a constant level and by varying input voltage corresponding emitter current values are noted down.
3. This procedure is repeated for different values of output voltages.
4. All the readings are tabulated and Intrinsic Stand-Off ratio is calculated using $\eta = (V_p - V_D) / V_{BB}$
5. A graph is plotted between V_{EE} and I_E for different values of V_{BE}.

MODEL GRAPH:



OBSERVATIONS:

V_{BB}=1V		V_{BB}=2V		V_{BB}=3V	
V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)

CALCULATIONS:

$$V_P = \eta V_{BB} + V_D$$

$$\eta = (V_P - V_D) / V_{BB}$$

$$\eta = (\eta_1 + \eta_2 + \eta_3) / 3$$

VIVA QUESTIONS

1. Wha is the symbol of UJT?
2. Draw the equivalent circuit of UJT?
3. What are the applications of UJT?
4. Formula for the intrinsic stand off ratio?
5. What does it indicates the direction of arrow in the UJT?
6. What is the difference between FET and UJT?
7. Is UJT is used an oscillator? Why?
8. What is the Resistance between B_1 and B_2 is called as?
9. What is its value of resistance between B_1 and B_2?
10. Draw the characteristics of UJT?

8. Design and Verification of Transistor Self bias circuit

AIM: To design a self bias circuit and observe stability by changing β of the transistor.

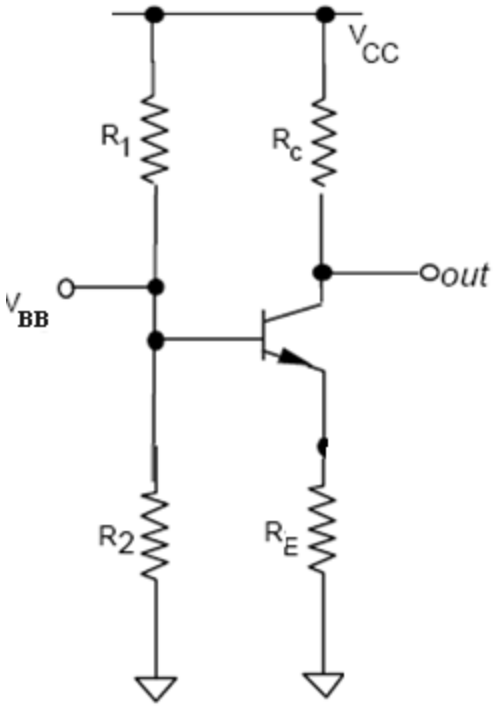
APPARATUS:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Transistors with different β values (SL100)	Refer Appendix A	1
2	Resistor	1kΩ, 100Ω	2
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-200 mA)	1
5	Voltmeter	(0-20 V)	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

Theory:

A self-bias circuit stabilizes the bias point more appropriately than a fixed bias circuit. In this experiment CE configuration is used and a self-bias circuit is designed and verified. By selecting the proper values of R1 and R2, the Q point of the transistor is located in the active region.

CIRCUIT DIAGRAM:



CALCULATIONS:

Given V_{CC}=15V, R_E=220 ohm I_C=4mA V_{CE}=6V V_{BE}=0.6V h_{fe}=229

$R_C=(V_{CC}-V_{CE})/I_C$

$I_B=I_C/\ \beta$

$R_B=\ \beta*R_E/10$

$V_{BB}=I_B*R_B+V_{BE}+(I_B+I_C)R_E$

$R_1=(V_{CC}/V_{BB})*R_B$

$R_2=R_B/(1-V_{BB}/V_{CC})$

PROCEDURE:

1. Assemble the circuit on a bread board with designed values of resistors and transistor.
2. Apply Vcc and measure VCE, VBE and VEE and record the readings in table I.
3. Without changing the values of biasing resistors, change the transistor with other β values and repeat the above steps and record the readings in the table.

OBSERVATIONS:

β value	**V_{CE}**	**V_{BE}**	**V_{EE}**	**$I_C=(V_{CC}-V_{CE})/R_C$**	**$I_E=V_{EE}/R_E$**

PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor
2. Connections must be tight.

VIVA QUESTIONS:

1. What are the advantages of self bias?
2. What are the various other configurations available for bias?
3.

9. DESIGN AND VERIFICATION OF COLLECTOR TO BASE BIAS CIRCUITS

AIM:

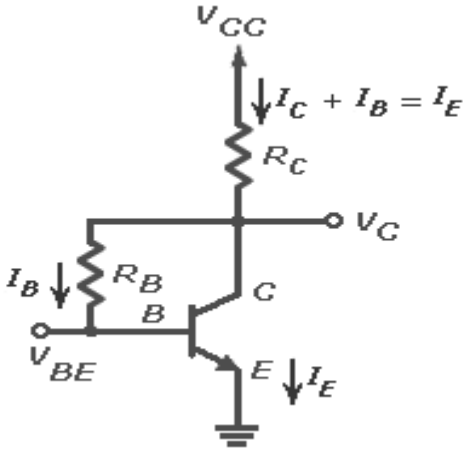
To design a collector to base bias circuit and observe stability by changing β of the given transistor in CE configuration.

APPARATUS:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Transistors with different β values (SL100)	Refer Appendix A	1
2	Resistor	1kΩ, 100Ω	2
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-200 mA)	1
5	Voltmeter	(0-20 V)	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

CIRCUIT DIAGRAM:

Collector-to-base bias circuit



CALCULATIONS:

Collector-to-base bias circuit

Given V_{CC}=15V, I_C=4mA, V_{CE}=6V, V_{BE}=0.6V

$I_C=I_B\beta$

$R_C=(V_{CC}-V_{CE})/(I_B+I_C)$

$R_B=\{(V_{CC}-V_{BE}-I_CR_C)\ \beta\}/I_C\ \} - R_C$

PROCEDURE:

1. Assemble the circuit on breadboard with design values of R_C, R_B and β.
2. Apply V_{CC} and measure V_{CE} and V_{BE} and record the readings in the table.
3. Without changing bias resistors, change the transistors with other β values and repeat the above step.
4. Repeat the above steps using the collector to base bias circuit and tabulate all the readings.

OBSERVATIONS:

Collector to base bias

β value	**V_{CE}**	**V_{BE}**	**$I_C=(V_{CC}-V_{CE})/R_C - I_B$**

PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor
2. Meters should be connected properly according to their polarities

VIVA QUESTIONS:

1. What are the applications of fixed bias configuration?
2. What are the applications of collector to base bias configuration?
3. What are the disadvantages of fixed bias configuration?
4. How to overcome the disadvantages of fixed bias configuration.

10. DESIGN AND VERIFICATION OF FIXED BIAS CIRCUITS

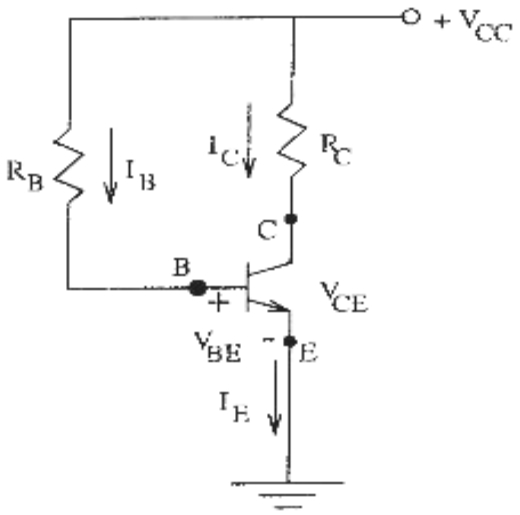
AIM: To design a fixed bias circuit and observe stability by changing β of the given transistor in CE configuration.

APPARATUS:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Transistors with different β values (SL100)		1
2	Resistor	1kΩ, 100Ω	2
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-200 mA)	1
5	Voltmeter	(0-20 V)	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

CIRCUIT DIAGRAM:

Fixed Bias Circuit



CALCULATIONS:

Fixed Bias Circuit

Given V_{CC}=15V, I_C=4mA, V_{CE}=6V, V_{BE}=0.6V

$I_C=I_B\beta$

$R_B=(V_{CC}-V_{BE})/I_B$

$R_C=(V_{CC}-V_{CE})/I_C$

PROCEDURE:

5. Assemble the circuit on breadboard with design values of R_C, R_B and β.
6. Apply V_{CC} and measure V_{CE} and V_{BE} and record the readings in the table.
7. Without changing bias resistors, change the transistors with other β values and repeat the above step.
8. Repeat the above steps using the collector to base bias circuit and tabulate all the readings.

OBSERVATIONS:

Fixed Bias

β value	V_{CE}	V_{BE}	$I_C=(V_{CC}-V_{CE})/R_C$

PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor
2. Meters should be connected properly according to their polarities

VIVA QUESTIONS:

1. What are the applications of fixed bias configuration?
2. What are the disadvantages of fixed bias configuration?

11. voltage regulator using BJT

Aim: To verify the source regulation characteristics for the series voltage regulator using BJT

Apparatus:

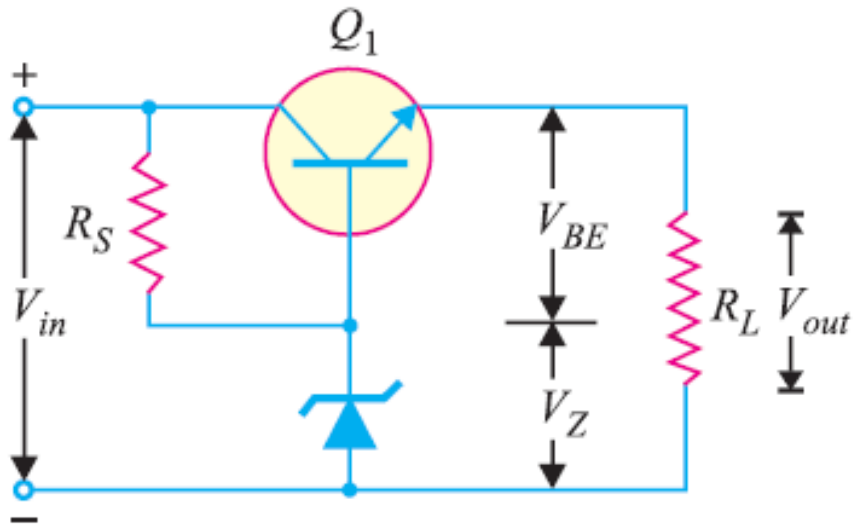
S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Transistors with different β values (SL100)	Refer Appendix A	1
2	Zener Diode BZ7	Refer Appendix A	1
3	Resistor	1kΩ, 100Ω	2
4	Regulated Power Supply	(0 – 30V),1A	2
5	Ammeters	(0-200 mA)	1
6	Voltmeter	(0-20 V)	1
7	Cathode Ray Oscilloscope	(0 – 20MHz)	1

Theory:

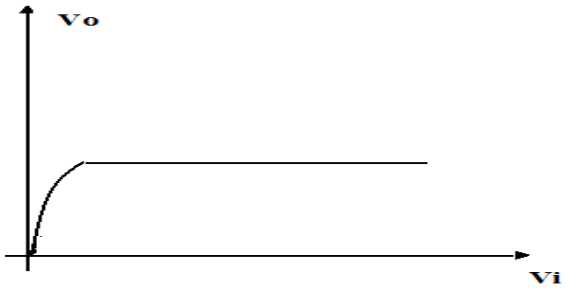
A voltage regulator is designed to automatically 'regulate' voltage level. It basically steps down the input voltage to the desired level and keeps that in that same level during the supply. This makes sure that even when a load is applied the voltage doesn't drop.

Voltage regulators find their applications in computers, alternators, power generator plants where the circuit is used to control the output of the plant. Voltage regulators may be classified as electromechanical or electronic. It can also be classified as AC regulators or DC regulators.

Circuit Diagram:



Model wave forms:



Procedure:

1. Connect the circuit as per the circuit diagram
2. Change the RPS voltage at different instants and note down the corresponding output voltmeter readings
3. Plot the graph between input voltage and output voltage readings.

Tabular colums:

S.No	Vi	Vo

Precautions:

1. Avoid loose connections
2. Keep the input series resistance with a value of 1 k ohms.

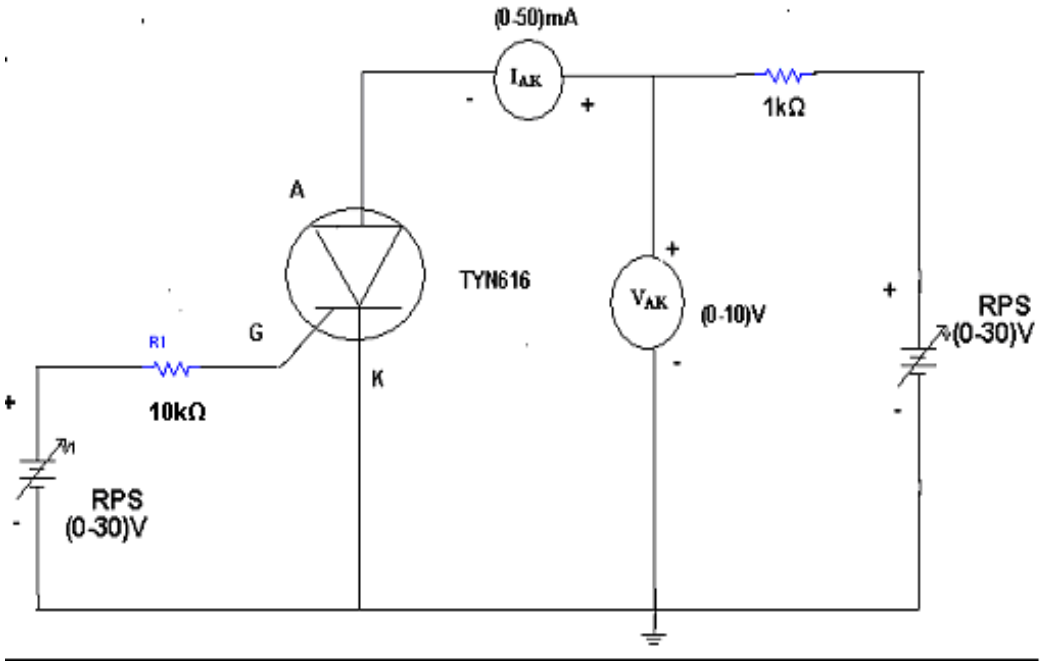
12. CHARACTERISTICS of SILICON-CONTROLLED RECTIFIER (SCR)

AIM: To draw the V-I Characteristics of SCR.

APPARATUS:

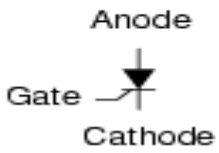
S.No	Equipment/Component Name	Specifications/Value	Quantity
1	SCR (TYN616)	Refer Appendix F	1
2	Resistor	10kΩ, 1kΩ	2
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-50) μA	1
5	Voltmeter	(0-20 V)	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

CIRCUIT DIAGRAM:



THEORY:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists os 3 junctions J_1, J_2, J_3 the J_1 and J_3 operate in forward direction and J_2 operates in reverse direction and three terminals called anode A, cathode K , and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode.



Schematic symbol

- When gate is open, no voltage is applied at the gate due to reverse bias of the junction J_2 no current flows through R_2 and hence SCR is at cutt off. When anode voltage is increased J_2 tends to breakdown.
- When the gate positive,with respect to cathode J_3 junction is forward biased and J_2 is reverse biased .Electrons from N-type material move across junction J_3 towards gate while holes from P-type material moves across junction J_3 towards cathode. So gate current starts flowing ,anode current increaase is in extremely small current junction J_2 break down and SCR conducts heavily.

- When gate is open thee break over voltage is determined on the minimum forward voltage at which SCR conducts heavily. Now most of the supply voltage appears across the load resistance. The holding current is the maximum anode current gate being open , when break over occurs.

PROCEDURE:

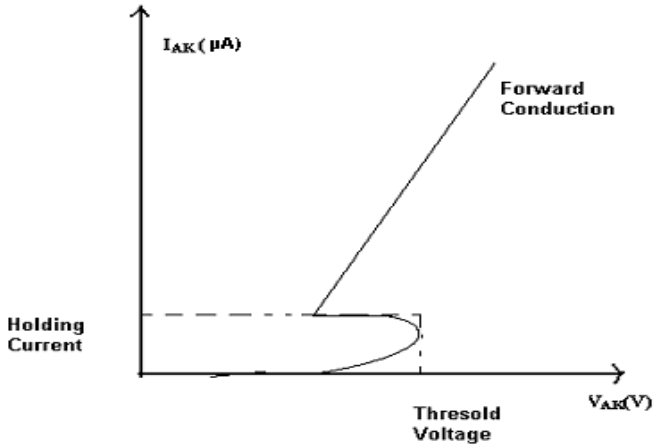
1. Connections are made as per circuit diagram.
2. Keep the gate supply voltage at some constant value

3. Vary the anode to cathode supply voltage and note down the readings of voltmeter and ammeter.Keep the gate voltage at standard value.
4. A graph is drawn between V_{AK} and I_{AK} .

OBSERVATION

V_{AK}(V)	I_{AK} (µA)

MODEL WAVEFORM:



VIVA QUESTIONS

1. What the symbol of SCR?
2. IN which state SCR turns of conducting state to blocking state?
3. What are the applications of SCR?
4. What is holding current?
5. What are the important type's thyristors?
6. How many numbers of junctions are involved in SCR?
7. What is the function of gate in SCR?
8. When gate is open, what happens when anode voltage is increased?
9. What is the value of forward resistance offered by SCR?
10. What is the condition for making from conducting state to non conducting state?

13. STUDY OF CRO

AIM: To observe front panel control knobs and to find amplitude, time period and frequency for given waveforms.

APPARATUS:

CRO

Function generator and probes

PROCEDURE

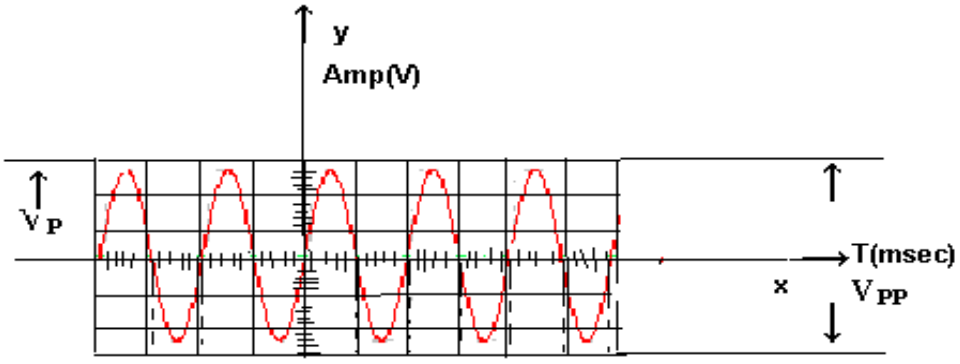
1. Understand the significance of each and every knob on the CRO.
2. From the given function generator feed in a sinusoidal wave and adjust the time base knob and the amplitude knob to observe the waveform as a function of time.
3. Measure the time period and amplitude (peak to peak) of the signal. Find the frequency and verify if the same frequency is given fro the function generator.
4. Observe two waveforms simultaneously on the two channels of a CRO.
5. Repeat the above steps for pulse and triangular waveforms.
6. Report the readings and the waveforms taken.

MEASUREMENTS:

Amplitude = no. of vertical divisions * Volts/div.

Time period = no. of horizontal divisions * Time/div. Frequency=(1/T)Hz

MODEL GRAPHS:



APPLICATIONS OF CRO:

1. Measurement of current
2. Measurement of voltage
3. Measurement of power
4. Measurement of frequency
5. Measurement of phase angle
6. To see transistor curves
7. To trace and measuring signals of RF, IF and AF in radio and TV.
8. To trace visual display of sine waves.

VIVA Questions:

1. How do you measure frequency using the CRO?

2. Can you measure signal phase using the CRO?

3. Suggest a procedure for signal phase measurement using the data from CRO?

4. Can you comment on the wavelength of a signal using CRO>

5. How many channels are there in a CRO?

6. Can you measure DC voltage using a CRO?

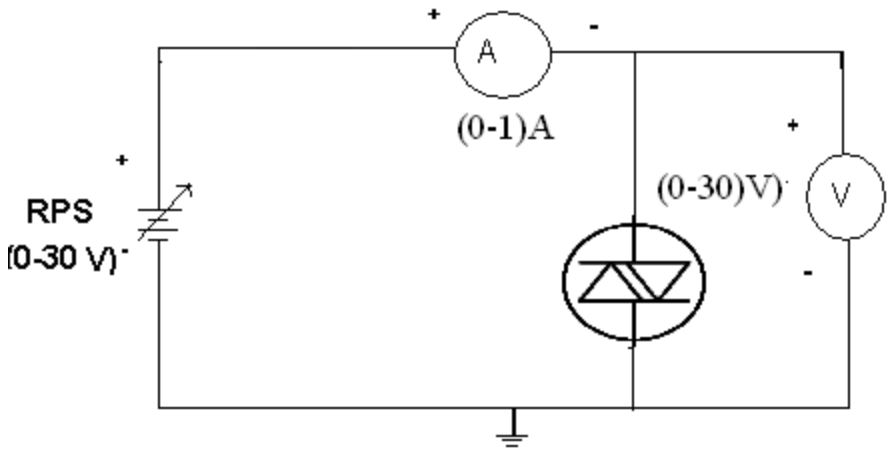
14. Characteristics of DIAC

AIM: To obtain the V-I characteristics of the given DIAC device.

APPARATUS:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	DIAC ST34BRP	Refer Appendix G	1
2	Resistor	1kΩ, 100Ω	2
3	Regulated Power Supply	(0 – 30V),1A	1
4	Ammeter	(0-200 mA)	
5	Voltmeter	(0-20 V)	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1 1

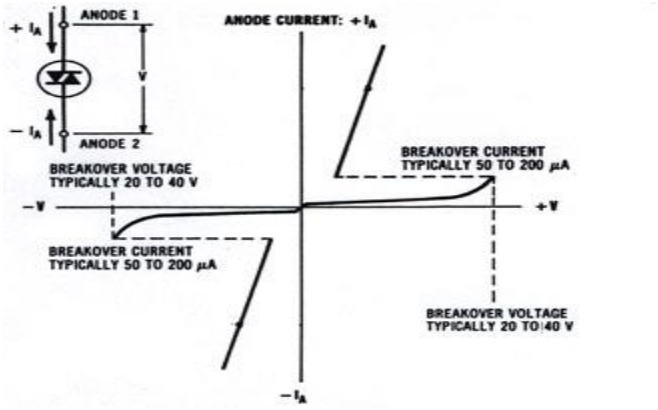
CIRCUIT DIAGRAM:



THEORY:

DIAC is a diode that can work on AC. The DIAC has symmetrical breakdown characteristics. The leads are interchangeable. It turns on around 30V. While conducting, it acts like a low resistance with a drop of around 3V. When not conducting, it acts like an open switch.

MODEL GRAPH:



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Change the voltage V_{12} in steps till 30V and observe V_{B01}, the start of break over voltage. Observe the conduction of PnPn .
3. Change the voltage V_{12} in steps in the negative direction till -30V and observe V_{B02}, the start of break over voltage. Observe the conduction of PnPn' .
4. The characteristics are tabulated and plotted.

OBSERVATIONS:

V-I Characteristics:

V_a (V)	I_a

PRECAUTIONS:

1. The break down condition must be properly verified.
2. Connections must be tight.

VIVA QUESTIONS:

1. What are the applications of DIAC?
2. Why is DIAC a gateless TRIAC?
3. When does the DIAC conduct?
4. How many terminals are present in a DIAC?
5. Do you notice a similarity of operation as a Shockley diode? If so how?

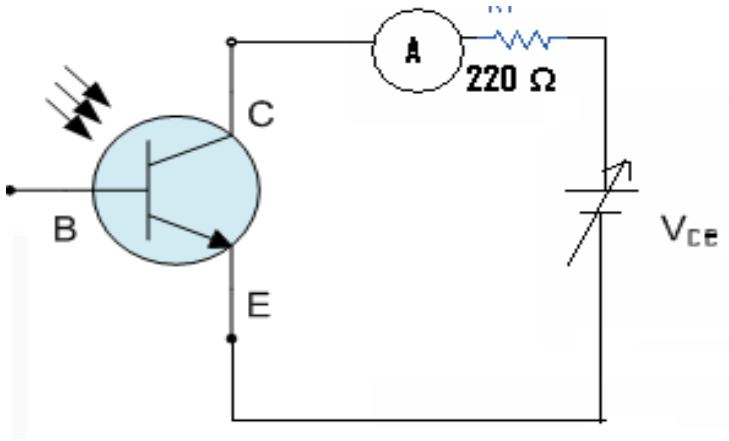
15. Characteristics of Phototransistor

AIM: To obtain the V-I characteristics of the given photo transistor.

APPARATUS:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Photo transistor IR 3MM 935NM	Refer Appendix H	1
2	Resistor	220 ohm	1
3	Regulated Power Supply	(0 – 30V),1A	2
4	Ammeters	(0-200 mA)	1
5	Cathode Ray Oscilloscope	(0 – 20MHz)	1

CIRCUIT DIAGRAM:



THEORY:

The photo transistor is a 3 terminal device which gives an electrical current as output if an input light excitation is provided. It works in reverse bias. When reverse biased along with the reverse bias current I_{CO}, the light current I_L is also added to the total output current. The amount of current flow depends on the input light intensity given as excitation. Phototransistor is basically a photodiode with amplification and operates by exposing its base region to the light source. Phototransistor light sensors operate the same as photodiodes except that they can provide current gain and are much more sensitive than the photodiode with currents are 50 - 100 times greater

than that of the standard photodiode. Phototransistors consist mainly of a bipolar NPN transistor with the collector-base PN-junction reverse-biased. The phototransistor's large base region is left electrically unconnected and uses photons of light to generate a base current which in turn causes a collector to emitter current to flow.

PROCEDURE:

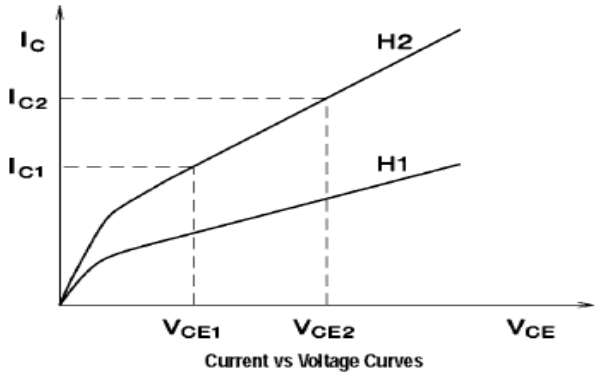
1. Connect the circuit as per the circuit diagram.
2. Keep the input light excitation fixed. Then vary the V_{ce} in steps of 1V till the maximum voltage rating of the transistor is reached and then note down the corresponding values of $I_{c.}$
3. Tabulate the readings. For various values of input excitation record the values of Vce and Ic and plot the characteristics of the photo transistor.

OBSERVATIONS:

V-I Characteristics:

V_{ce} (V)	I_c (mA)

MODEL GRAPH:



Current vs Voltage Curves

PRECAUTIONS:

1. The photo transistor must be given a proper excitation for a reasonable current flow.
2. Connections must be tight.

VIVA QUESTIONS:

1. What are the applications of phototransistor?
2. When does the photo transistor conduct?
3. What is the input excitation in a photo transistor?

REFERENCES

1. A. Anand Kumar, Pulse and Digital Circuits, PHI
2. David A. Bell, Solid State Pulse circuits, PHI
3. D.Roy Choudhury and Shail B.Jain, Linear Integrated Circuits, 2nd edition, New Age International.
4. James M. Fiore, Operational Amplifiers and Linear Integrated Circuits: Theory and Application, WEST.
5. J.Milliman and H.Taub, Pulse and digital circuits, McGraw-Hill
6. Ramakant A. Gayakwad, Operational and Linear Integrated Circuits, 4th edition, PHI.
7. Roy Mancini, OPAMPs for Everyone, 2nd edition, Newnes.
8. S. Franco, Design with Operational Amplifiers and Analog Integrated Circuits, 3rd edition, TMH.
9. William D. Stanley, Operational Amplifiers with Linear Integrated Circuits, 4th edition, Pearson.
10. www.analog.com
11. www.datasheetarchive.com
12. www.ti.com

APPENDIX – A

Data Sheets

PN DIODE:

Type No	1N4007
Max. Peak Inverse Volts	50
Max RMS Supply Volts	35
Maximum Forward Voltage @ 1Ampere, DC @ 75^0 C	1.1 Volts,Peak
Maximum Reverse DC Current @PIV @ 25^0 C	10µA
Maximum Dynamic Reverse Current @PIV @75^0 C	30µA,Average

Zener Diode:

PRIMARY CHARACTERISTICS		
PARAMETER	VALUE	UNIT
V_Z range nom.	3.3 to 75	V
Test current I_{ZT}	3.3 to 76	mA
V_Z specification	Thermal equilibrium	
Circuit configuration	Single	

ORDERING INFORMATION			
DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL	MINIMUM ORDER QUANTITY
1N4728A to 1N4761A	1N4728A to 1N4761A -series-TR	5000 per 13" reel	25 000/box
1N4728A to 1N4761A	1N4728A to 1N4761A-series-TAP	5000 per ammopack (52 mm tape)	25 000/box

PACKAGE				
PACKAGE NAME	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
DO-41 (DO-204AL)	approx. 310 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

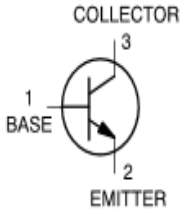
ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Power dissipation	Valid provided that leads at a distance of 4 mm from case are kept at ambient temperature t_p = 10 ms	P_{tot}	1300	mW
Zener current		I_Z	P_V/V_Z	mA
Thermal resistance junction to ambient air	Valid provided that leads at a distance of 4 mm from case are kept at ambient temperature t_p = 10 ms	R_{thJA}	110	K/W
Junction temperature		T_j	175	°C
Storage temperature range		T_{stg}	-65 to +175	°C
Forward voltage (max.)	I_F = 200 mA	V_F	1.2	V

Transistor:

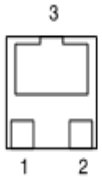
General Purpose Transistors

NPN, 65 V, 100 mA

NST846MTWFT



The NST846MTWFT is designed for general purpose amplifier applications. It is housed in an ultra−compact DFN1010−3 with wettable flanks, recommended for the automotive industry's optical inspection methods. The transistor is ideal for low−power surface mount applications where board space and reliability are at a premium.



XDFNW3
CASE 521AC

MARKING DIAGRAM

46 = Specific Device Code
M = Month Code

Features

- Wettable Flank Package for Optimal Automated Optical Inspection (AOI)
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	65	Vdc
Collector−Base Voltage	V_{CBO}	80	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous	I_C	100	mA
Collector Current − Peak	I_{CM}	200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction−to−Ambient (Note 1)	$R_{\theta JA}$	220	°C/W
Total Power Dissipation per Device @T_A = 25°C (Note 1)	P_D	570	mW
Junction and Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C

1. Per JESD51−7 with standard PCB footprint and 2 oz. Cu.

ORDERING INFORMATION

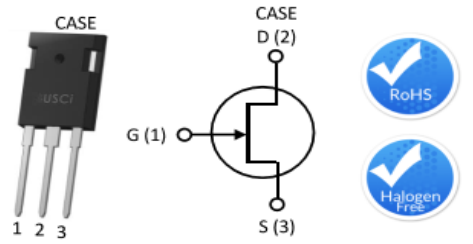
Device	Package	Shipping†
NST846MTWFTBG	XDFNW3 (Pb−Free)	3000 / Tape & Reel
NSVT846MTWFTBG	XDFNW3 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

JFET:

Description

United Silicon Carbide, Inc offers the high-performance G3 SiC normally-on JFET transistors. This series exhibits ultra-low on resistance ($R_{DS(ON)}$) and gate charge (Q_G) allowing for low conduction and switching loss. The device normally-on characteristics with low $R_{DS(ON)}$ at V_{GS} = 0 V is also ideal for current protection circuits without the need for active control, as well as for cascode operation.



Part Number	Package	Marking
UJ3N120070K3S	TO-247-3L	UJ3N120070K3S

Features

- Typical on-resistance $R_{DS(on),typ}$ of 70mΩ
- Voltage controlled
- Maximum operating temperature of 175°C
- Extremely fast switching not dependent on temperature
- Low gate charge
- Low intrinsic capacitance
- RoHS compliant

Typical Applications

- Over current protection circuits
- DC-AC inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-20 to +3	V
		AC (1)	-20 to +20	
Continuous drain current (2)	I_D	T_C = 25°C	33.5	A
		T_C = 100°C	24.5	A
Pulsed drain current (3)	I_{DM}	T_C = 25°C	85	A
Power dissipation	P_{tot}	T_C=25°C	254	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	°C

(1) +20V AC rating applies for turn-on pulses <200ns applied with external R_G > 1Ω.
(2) Limited by $T_{J,max}$
(3) Pulse width t_p limited by $T_{J,max}$

UJT:

Electrical Characteristics: (T_A = +25°C unless other specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Intrinsic Standoff Ratio	η	V_{B2B1} = 10V, Note 3	0.70	–	0.85	
Interbase Resistance	R_{BB}		4.0	6.0	9.1	kΩ
Interbase Resistance Temperature Coefficient	αR_{BB}		0.1	–	0.9	%/°C
Emitter Saturation Voltage	$V_{BE1(sat)}$	V_{B2B1} = 10V, I_E = 50mA, Note 4	–	2.5	–	V
Modulated Interbase Current	$I_{B2(Mod)}$	V_{B2B1} = 10V, I_E = 50mA	–	15	–	mA
Emitter Reverse Current	I_{EB2O}	V_{B2E} = 30V, I_{B1} = 0	–	0.005	1.0	μA
Peak–Point Emitter Current	I_P	V_{B2B1} = 25V	–	1.0	5.0	μA
Valley–Point Current	I_V	V_{B2B1} = 20V, R_{B2} = 100Ω, Note 4	4.0	7.0	–	mA
Base–One Peak Pulse Voltage	V_{OB1}		5.0	8.0	–	V

SCR (Silicon Controlled Rectifier):

Maximum Ratings (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Peak Repetitive Off–State Voltage (Note 1) (– 40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open)	MCR16NG	V_{DRM}, V_{RRM}	800	V
On-State RMS Current (180° Conduction Angles; T_C = 80°C)		$I_{T\ (RMS)}$	16	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, T_J = 125°C)		I_{TSM}	160	A
Circuit Fusing Consideration (t = 8.3 ms)		I^2t	106	A^2sec
Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec, T_C = 80°C)		P_{GM}	5.0	W
Forward Average Gate Power (t = 8.3 msec, T_C = 80°C)		$P_{G\ (AV)}$	0.5	W
Forward Peak Gate Current (Pulse Width ≤ 1.0 μsec, T_C = 80°C)		I_{GM}	2.0	A
Operating Junction Temperature Range		T_J	-40 to 125	°C
Storage Temperature Range		T_{stg}	-40 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. $V_{(BR)R}$ and $V_{(BR)D}$ for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

Thermal Characteristics

Rating		Symbol	Value	Unit
Thermal Resistance	Junction–to–Case (AC) Junction–to–Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds		T_L	260	°C

Electrical Characteristics - OFF (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Repetitive Forward or Reverse Blocking Current ($V_{AK} = V_{DRM} = V_{RRM}$; Gate Open)	T_J = 25°C	I_{DRM}, I_{RRM}	-	-	0.01	mA
	T_J = 125°C		-	-	2.0	mA

Electrical Characteristics - ON (T_J = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward On–State Voltage (Note 2) (I_{TM} = 32 A)	V_{TM}	–	–	1.7	V
Gate Trigger Current (Continuous dc) (V_D = 12 V; R_L = 100 Ω)	I_{GT}	2.0	10	20	mA
Holding Current (Anode Voltage = 12 V, Initiating Current = 200 mA, Gate Open)	I_H	4.0	25	40	mA
Latch Current (V_D = 12 V, I_G = 200 mA)	I_L	–	30	60	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω)	V_{GT}	0.5	0.65	1.0	V

Dynamic Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Critical Rate of Rise of Off–State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, Gate Open, T_J = 125°C)	dv/dt	100	300	–	V/μs
Critical Rate of Rise of On–State Current (I_{PK} = 50 A, Pw = 30 μsec, diG/dt = 1 A/μsec, Igt = 50 mA	di/dt	–	–	50	A/μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test; Pulse Width ≤ 2.0 msec, Duty Cycle ≤ 2%.