Lab Code:20ECL503

Linear Integrated Circuits Lab Manual

Department of Electronics & Communication Engineering

Bapatla Engineering College :: Bapatla

(Autonomous)

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Bapatla Engineering College :: Bapatla
(Autonomous)

Vision

- To build centers of excellence, impart high quality education and instill high standards of ethics and professionalism through strategic efforts of our dedicated staff, which allows the college to effectively adapt to the ever changing aspects of education.

- To empower the faculty and students with the knowledge, skills and innovative thinking to facilitate discovery in numerous existing and yet to be discovered fields of engineering, technology and interdisciplinary endeavors.

Mission

- Our Mission is to impart the quality education at par with global standards to the students from all over India and in particular those from the local and rural areas.

- We continuously try to maintain high standards so as to make them technologically competent and ethically strong

individuals who shall be able to improve the quality of life and economy of our country.

Bapatla Engineering College :: Bapatla

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Department of Electronics and Communication Engineering

Vision

To produce globally competitive and socially responsible Electronics and Communication Engineering graduates to cater the ever changing needs of the society.

Mission

- To provide quality education in the domain of Electronics and Communication Engineering with advanced pedagogical methods.

- To provide self-learning capabilities to enhance employability and entrepreneurial skills and to inculcate human values and ethics to make learners sensitive towards societal issues.

- To excel in the research and development activities related to Electronics and Communication Engineering.

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Department of Electronics and Communication Engineering

Program Educational Objectives (PEO's)

PEO-I: Equip Graduates with a robust foundation in mathematics, science and Engineering Principles, enabling

them to excel in research and higher education in Electronics and Communication Engineering and related fields.

PEO-II: Impart analytic and thinking skills in students to develop initiatives and innovative ideas for Start-ups, Industry and societal requirements.

PEO-III: Instill interpersonal skills, teamwork ability, communication skills, leadership, and a sense of social, ethical, and legal duties in order to promote lifelong learning and Professional growth of the students.

Program Outcomes (PO's)

Engineering Graduates will be able to:

PO1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7.Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. Individual and Teamwork: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. Life-long learning: Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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Department of Electronics and Communication Engineering

Program Specific Outcomes (PSO's)

PSO1: Develop and implement modern Electronic Technologies using analytical methods to meet current as well as future industrial and societal needs.

PSO2: Analyze and develop VLSI, IoT and Embedded Systems for desired specifications to solve real world complex problems.

PSO3: Apply machine learning and deep learning techniques in communication and signal processing.

Linear Integrated Circuits Lab

III B.Tech – I Semester (Code: 20ECL52)

Lectures	0	Tutorial	0	Practical	3	Credits	1
Continuous Internal Assessment			50	Semester End Examination (3 Hours)			50

Prerequisites: None

Course Objectives: Students will

- Perform experiments based on 741 Op-Amp.
- Realize the circuits related to the applications of 555 Timer.
- Test the functionality of voltage regulators using IC 723.
- Measure the lock range of IC 556 (Phase Locked Loop).

Course Outcomes: After studying this course, the students will be able to

CO 1	Design different linear applications of Op-Amp like Adder, Integrator, Active filters
CO 2	Demonstrate different non-linear applications of operational amplifiers likeOscillators, waveform generators, DAC
CO 3	Construct multivibrator and oscillator circuits using IC555 and IC556 andperform measurements of frequency and time
CO 4	Design and demonstrate a Variable Voltage Regulator using IC 723

Mapping of Course Outcomes with Program Outcomes & Program Specific

Outcomes															
	PO's												PSO's		
CO	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1		2	3	3									2		
CO2	2			3									2		
CO3	2			3									2		
CO4	2		3	3									2		
AVG	2	2	3	3									2		

LIST OF LAB EXPERIMENTS

1. Measurement of Op-amp Parameters.
2. Applications of Op-amp (Adder, Subtractor, Integrator, Differentiator).
3. Design of Full Wave Rectifier using Op-Amp.
4. Design of Low Frequency Oscillators using Op-Amp (Wein Bridge & RC Phase Shift Oscillators).
5. Waveform Generation using Op-amp (Square, Triangular).
6. Instrumentation Amplifier using Op-Amp IC741.
7. Design and Verification of Schmitt Trigger using Op-Amp IC741.
8. Design of Active Filters (First Order LPF&HPF).
9. Design of State Variable Filter using Op-Amps.
10. Applications of 555 Timer ICs (Astable, Monostable, Schmitt Trigger).

11. PLL using IC 565.
12. Design of Fixed Voltage Regulators.
13. Design of Variable Voltage Regulator using IC 723.
14. Design of VCO using IC 566.
15. Design of 4 bit DAC using R-2R Ladder Network.

NOTE: A minimum of 10 (Ten) experiments have to be Performed and recorded by the candidate to attain eligibility for Semester End Examination.

1. Measurement of op-Amp parameters

Aim: To measure the op-Amp parameters such as

1. Input Bias Current
2. Input Offset current
3. Input offset voltage
4. Slew Rate

S. No	Equipment/ Component Name	Specifications/ Value	Quantity
1.	IC μA741	Refer Appendix B	1
2.	Capacitors	0.01μF	1
3.	Resistors	100Ω,	2
4.	Resistor	10kΩ	1
5.	Regulated Power Supply	(0 – 30V),1A	2
6.	Function Generator	(0.1 – 1MHz), 20V $_{pp}$	1
7.	Digital Multimeter	3 digit display	1

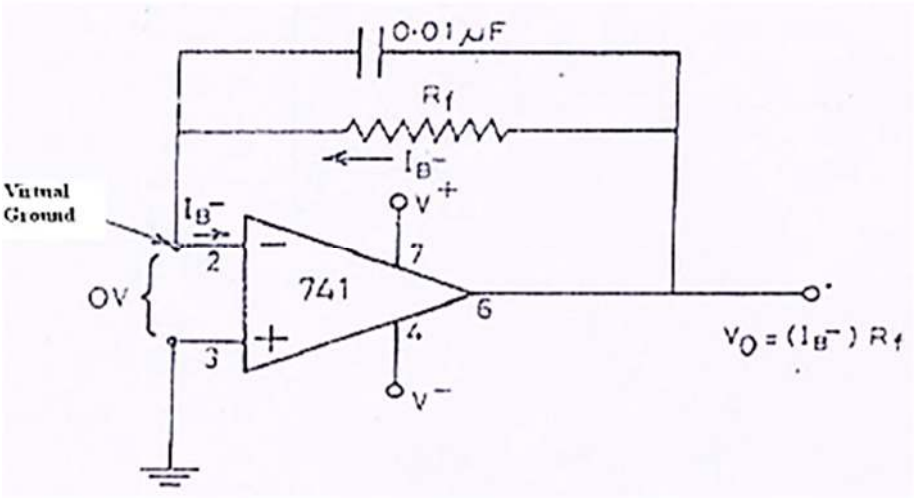
Procedure:

1. Set up the circuit shown in fig 1.1 to measure I_B^-
2. Set up the circuit shown in fig 1.2 to measure I_B^+
3. Select the large resistor (in MΩ) and measure the output voltage.
4. Calculate $I_{B-} = V_0/R_f$
5. Calculate $I_{B+} = V_0/R$
6. Calculate $I_B = (I_{B+} + I_{B-})/2$, $I_{io} = |I_{B+} - I_{B-}|$
7. set up the circuit shown in fig 1.3 to measure offset current, $I_{io} = Vo/Rf$.
8. Set up the circuit shown in fig 1.4 for

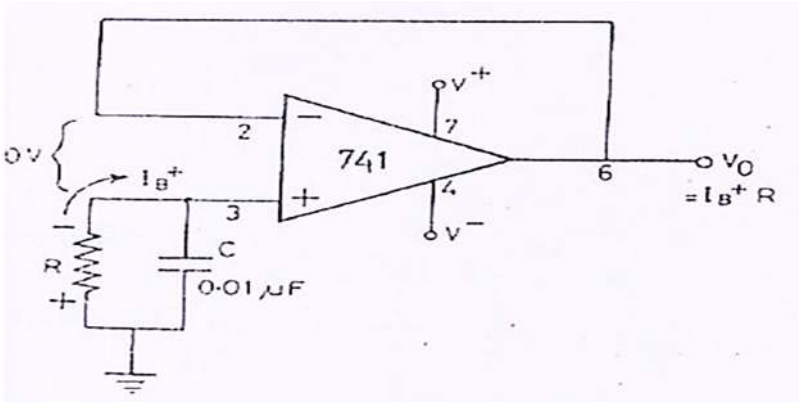
$$V_0 = \left(1 + \frac{R_f}{R_i}\right) V_{io} + R_f I_{io} \approx \left(1 + \frac{R_f}{Ri}\right) V_{io}$$

9. Set up the circuit shown in fig 1.5, adjust the input sine wave signal generator so that the output is 1V peak sine wave at I KHz. Slowly increase the input signal Frequency until the output gets just distorted. Then Calculate slew rate, $SR = (2\pi f Vm / 106)\ V/\mu S$ where V_m = peak output amplitude in volts and f = frequency in Hz.
10. Now give a square-wave input and repeat step-9 increase the i/p frequency slowly until the Output is just barely a triangular wave. The SR = (dV_0 /dt) V/μs where V_0 is the change in the Output voltage amplitude in volts, dt = time required for change in dV_0.

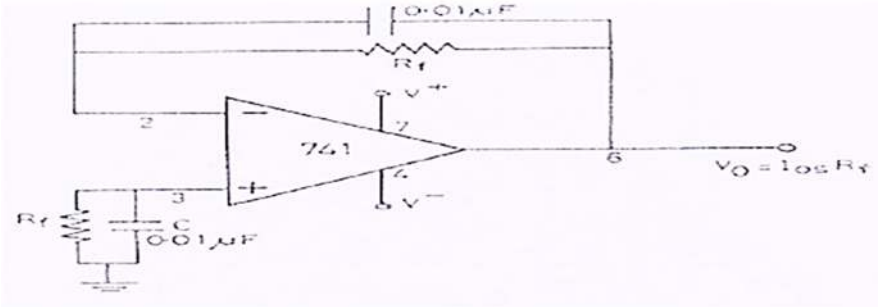
1. Measurement of Inverting input Bias current : Fig (1.1)



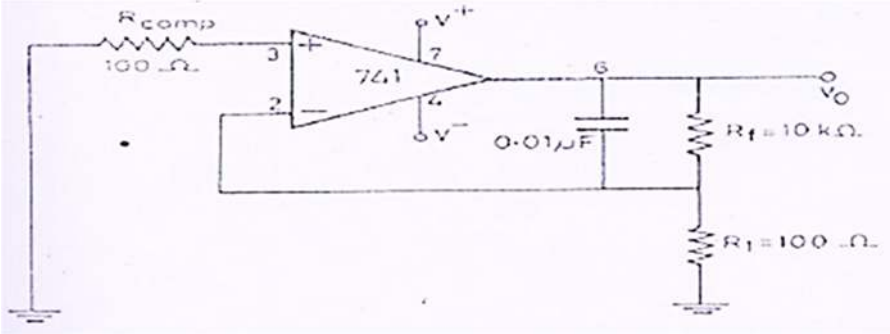
2. Measurement of Non-Inverting input Bias current : fig(1.2)



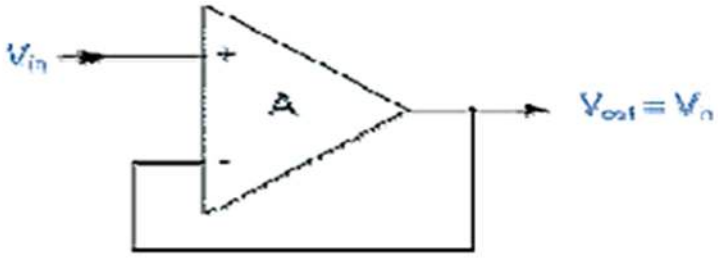
3. Measurement of Offset current : Fig (1.3)



4. Measurement of offset voltage : Fig(1.4)



5. Measurement of slew rate: Fig(1.5)



Precautions:

1. Don't disturb the set up while performing experiment.
2. Take the readings without parallax error

Result:

2. Applications of Op-Amp.

Aim:

To design adder, subtractor for the given signals by using operational amplifier and to design integrator and differentiator for a given input (square/sine)

Apparatus required:

S. No	Equipment / Component Name	Specifications / Value	Quantity
1.	IC μA741	Refer Appendix B	1
2.	Capacitors	0.1μF, 0.01μF	Each one
3.	Resistors	159Ω, 1.5kΩ	Each one
4.	Resistor	1kΩ	4
5.	Regulated Power Supply	(0 – 30V),1A	2
6.	Function Generator	(0.1 – 1MHz), 20V pp	1
7.	Dual Channel CRO	(0 – 20MHz)	1
8.	Digital Multimeter	3 digit display	1

Theory:

Adder*:*

A two input summing amplifier may be constructed using the inverting mode. The adder can be obtained by using either inverting or non-inverting mode. Here the inverting mode is used. So the inputs are applied through resistors to the inverting terminal and non-inverting terminal is grounded. This is called “virtual ground”, i.e. the voltage at that terminal is zero. The gain of this summing amplifier is 1, any scale factor can be used for the inputs by selecting proper external resistors.

Subtractor:

The subtractor circuit, input signals can be scaled to the desired values by selecting appropriate values for the resistors. When this is done, the circuit is referred to as scaling amplifier. However in this circuit all external resistors are equal in value. So the gain of amplifier is equal to one. The output voltage V_o is equal to the voltage applied to the non-inverting terminal minus the voltage applied to the inverting terminal , hence the circuit is called a subtractor.

Integrator:

In an integrator circuit, the output voltage is the integration of the input voltage. At low frequencies the gain becomes infinite, so the capacitor is fully charged and behaves like an open circuit. The gain of an integrator at low frequency can be limited by connecting a resistor in shunt with capacitor

Differentiator:

It performs the mathematical operation of Differentiation that is it "produces a voltage output which is directly proportional to the input voltage's rate-of-change with respect to time". In other words the faster or larger the change to the input voltage signal, the greater the input current, the greater will be the output voltage change in response, becoming more of a "spike" in shape.

Circuit Diagrams:

Fig 1: Adder

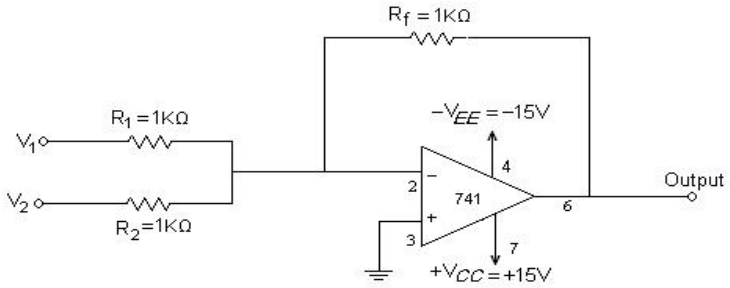


Fig 2: Subtractor

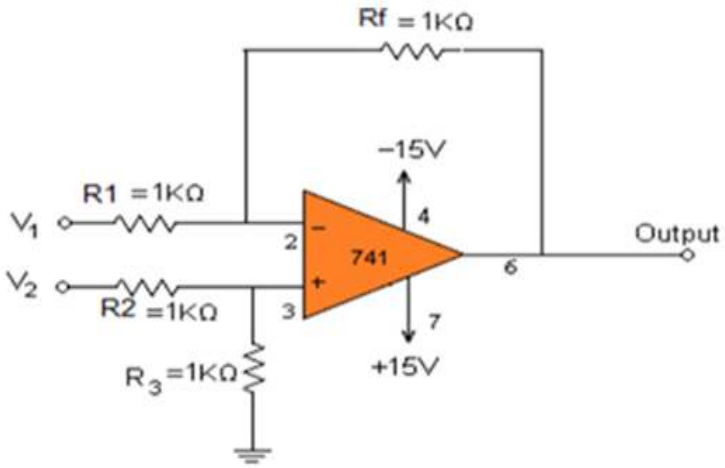


Fig 3: Integrator

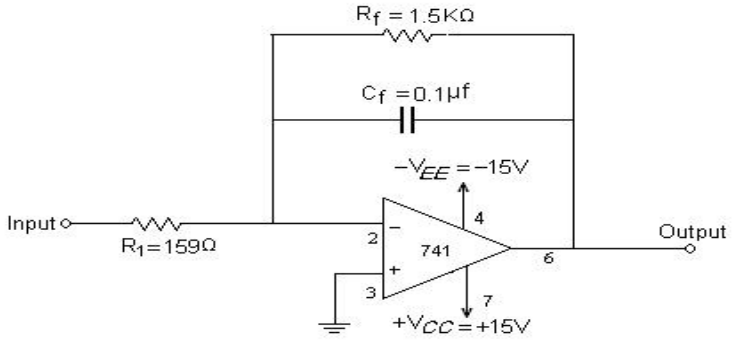
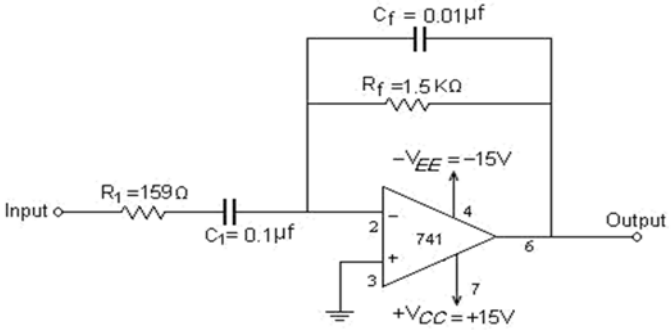


Fig 4: Differentiator



Design equations:

1. **Adder:**
   Output voltage, V_o = - (V_1+V_2)
2. **Subtractor:**
   $V_o = V_2 – V_1$
3. **Integrator:**
   Choose T = $2\pi R_f C_f$
   Where T= Time period of the input signal
   Assume C_f and find R_f
   Select $R_f = 10R_1$

$$V_{O(p-p)} = \frac{-1}{RC}\int_0^{T/2} i_{(p-p)}dt$$

4. **Differentiator:**
   Select given frequency $f_a = 1/(2\pi R_f C_1)$, Assume C_1 and find R_f
   Select $f_b = 10\ f_a = 1/2\pi R_1 C_1$ and find R_1

From $R_1C_1 = R_fC_f$, find C_f

Procedure:

1. Adder:

1. Connect the circuit diagram as shown in Fig 1.
2. Apply the supply voltages of $\pm$15V to pin7 and pin4 of IC741 respectively.
3. Apply the inputs V_1 and V_2 as shown in fig 1.
4. Apply two different signals (DC/AC) to the inputs
5. Vary the input voltages and note down the corresponding output at pin 6 of the IC 741 adder circuit.
6. Notice that the output is equal to the sum of the two inputs.

2. Subtractor:

1. Connect the circuit as shown in Fig 2.
2. Apply the supply voltages of +15V to pin7 and pin4 of IC741 respectively.
3. Apply the inputs V_1 and V_2.
4. Apply two different signals (DC/AC) to the inputs.
5. Vary the input voltages and note down the corresponding output at pin 6 of the IC 741.
6. Notice that the output is equal to the difference of the two inputs.

3. Integrator

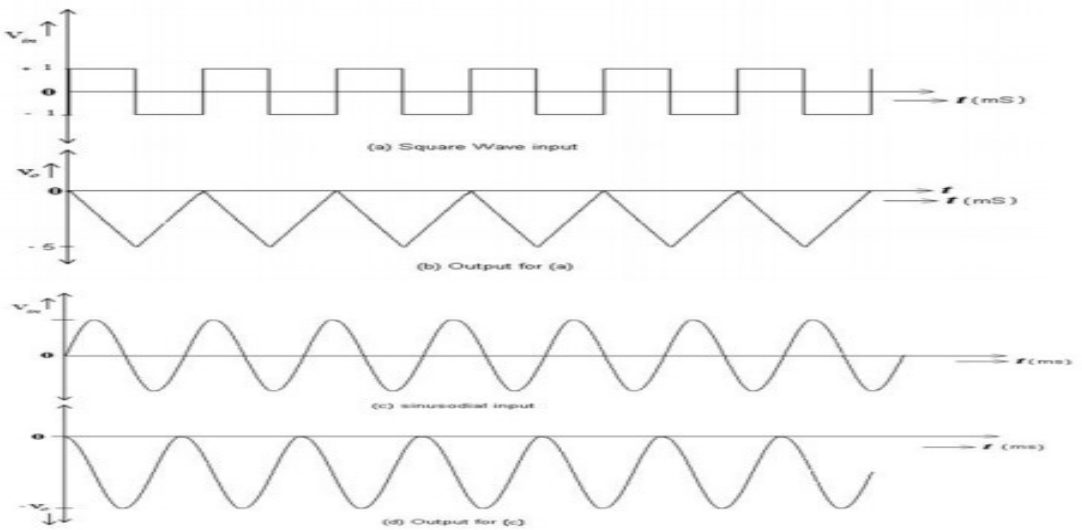
1 Connect the circuit as per the diagram shown in Fig.3
2 Apply a square wave/sine input of 4V(p-p) of 1KHz
3 Observe the o/p at pin 6.
4 Draw input and output waveforms as shown in Fig: 5

4. Differentiator

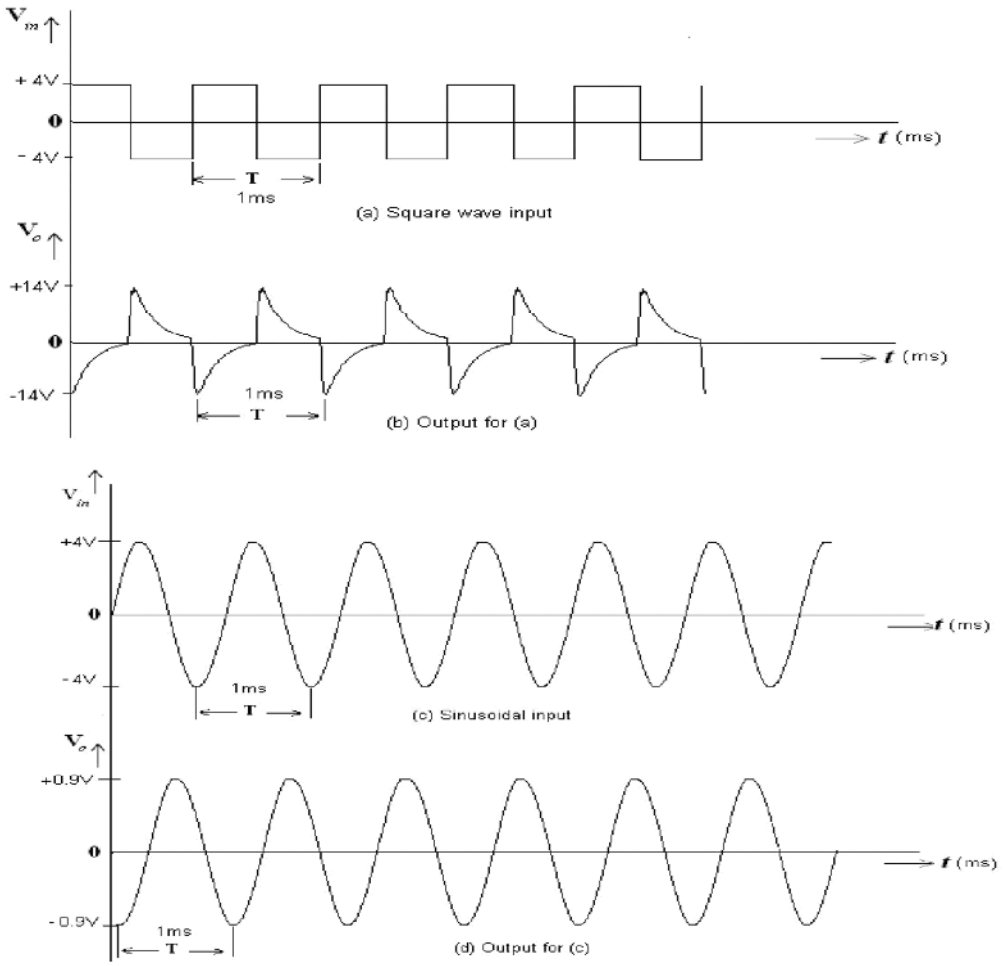
1. Connect the circuit as per the diagram shown in Fig.4
2. Apply a square wave/sine input of 4V(p-p) of 1KHz
3. Observe the output at pin 6
4. Draw the input and output waveforms as shown in Fig:6

Wave Forms:

1. **Input and output waves forms of integrator : Fig (2.5)**



2.Input and output waveforms of differentiator : Fig (2.6)



Sample readings:

1. Adder:

Input V_1	Input V_2	V_o(V)

2. Subtractor:

Input V_1	Input V_2	V_o(V)

3. Integrator:

Input – Square wave		Output – Triangular Wave	
Amplitude (V_{PP}) (V)	Time Period (ms)	Amplitude (V_{PP}) (V)	Time Period (ms)

Input – sine wave		Output – Cosine Wave	
Amplitude (V_{PP}) (V)	Time Period (ms)	Amplitude (V_{PP}) (V)	Time Period (ms)

4. Differentiator:

Input – Square wave		Output – Spike Waves	
Amplitude (V_{PP}) (V)	Time Period (ms)	Amplitude (V_{PP}) (V)	Time Period (ms)

Input – Sine wave		Output – Cosine Wave	
Amplitude (V_{PP}) (V)	Time Period (ms)	Amplitude (V_{PP}) (V)	Time Period (ms)

Model Calculations:

1. **Adder**

   $V_o = - (V_1+V_2)$

   If Input V_1 = 2.5V and V_2= 2.5V, then

   $V_o = - (2.5+2.5) = -5V$.

2. **Subtractor:**

   If Input V_1 = 2.5V and V_2= 12.5V, then V_o = 10V.

3. **Integrator:**

   For T= 1 msec

   $f_a = 1/T = 1$ KHz

   $f_a = 1$ KHz $= 1/(2\pi R_f C_f)$

   Assuming Cf= 0.1μf, R_f is found from $R_f=1/(2\pi f_a C_f)$

   R_f=1.59 K

   $R_f = 10\ R_1$

   R_1= 159 ohms

4. **Differentiator**

   For T = 1 msec

   $f = 1/T = 1$ KHz

   $f_a = 1$ KHz $= 1/(2\pi R_f C_1)$

   Assuming C_1= 0.1μf, R_f is found from $R_f=1/(2\pi f_a C_1)$

   R_f=1.59 K

   $f_b = 10\ f_a = 1/2\pi R_1 C_1$

   for C_1= 0.1μf;

   R_1 =159

Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Result:

3. Design of Full Wave Rectifier using IC 741

Aim:

To design and verify the output of Full Wave Rectifier using IC741

Apparatus Required:

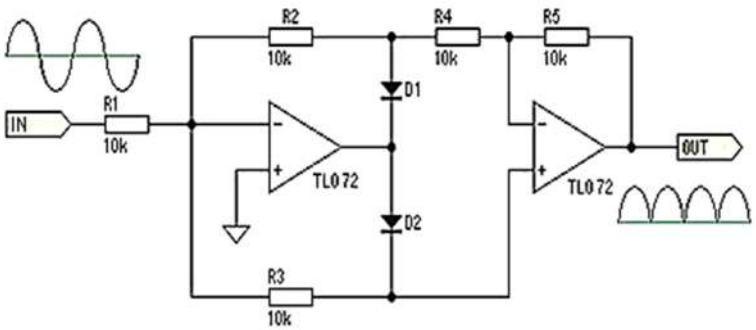
S.No	Equipment/ Component Name	Specifications/ Value	Quantity
1.	IC μA 741	Refer Appendix B	2
2.	IN4007 Diode		2
3.	Resistors	10 KΩ	5
4.	Function Generator	(1Hz- 1MHz), $20V_{pp}$	1
5.	Dual Channel CRO	0 – 20 MHz	1
6.	Regulated Power Supply	(0 – 30V), 1A	2

Theory:

A Full Wave Rectifier is a circuit, which converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. It uses two diodes of which one conducts during one half cycle while the other conducts during the other half cycle of the applied ac voltage.

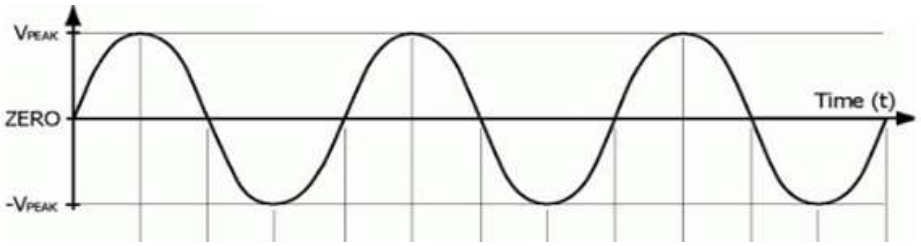
During the positive half cycle of the input voltage, diode D1 becomes Forward biased and D2 becomes Reverse biased. Hence D1 conducts and D2 remains OFF. The load current flows through D1 and the voltage drop across R_L will be equal to the input voltage. During the negative half cycle of the input voltage, diode D1 becomes Reverse biased and D2 becomes Forward biased. Hence D1 remains OFF and D2 conducts. The load current flows through D2 and the voltage drop across R_L will be equal to the input voltage.

Circuit Diagram:

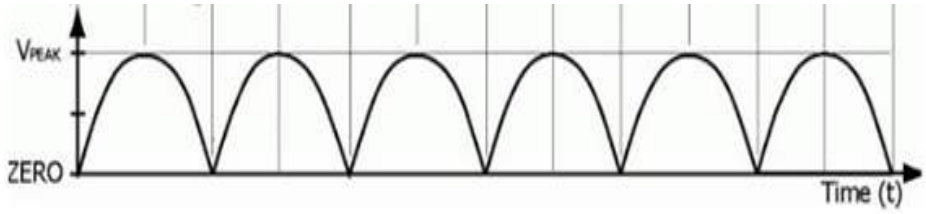


Model Waveforms:

1. **Input Signal:**



2. **Output Signal:**



Procedure:

1. Connect the circuit as shown in figure.
2. Apply a sinusoidal signal of $2V_{PP}$, 1KHz as input waveform from Function generator.
3. Observe the input and output waveforms on CRO.
4. Note down the amplitudes and time periods of input & output waveforms.

Precautions:

- Check the connections before giving the power supply.
- Readings should be taken carefully

Result:

4. Design of Low Frequency Oscillators using Op-amp (Wein Bridge & RC Phase Shift Oscillators)

Aim: To design Wein Bridge & RC Phase shift oscillators using OP-AMP

Apparatus required:

S.No	Equipment/ Component Name	Specifications/ Value	Quantity
1.	IC μA741	Refer Appendix B	2
2.	CRO	0 - 20MHz	1
3.	Capacitors	0.01μF	2
4.	Resistors	3.18 kΩ & 31.8 kΩ	2 & 1
5.	Bread Board		1
6.	Regulated Power Supply	(0 – 30V),1A	2

Theory:

An oscillator is a circuit, which generates an ac output signal without giving any input ac signal. This circuit is usually applied for audio frequencies only. The basic requirement for any oscillator is Amplifier and positive feedback network.

a. Op Amp is used as an amplifier.
b. Passive components such as R- C or L - C combinations are used as feedback network.

To start the oscillation with the constant amplitude, positive feedback is not the only sufficient condition. Oscillator circuit must satisfy the following two conditions known as **Barkhausen** conditions:

1. The first condition is that the magnitude of the loop gain (Aβ) =1 Where A = Amplifier gain and β = Feedback gain.
2. The second condition is that the phase shift around the loop must be 0° or 360° .

1. **Wein Bridge oscillator**

A Wien bridge oscillator is a type of electronic oscillator that generates sine waves. It can generate a low range of frequencies. The frequency of oscillation is given by:

$$f = (1/2\pi RC)$$

The Wien Bridge Oscillator uses a feedback circuit consisting of a

series RC circuit connected with a parallel RC of the same component values producing a phase delay or phase advance circuit depending upon the frequency. At the resonant frequency f_r the phase shift is 0^o. Then for oscillations to occur in a Wien Bridge Oscillator circuit the following conditions must apply:

1. With no input signal the Wien Bridge Oscillator produces output oscillations.
2. The Wien Bridge Oscillator can produce a large range of frequencies.
3. The Voltage gain of the amplifier must be at least 3.
4. The network can be used with a Non-inverting amplifier.
5. The input resistance of the amplifier must be high compared to R so that the RC Networks are not overloaded and alter the required conditions.
6. The output resistance of the amplifier must be low so that the effect of external loading is minimized.
7. Some method of stabilizing the amplitude of the oscillations must be provided because if the voltage gain of the amplifier is too small the desired oscillation will decay and stop and if it is too large the output amplitude rises to the value of the supply rails, which saturates the op-amp and causes the output waveform to become distorted?
8. With amplitude stabilization in the form of feedback diodes, oscillations from the Oscillator can go on indefinitely.

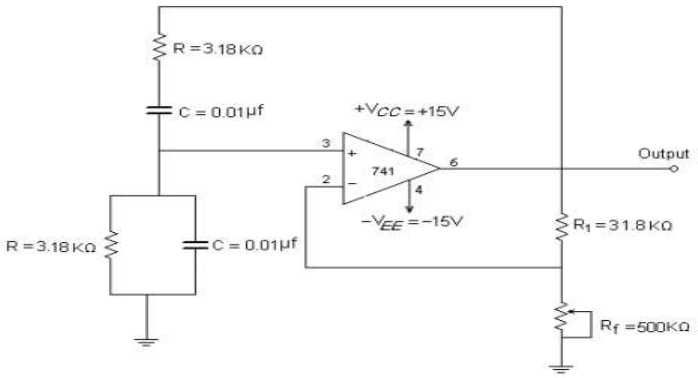
2. RC phase shift oscillator:

Phase-shift oscillator is a simple electronic oscillator. It contains an inverting amplifier, and a feedback filter which 'shifts' the phase of the amplifier output by 180^0 at the oscillation frequency. The filter produces a phase shift that increases with frequency. It must have a maximum phase shift of considerably greater than 180° at high frequencies, so that the phase shift at the desired oscillation frequency is 180°. The most common way of achieving this kind of filter is using three identical cascaded resistor-capacitor filters, which together produce a phase shift of zero at low frequencies, and 270^0 at high frequencies. At the oscillation frequency each filter produces a phase shift of 60^0 and the whole filter circuit produces a phase shift of 180^0 .The frequency of oscillation is given by,

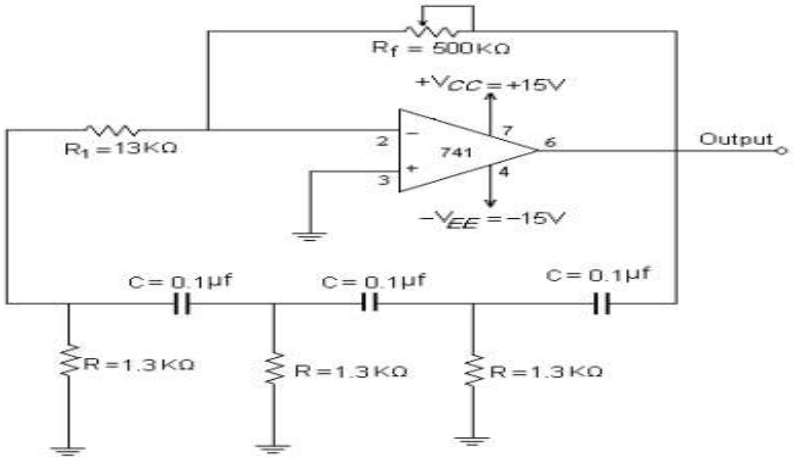
$$f_o = 1/(2\pi RC\sqrt{6})$$

Circuit Diagrams:

1. Wein Bridge oscillator :

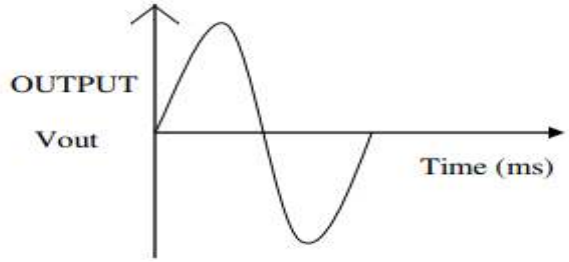


2. RC phase shift oscillator :



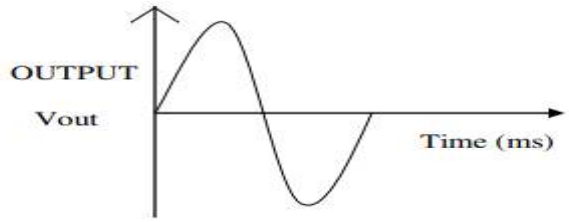
Model Waveforms:

1. Wein Bridge oscillator



Output Waveform

2. RC phase shift oscillator



Output waveform

Design :

1. Wein Bridge Oscillator :

To design a Wein Bridge Oscillator for f_0 = 5KHz

Sol : Formula (f_0)= 1 / (2πRC) and $R_F = 2R_1$

Let C = 0.01μF , then R is found from

R= 1/ (2πf_0 C) = 1 / (2x3.18x 5x 10^3x 0.01x10^{-6}) = 3.18kΩ

Let R_1 = 10R = 31.8kΩ , $R_F = 2R_1$= 63.6KΩ (use 100kΩ potentio meter)

2. RC Phase Shift Oscillator :

To design a RC Phase Shift Oscillator with f_0 = 500Hz

Sol : Formula (f_0)= 1 / (2πRC$\sqrt{6}$) and $R_F = 29R_1$

Let C = 0.1μF , then R is found from

R= 1 / (2πf_0 C$\sqrt{6}$) = 1 / (2x3.18x 500x 0.01x10^{-6}x$\sqrt{6}$) = 1.3kΩ

Let R_1 = 10R = 13kΩ , $R_F = 29R_1$= 169KΩ (use 500kΩ potentio meter)

Procedure:

1. Wein Bridge oscillator:

1. Design the circuit for f =1KHz , calculate R,R_1,and R_F
2. Connect the circuit as shown in the figure with the designed values.
3. Observe the output waveform at pin 6 of op-amp.
4. Note down the amplitude and time period of output waveform.
5. Plot the waveform on a graph sheet.

2. RC phase shift oscillator:

1. Design the circuit for f_0 = 500Hz , calculate R,R_1,and R_F
2. Connect the circuit as shown in the figure with the designed values.
3. Observe the output waveform at pin 6 of op-amp.
4. Note down the amplitude and time period of output waveform.
5. Plot the waveform on a graph sheet.

Precautions:

- Check the connections before giving the power supply.
- Readings should be taken carefully

Result:

5. WAVEFORM GENERATION USING OP-AMP
(SQUARE & TRIANGULAR WAVE FORMS)

Aim:

To generate square and Triangular wave forms by using OP-AMPs.

Apparatus required:

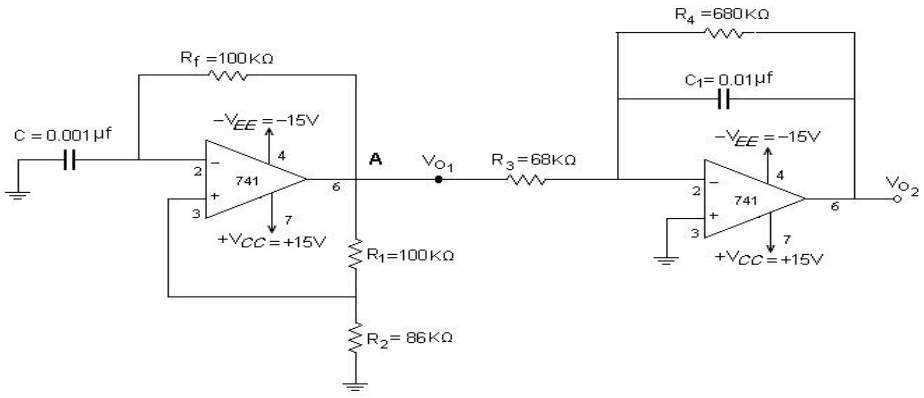
S.No	Equipment/ Component name	Specifications/ Value	Quantity
1	IC μA741	Refer Appendix B	2
2	Capacitors	0.01μF, 0.001μF	Each one
3	Resistors	86kΩ ,68kΩ ,680kΩ	Each one
	Resistors	100kΩ	2
4	Regulated Power supply	(0 – 30V),1A	1
5	Dual Channel CRO	(0 -20MHz)	1

Theory:

Function generator generates waveforms such as sine, triangular, square waves and so on of different frequencies and amplitudes. The circuit shown in Fig1 is a simple circuit which generates square waves and triangular waves simultaneously. Here the first section is a square wave generator and second section is an integrator. When square wave is given as input to integrator it produces triangular wave.

Circuit Diagram:

Fig.1



Model Wave Forms:

Fig (2): Output at 'A' i.e. Square wave

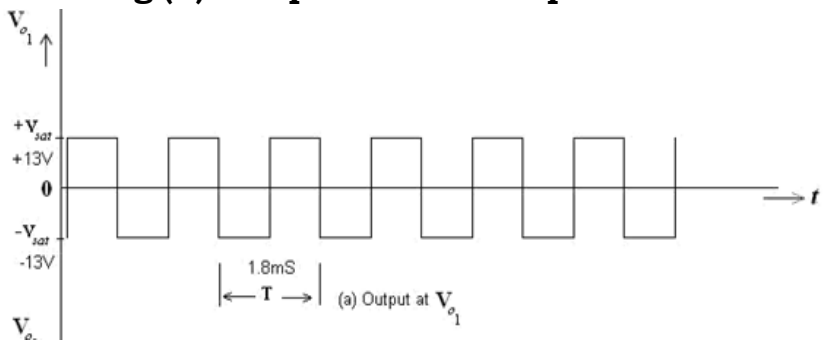
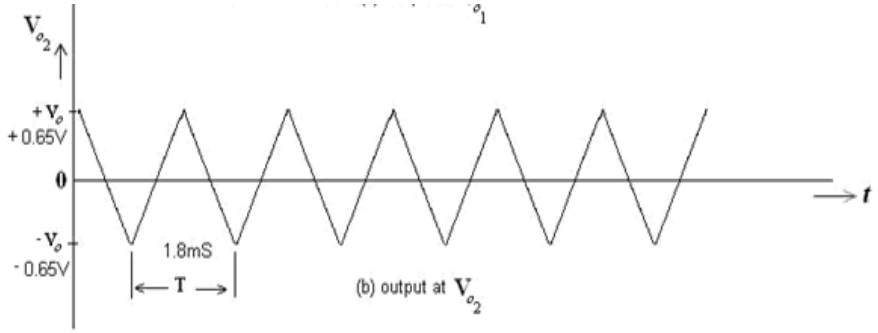


Fig (3): Triangular Output



Design:

Square wave Generator:

$T = 2R_f C \ln \{R_2 / (R_1+R_2)\}$

Assume C to be a fixed value and find R_f for the given time period.

Procedure:

1. Connect the circuit as per the circuit diagram shown in Fig .
2. Obtain square wave at A and Triangular wave at V_o as shown in fig (a) and (b).
3. Draw the output waveforms as shown in fig (a) and (b).

Precautions:

- Check the connections before giving the power supply.
- Readings should be taken carefully.

Result:

6. Instrumentation Amplifier using Op-amp

Aim : To verify the output of the Instrumentation amplifier using IC741

Apparatus Required:

S.No	Equipment/ Component Name	Specifications/ Value	Quantity
1	IC μA741	Refer Appendix B	3
2	Bread Board		1
3	Resistors	10kΩ	5
4	Regulated Power Supply	(0 – 30V),1A	2
5	Digital Multimeter		1

Theory:

An instrumentation amplifier is a type of differential amplifier that has been outfitted with input buffers, which eliminate the need for input impedance matching and thus make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics include very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. Instrumentation amplifiers are used where great accuracy and stability of the circuit both short- and long-term are required.

$$V_o = (V_2 - V_1)\left(1 + 2\frac{R_G}{R_2}\right)\left(\frac{R_f}{R_1}\right) \quad \textbf{6.1}$$

If $R_G = 0\Omega$ then the given instrumentation amplifier becomes subtractor.

$$V_o = (V_2 - V_1) \quad \textbf{6.2}$$

Circuit Diagram:

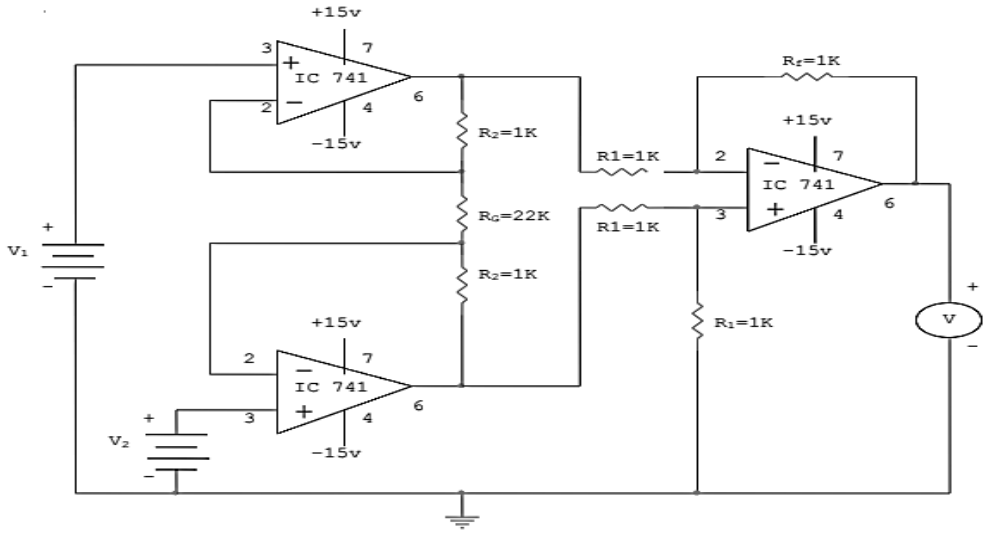


Table:

S.NO.	i/p voltage (V_2)	i/p voltage (V_1)	Theoretical o/p ($V_o=V_2-V_1$)	Practical o/p (V_o)
1	0V	0V	0V	
2	5V	5V	0V	
3	5V	-5V	10V	
4	10V	-10V	$+V_{sat}$ = +14V	
5	10V	10V	0V	
6	-10V	10V	$-V_{sat}$ = -14V	

Procedure:

1. Connect the circuit as shown in figure
2. Calculate the output for different input combinations practically
3. Calculate output theoretically.
4. Compare Theoretical and Practical Values.

Precautions:

- Check the connections before giving the power supply.
- Readings should be taken carefully

Result:

7. Design of Schmitt Trigger using op-amp

Aim: To design and verify the Schmitt trigger circuit using op-amp.

Apparatus required:

S. No	Equipment/ Component name	Specifications/ Value	Quantity
1	IC µA741	Refer Appendix B	1
2	Dual Channel CRO	(0 – 20MHz)	1
3	Resistors	100 Ω	2
		10 KΩ 60 KΩ - Pot	1 1
4	Regulated power supply	(0 -30V),1A	1
5	Function Generator	(0.1 – 1MHz), 20V $_{pp}$	1
6	Bread Board		1

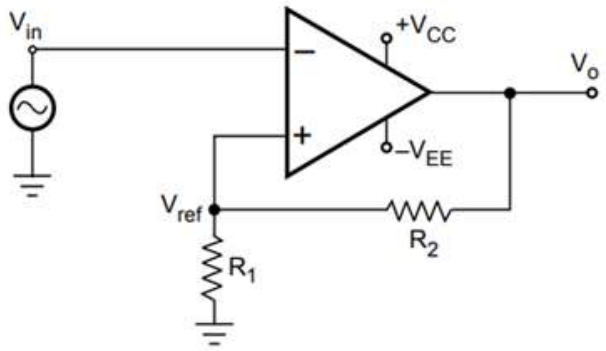
Theory:

The circuit shows an inverting comparator with positive feedback. This circuit converts arbitrary wave forms to a square wave or pulse. The circuit is known as the Schmitt trigger (or) squaring circuit. The input voltage V_{in} changes the state of the output V_o every time it exceeds certain voltage levels called the upper threshold voltage V_{ut} and lower threshold voltage V_{lt}.

1. When V_o= - V_{sat}, the voltage across R_1 is referred to as lower threshold voltage, V_{lt}.
2. When V_o=+V_{sat}, the voltage across R_1 is referred to as upper threshold voltage V_{ut}.

The comparator with positive feedback is said to exhibit hysteresis, a dead band condition.

Circuit Diagram:



Design:

Let V_{ut} = +2V, V_{lt} = - 2V, Vsat = +14V

$V_{ut} = [R_1/(R_1+R_2)](+V_{sat}) = +2V$

$V_{lt} = [R_1/(R_1+R_2)](-V_{sat}) = -2V$

$V_{hy} = V_{utp} - V_{ltp} = 4V$

$= [R_1/(R_1+R_2)] [+V_{sat} – (-V_{sat})]$

$= 2V_{sat} [R_1/(R_1+R_2)] = 4V$

By solving above equations we will get

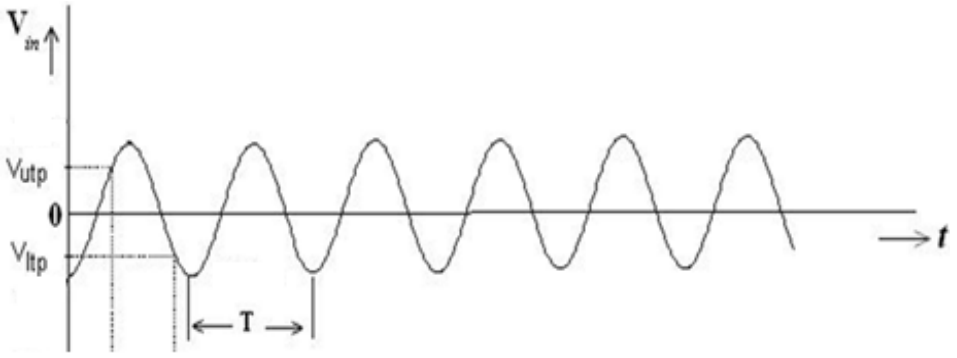
R_1 =10kΩ R_2 = 60kΩ

Procedure:

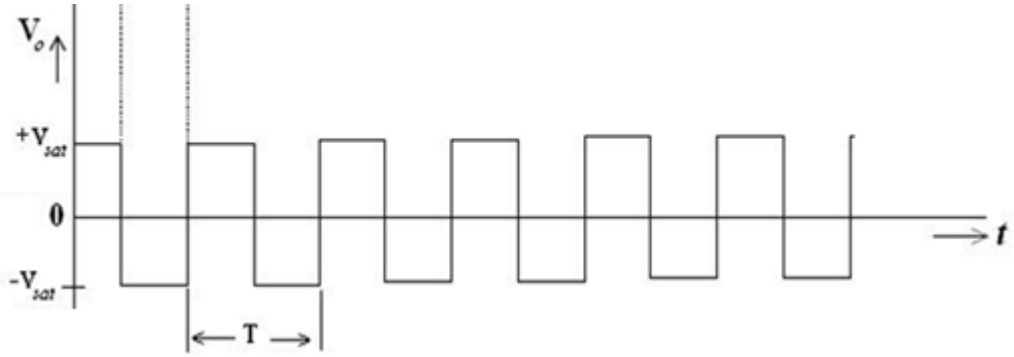
1. Connect the circuit as shown in figure.
2. Apply an arbitrary waveform (sine/triangular) of peak voltage greater than UTP to the input of a Schmitt trigger.
3. Observe the output at pin no.6 of the IC 741 Schmitt trigger circuit by varying the input and note down the amplitude and time period of input and output waveforms.
4. Find the upper and lower threshold voltages (V_{ut}, V_{Lt}) from the output wave form.

Model Wave forms:

1. input wave form (Sine wave)



2.Output waveform (Square wave)



Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Result:

8. Design of Active Filters – First Order LPF& HPF

Aim: To design and obtain the frequency responses of

i) First order Active Low Pass Filter (LPF)

ii) First order Active High Pass Filter (HPF)

Apparatus required:

S.No.	Equipment/ Component name	Specifications/ Value	Quantity
1	IC - μA741	Refer Appendix B	1
2	Resistors	10 kΩ 3.9 kΩ	2 1
3	Capacitor	0.01μF	1
4	Dual Channel CRO	(0 – 20MHz)	1
5	RPS	(0 – 30V),1A	1
6	Function Generator	(1Hz – 1MHz)	1

Theory:

a) LPF:

A LPF allows frequencies from 0 to higher cut of frequency, f_H. At f_H the gain is 0.707 A_{max}, and after f_H gain decreases at a constant rate with an increase in frequency. The gain decreases 20dB each time the frequency is increased by 10. Hence the rate at which the gain rolls off after f_H is 20dB/decade or 6 dB/ octave, where octave signifies a two fold increase in frequency. The frequency $f = f_H$ is called the cut off frequency because the gain of the filter at this frequency is down by 3 dB from 0 Hz. Other equivalent terms for cut-off frequency are - 3dB frequency, break frequency, or corner frequency.

b) HPF:

The frequency at which the magnitude of the gain is 0.707 times the maximum value of gain is called “low cut off frequency”. Obviously, all frequencies higher than f_L are pass band frequencies with the highest frequency determined by the closed –loop band width all of the op-amp.

Circuit diagrams:

Fig 1: Active Low pass filter

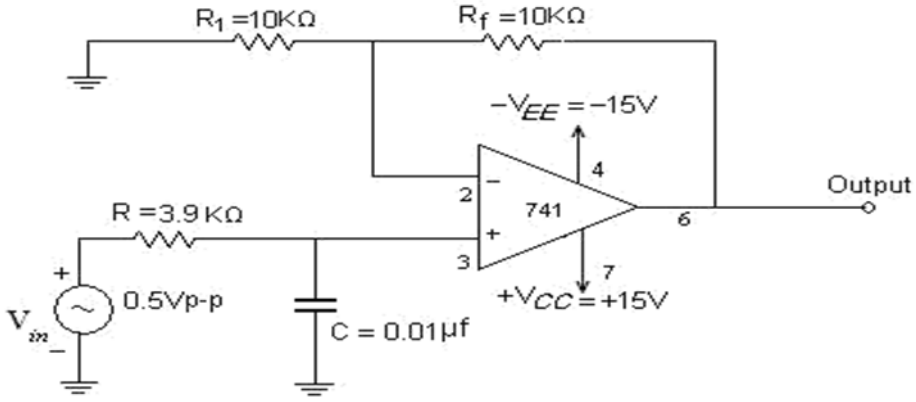
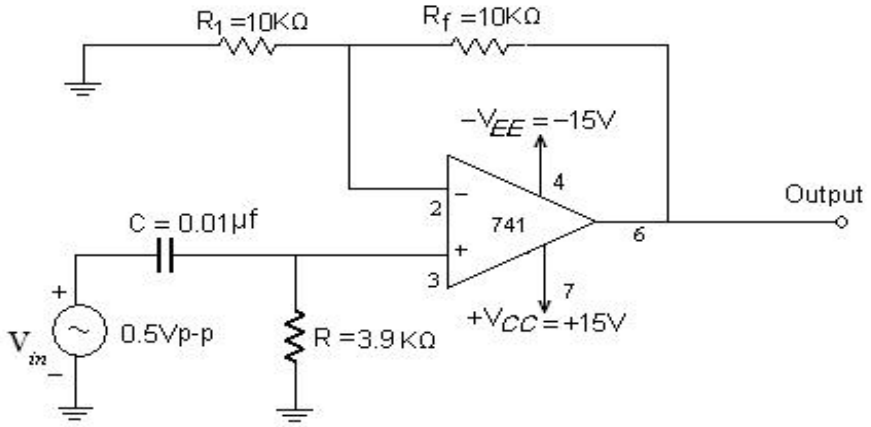


Fig 2: Active High pass filter



Design:

(a) First Order LPF:

To design a LPF for higher cut off frequency f_H = 4 KHz , pass band gain of 2

$f_H = 1/(2\pi RC)$

Assuming C=0.01 μF, the value of R is found from

$R= 1/(2\pi f_H C) = 3.97K\Omega$

The pass band gain of LPF is given by, $A_F = 1+ (R_F / R_1) = 2$

Assuming R_1 =10 KΩ, the value of R_F is found from

$R_F = (A_F -1) R_1 = 10K\Omega$

(b) First Order HPF:

To design a HPF for lower cut off frequency f_L = 4 KHz , pass band gain of 2

$f_L = 1/(2\pi RC)$

Assuming C=0.01 μF, the value of R is found from

$R = 1/(2\pi f_L C) = 3.97K\Omega$

The pass band gain of HPF is given by $A_F = 1 + (R_F / R_1) = 2$

Assuming $R_1 = 10\ K\Omega$, the value of R_F is found from

$R_F = (A_F - 1) R_1 = 10K\Omega$

Procedure:

(a) First Order LPF

1. Connections are made as per the circuit diagram shown in fig 1.
2. Apply sinusoidal wave of constant amplitude (1V) as the input such that op-amp does not go into saturation.
3. Vary the input frequency from 100Hz to 200 KHz and note down the output amplitude at each step as shown in Table (a).
4. Plot the frequency response as shown in fig 3.

(b) First Order HPF

1. Connections are made as per the circuit diagrams shown in fig 2.
2. Apply a sinusoidal wave of constant amplitude (1V) as the input such that op-amp does not go into saturation.
3. Vary the input frequency from 100Hz to 200 KHz and note down the output amplitude at each step as shown in Table (b).
4. Plot the frequency response as shown in fig 4.

Observations:

1. LPF

Input voltage (V_{in}) = 1V

S.No.	Frequency (Hz)	Output Voltage (V_0)	Voltage Gain (V_o/V_i)	Gain In dB = 20Log (V_o/V_i)

2. HPF

Input voltage V_{in} = 1V

S.No.	Frequency (Hz)	Output Voltage (V_0)	Voltage Gain (V_o/V_i)	Gain In dB = 20Log (V_o/V_i)

Model Graphs:

Fig 3: Frequency response characteristics of LPF

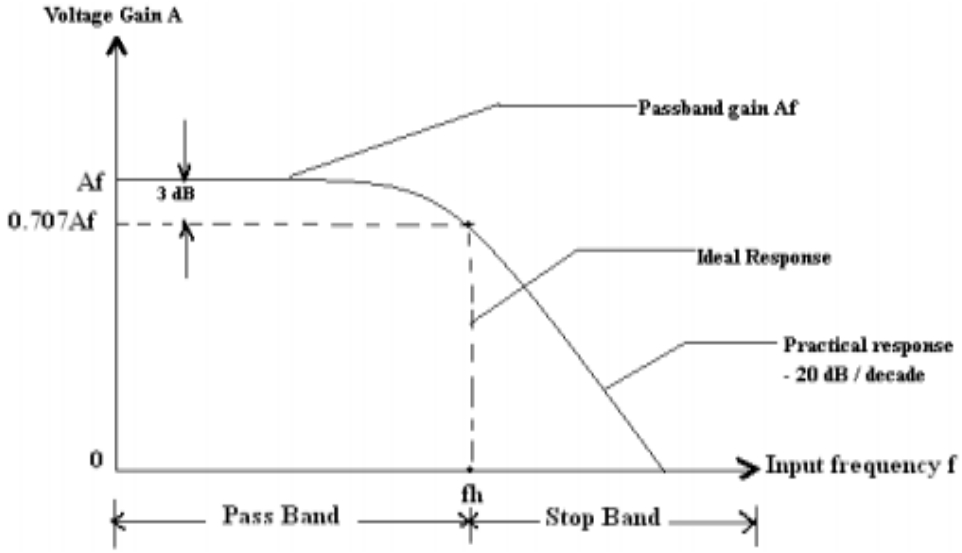
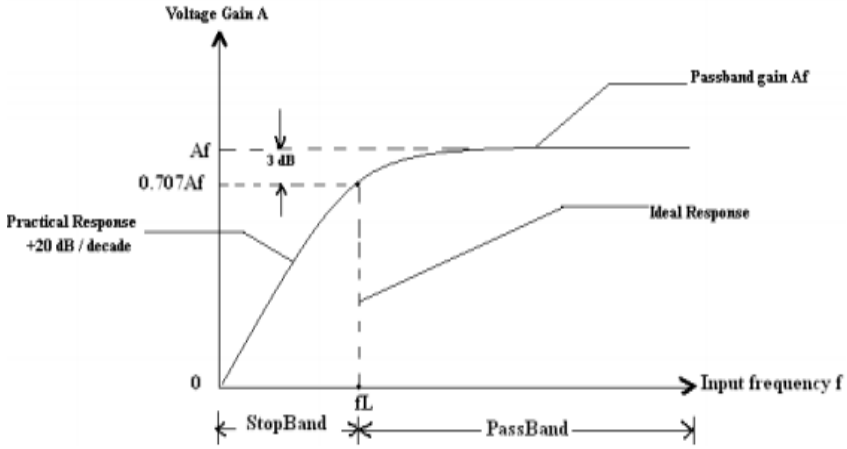


Fig 4: Frequency response characteristics of HPF



Precautions:

- Check the connections before giving the power supply.
- Readings should be taken carefully.
- V_{CC} and V_{EE} must be given to the corresponding pins.

Result:

9. Design of State Variable Filter using Op-amps

Aim: To design a State Variable Filter which has a corner frequency, f_c of 1 KHz and a quality factor(Q) of 10. Assume both the frequency determining resistors and capacitors are equal. Determine the filters DC gain and draw the frequency response of LPF, HPF and BPF.

Apparatus Required:

S. No	Equipment/ Component name	Specifications/ Value	Quantity
1	IC - μA741	Refer Appendix B	3
2	Resistors	1kΩ 19kΩ	1 1
3	Resistors	10kΩ 16KΩ	2 2
4	Capacitors	1nF	2
5	Bread Board		1
6	Dual Channel CRO	(0 – 20MHz)	1
7	RPS	(0 – 30V),1A	1
8	Function Generator	(1Hz – 1MHz)	1

Theory:

The **state variable filter** is a type of multiple-feedback filter circuit that can produce all three filter responses, *Low Pass*, *High Pass* and *Band Pass* simultaneously from the same single active filter design. One of the main advantages of a state variable filter design is that all three of the filters main parameters, Gain (A), corner frequency, f_C and the filters Q can be adjusted or set independently without affecting the filters performance.

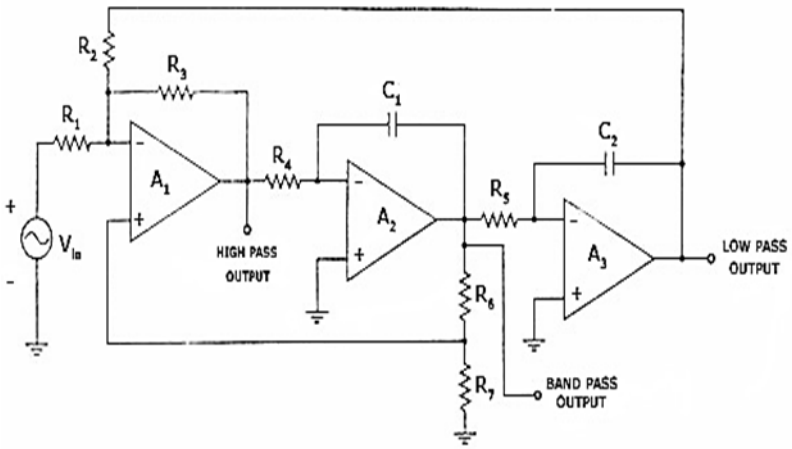
In fact if designed correctly, the -3dB corner frequency, (f_c) point for both the low pass amplitude response and the high pass amplitude response should be identical to the center frequency point of the band pass stage. That is $f_{LP(-3dB)}$ equals $f_{HP(-3dB)}$ which equals $f_{BP(center)}$. Also the damping factor, (ζ) for the band pass filter response should be equal to 1/Q as Q will be set at -3dB, (0.7071). Although the filter provides low pass (LP), high pass (HP) and band pass (BP) outputs the main application of this type of filter circuit is as a state variable band pass filter design with the center frequency set by the two RC integrators.

While we have seen before that a band pass filters characteristics can be obtained by simply cascading together a low pass filter with a high pass filter, state variable band pass filters have the advantage that they can be tuned to be highly selective (high Q) offering high gains at the center frequency point.

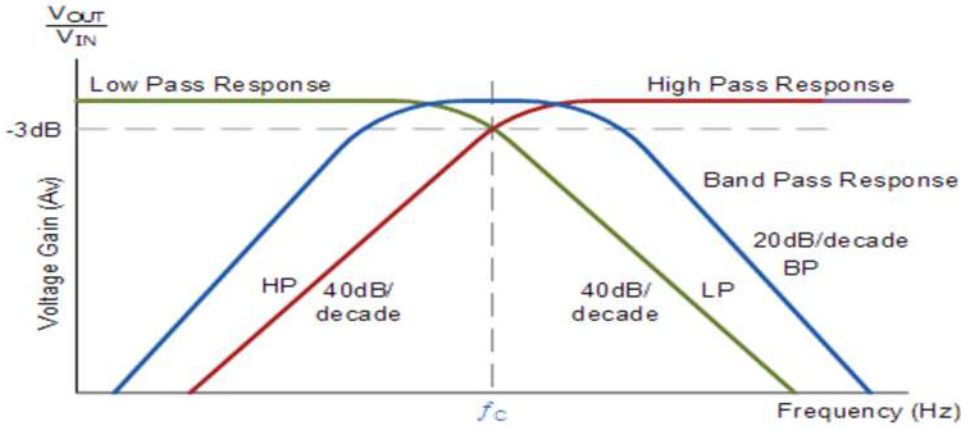
There are several state variable filter designs available all based on the standard filter design with both inverting and non-inverting variations available. However, the basic filter design will be the same for both variations as shown in the following block diagram representation.

Circuit Diagram:

The basic non-inverting state variable filter design is therefore given as:



Model Waveforms:



Design Calculations:

If both the resistor, R and the feedback capacitor, C of the two integrator circuits are the same values, that is R = R and C = C, the cut-off or corner frequency point for the filter is given simply as:

Filter's Corner Frequency

$$fc = \frac{1}{2\pi RC}\ Hz$$

We can choose a value for either the resistor, or the capacitor to find the value of the other. If we assume a suitable value of 10nF for the capacitor then the value of the resistor will be:

$$R = \frac{1}{2\pi f_C C} = \frac{1}{2\pi \times 1000 \times 10nF} = 15.9k\Omega$$

Giving C = 10nF and R = 15.9kΩ, or 16kΩ to the nearest preferred value.

The value of Q is given as **10**. This relates to the filters damping coefficient as:

$$Q = 10 = \frac{1}{2\zeta} \qquad \therefore\ 2\zeta = \frac{1}{10} = 0.1$$

In the state variable transfer function above, the 2ζ part is replaced by the resistor combination giving:

$$2\zeta = \frac{1}{Q} = \frac{1}{10} = \frac{R_1(R_3+R_4)}{R_4(R_1+R_2)}\sqrt{\frac{R_3}{R_4}\times\frac{RC}{RC}} = 0.1$$

We know from above that R = 16kΩ's and C = 10nF, but if we assume that the two feedback resistors, R3 and R4 are the same and equal to 10kΩ's, then the above equation reduces down to:

$$0.1 = \frac{R_1(R_3+R_4)}{R_4(R_1+R_2)} = \frac{R_1(10k\Omega+10k\Omega)}{10k\Omega(R_1+R_2)}$$

Assuming a suitable value for the input resistor, R1 of say 1kΩ's, then we can find the value of R2 as follows:

$$\therefore R_2 = \frac{R_1(R_3+R_4)}{0.1\times R_4} - R_1$$

$$= \frac{1k\Omega(10k\Omega+10k\Omega)}{0.1\times 10k\Omega} - 1k\Omega = 19k\Omega$$

From the normalized transfer function above, the DC passband gain is defined as A_o and from the equivalent state variable filter transfer function this equates to:

The SVF Filters DC Pass band Gain

$$A_O = \frac{R_2(R_3+R_4)}{R_3(R_1+R_2)} = \frac{19k\Omega(10k\Omega+10k\Omega)}{10k\Omega(1k\Omega+19k\Omega)}$$

$$\therefore A_O = 1.9 = 5.57dB$$

Therefore the DC voltage gain of the filter is calculated at 1.9, which basically equates to R2/R3. Also the maximum gain of the filter at f_C can be calculated as: A_o x Q as follows.

The SVF Filters Maximum Gain

$$A_{(f_c)} = \frac{V_{OUT}}{V_{IN}} = \frac{A_O}{2\zeta} = A_O \times Q$$

$$\therefore A_O \times Q = 1.9 \times 10 = 19 = 25.6dB$$

State Variable Filter Circuit

Then the design of the state variable filter circuit will be: R = 16kΩ, C = 10nF, R_1 = 1kΩ, R_2 = 19kΩ and R_3 = R_4 = 10kΩ

Procedure:

1. Connections are made as per the circuit diagram.
2. Apply sinusoidal wave of constant amplitude as the input such that op-amp does not go into saturation.
3. Vary the input frequency and note down the output amplitude at output pin of op-amps-A_1, A_2, A_3.
4. Calculate gain in dB for HPF, BPF, LPF as shown in tables.
5. Plot the frequency response as shown in model waveform.

Sample Readings:

1. HPF: **V_{in} = 2V_{pp}**

S.No	Frequency (Hz)	O/P Voltage (V_o)	Gain dB = 20log(Vo/Vin)

2. BPF: **V_{in} = 2V_{pp}**

S.No	Frequency (Hz)	O/P Voltage (V_o)	Gain dB = 20log(Vo/Vin)

3. LPF: **V_{in} = 2V_{pp}**

S.No	Frequency (Hz)	O/P Voltage (V_o)	Gain dB = 20log(Vo/Vin)

Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Result:

10. APPLICATIONS OF 555 TIMERS

Aim: To design and study the following circuits using 555 timers.

1. MONOSTABLE MULTIVIBRATOR
2. ASTABLE MULTIVIBRATOR
3. SCHMITT TRIGGER

Apparatus required:

S.No	Equipment/ Component name	Specifications/ Value	Quantity
1	IC –SE/NE555	Refer Appendix B	1
2	Resistors	7.2kΩ 3.6Ω 10k Ω 100KΩ	1 1 1 2
3	Capacitor	0.01μF 0.1μF	1 1
4	Diode - OA79		1
5	Dual Channel CRO	(0 – 20MHz)	1
6	Bread Board		1
7	RPS	(0 – 30V),1A	1
8	Function Generator	(1Hz – 1MHz)	1

Theory:

A. Mon stable operation:

A Monostable Multivibrator, often called a one-shot Multivibrator, is a Pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby mode the output of the circuit is approximately Zero or at logic-low level. When an external trigger pulse is obtained, the output is forced to go high (V_{CC}). The time the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The Monostable circuit has only one stable state (output low), hence the name monostable. Normally the output of the Monostable Multivibrator is low. When the power supply V_{CC} is connected, the external timing capacitor 'C" charges towards V_{CC} with a time constant (R_A+R_B) C. During this time,

pin 3 is high (≈V_{CC}) as Reset R=0, Set S=1 and this combination makes $\bar{Q}$ =0 which has unclamped the timing capacitor 'C'. For pin configuration and specifications, see Appendix-C.

B. **Astable operation:**

When the capacitor voltage equals 2/3 V_{CC}, the UC triggers the control flip flop on that $\bar{Q}$ =1. It makes Q_1 ON and capacitor 'C' starts discharging towards ground through R_B and transistor Q_1 with a time constant R_BC. Current also flows into Q_1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1 .The minimum value of R_A is approximately equal to $V_{CC}/0.2$ where 0.2A is the maximum current through the ON transistor Q_1 .

During the discharge of the timing capacitor C, as it reaches $V_{CC}/3$, the LC is triggered and at this stage S=1, R=0 which turns $\bar{Q}$ =0. Now $\bar{Q}$ =0 unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between 2/3 V_{CC} and 1/3 V_{CC} respectively. The length of time that the output remains HIGH is the time for the capacitor to charge from 1/3 V_{CC} to 2/3 V_{CC}.

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{CC} volts is given by $V_C = V_{CC} (1 - e^{-t/RC})$

Total time period $T = 0.69 (R_A + 2 R_B) C$

$f = 1/T = 1.44/ (R_A + 2R_B) C$

C. **Schmitt Trigger:**

In the Bistable mode or Schmitt trigger the 555 can operate as a flip-flop, if the DIS pin is not connected and no capacitor is used. Uses include bounce free latched switches. The trigger and reset inputs (pins 2 and 4 respectively on a 555) are held high via Pull-up resistors while the threshold input (pin 6) is simply grounded. Thus configured, pulling the trigger momentarily to ground acts as a 'set' and transitions the output pin (pin 3) to Vcc (high state). Pulling the reset input to ground acts as a 'reset' and transitions the output pin to ground (low state). No capacitors are required in a bistable configuration. Pins 5 and 7 (control and discharge) are left floating. "Bistable" signifies two stable states—high and low. In the bistable mode, the 555 acts like a Schmitt trigger.A Schmitt trigger produces an output when the input exceeds a specified level. The output continues until the input falls below a specified level. With the 555, a trigger at one input sets the output to high; a trigger at another input sets the output to low. The output retains its value until the input changes sufficiently to trigger a state change.

Circuit Diagrams:

Fig 1: Monostable operation:

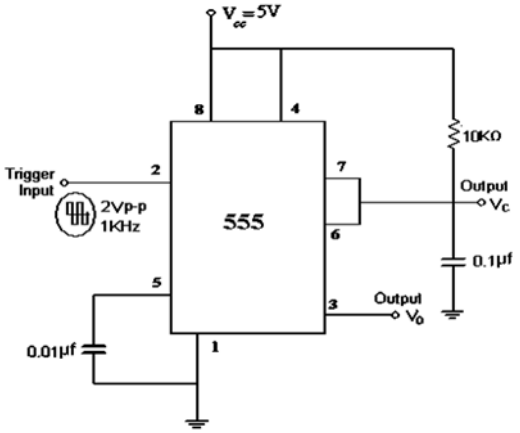


Fig 2: Astable operation:

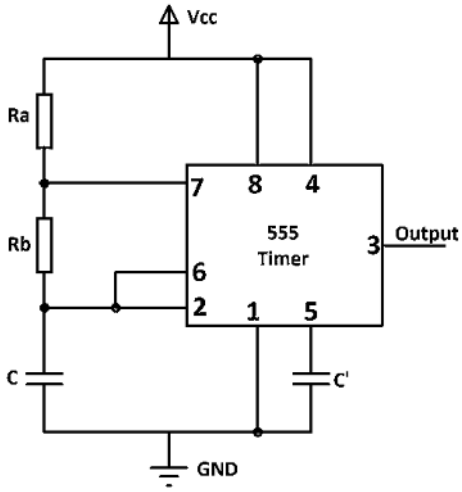
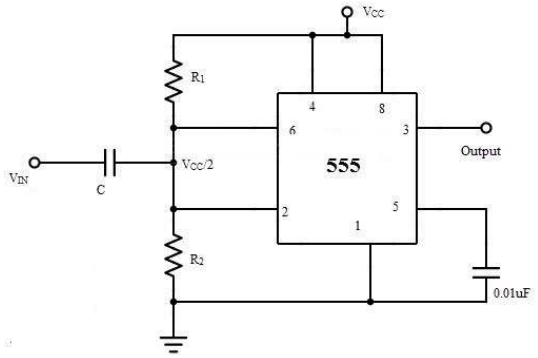


Fig 3: Schmitt Trigger :



Design:

(a)Monostable operation:

Consider V_{CC} = 5V, for given t_p

Output pulse width $t_p = 1.1\ R_A\ C$

Assume C in the order of μF & then find R_A

(b)Astable operation:

Formulae: $f = 1/T = 1.44/ (R_A+2R_B)\ C$

Duty cycle, $D = t_c /T = (R_A + R_B)/(R_A+2R_B)$

Model calculations:

(a)Monostable operation:

If C = 0.1 μF , R_A = 10k then t_p = 1.1 mSec

Trigger Voltage = 4 V

(b)Astable operation:

Given f =1 KHz and C = 0.1μF, D=0.25

1 KHz = $1.44/ (R_A+2R_B)$ x $0.1x10^{-6}$ and $0.25 = (R_A+R_B)/(R_A+2R_B)$

Solving both the above equations, we obtain R_A & R_B , then

R_A = 7.2KΩ & R_B = 3.6KΩ

Procedure:

1. Monostable operation:

1. Connect the circuit as shown in the circuit diagram as shown in Fig1.
2. Apply Negative triggering pulses at pin 2 of frequency 1 KHz.
3. Observe the output waveform and capacitor voltage as shown in Fig 3 (b)and (c) and measure the pulse duration
4. Theoretically calculate the pulse duration as $T_{high}=1.1.\ R_aC$
5. Compare it with experimental values.

2. Astable operation:

a) Unsymmetrical Square wave

1. Connect the circuit as per the circuit diagram shown in Fig 2 without connecting the diode OA 79.
2. Observe and note down the output waveform at pin 3 and across timing capacitor as shown in Fig 4(a) and (b).
3. Measure the frequency of oscillations and duty cycle and then compare with the given values.
4. Sketch both the waveforms to the same time scale.

b) Symmetrical square waveform generator:

1. Connect the diode OA79 as shown in fig (ii) to get D=0.5 or 50%.
2. Choose $R_a=R_b$ = 10K and C=0.1μF
3. Observe the o/p waveform as shown in Fig 4(c), measure frequency of oscillations and the duty cycle and then sketch the o/p waveform.

3. Schmitt Trigger:

1. Construct the circuit as shown in the figure.
2. Observe the output waveform of schmitt trigger circuit by giving sine wave as input.
3. Note down the amplitude and time period and draw the output waveform.

Model Waveforms:

(a)Monostable operation:

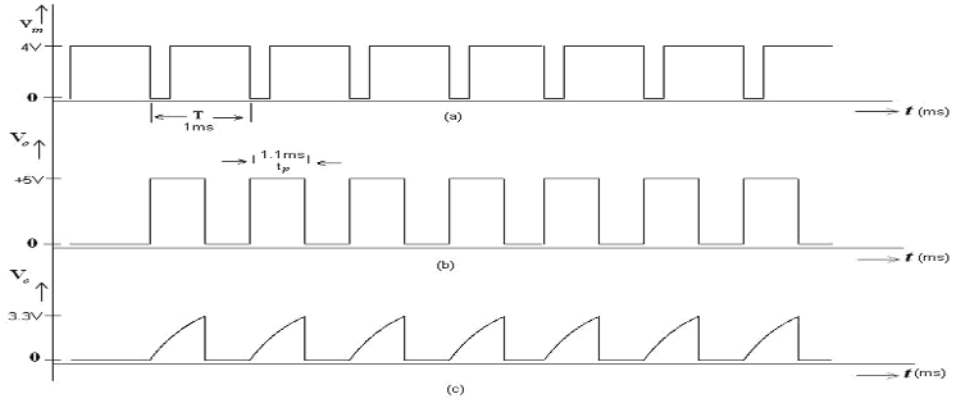


Fig (a): Trigger signal (b): Output Voltage (c): Capacitor Voltage

(b)Astable operation:

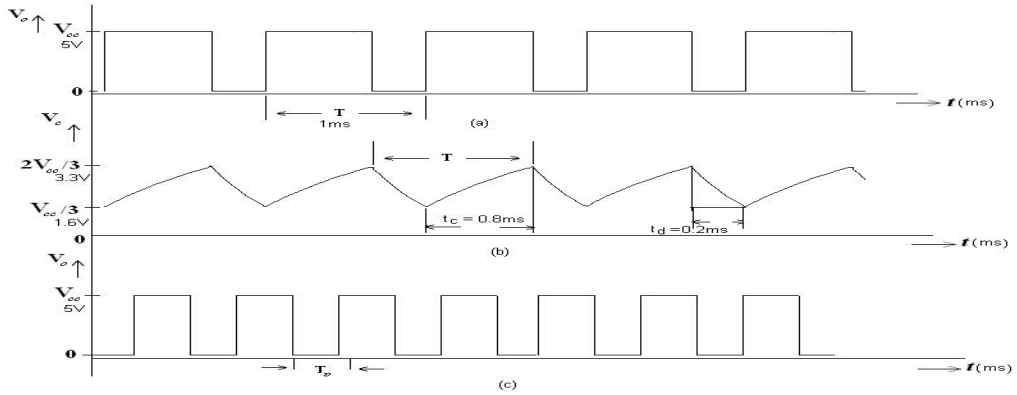
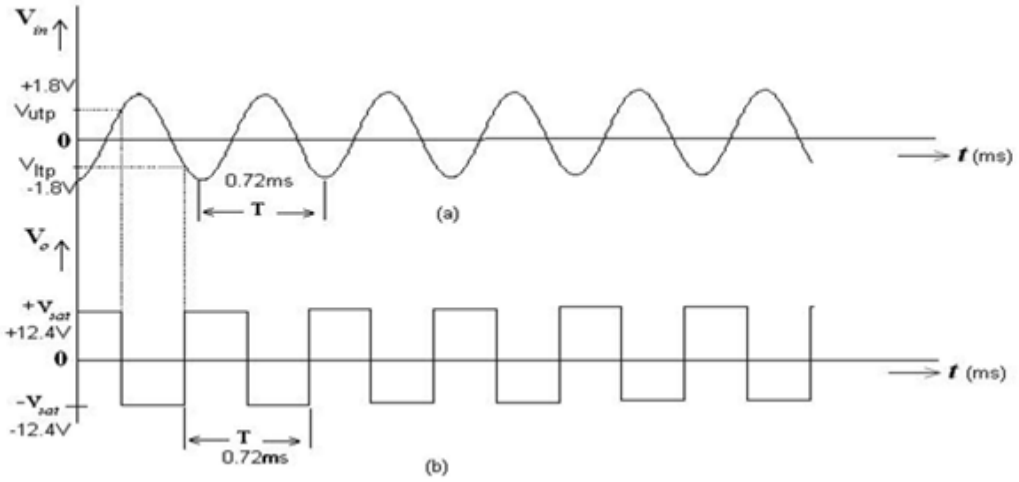


Fig (a): Unsymmetrical square wave output (b): Capacitor voltage of Unsymmetrical square wave output (c): Symmetrical square wave output

(c). Scmitt Trigger I/P and O/P waveforms:



Sample Readings:

(a) Monostable operation:

Trigger	Voltage(V_{PP})	Capacitor output

(b) Astable operation:

Voltage (V_{PP})	Unsymmetrical	Symmetrical
Time Period		
Duty cycle		

(c) Schmitt Trigger:

INPUT		OUTPUT		
Amplitude	Time period	Amplitude	Time period	
			ON time	OFF time

Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Result:

11. PLL using 565

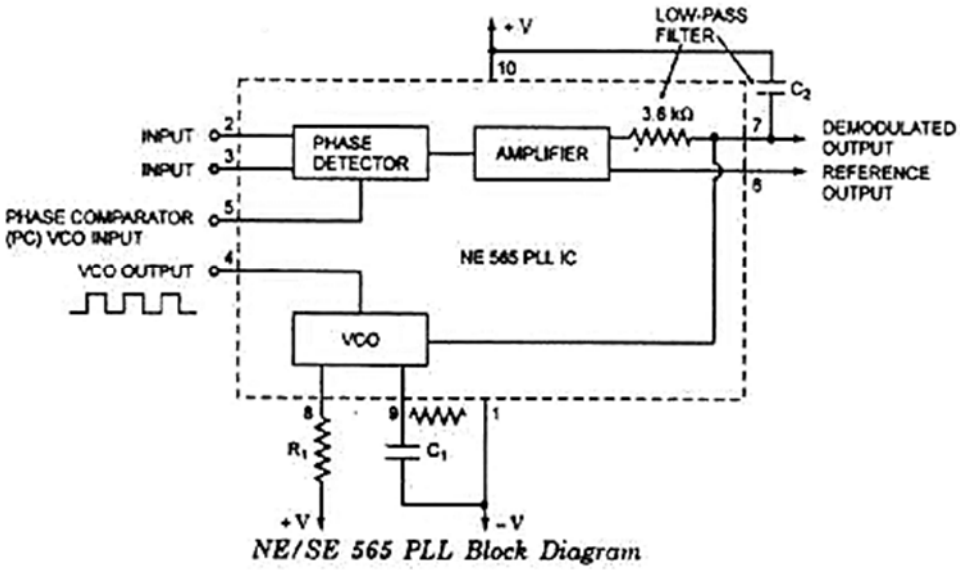
Aim: To study the operation of PLL using NE/SE 565.

Apparatus:

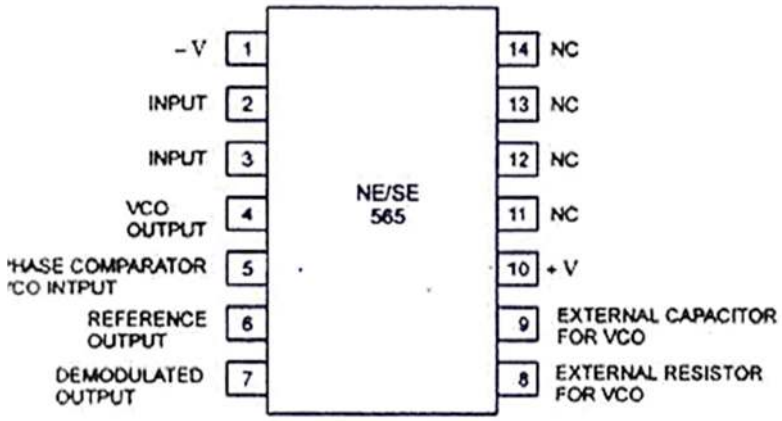
S.No	Equipment/ Component name	Specifications/ Value	Quantity
1	IC –SE/NE565	Refer Appendix B	1
2	Capacitor	0.01μF 1μF	1 1
3	Bread Board		1
4	Dual Channel CRO	(0 – 20MHz)	1
5	Resistor	6.8kΩ	1
6	RPS	(0 – 30V),1A	1
7	Function Generator	(1Hz – 1MHz)	1

CIRCUIT DIAGRAM:

Fig(1)



NE/SE 565 PLL Block Diagram



14-Pin DIP Package

Procedure:

1. Make connections of the PLL as shown in fig.1
2. Measure the free running frequency of" VCO at pin 4 with the i/p signal V_{in}, set equal to zero. Compare it with the calculated value = $0.25/R_TC_T$
3. Now apply the i/p signal of 1 V_{PP}, square wave at a 1 KHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the CRO.
4. Gradually increase the i/p frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower end of the capture range. Go on increasing the i/p frequency, till PLL tracks the i/p signal, say to a frequency "f_2". This frequency "f_2" gives the upper end of the lock range. If i/p frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the i/p frequency till the PLL is again locked. This is the frequency (f_3) the upper end of the capture range. Keep on decreasing the i/p frequency until the loop is Unlocked. This frequency 'f_4' gives lower end of lock range.
6. The lock range $\Delta f_L = f_2 - f_4$. Compare it with the calculated value of $(\pm 7.8 f_o)/12$ also the capture range is $\Delta f_c = (f_3 - f_1)$. Compare it with the calculated value of capture-range.

Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Result:

12. Design of Fixed Voltage Regulators

Aim: To obtain the regulation characteristics of three terminal voltage regulators.

Apparatus:

S.No.	Components name & Specification	Quantity
1	Bread board	1
2	IC 7805 (Refer Appendix F)	1
3	IC 7912 (Refer Appendix F)	1
4	Digital Multimeter (3 ½ digit display)	1
5	Milli Ammeter (0-150mA)	1
6	Regulated Power Supply (0-30V)	1
7	Connecting Wires	
8	Resistors-100Ω,1KΩ	Each one

Theory:

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load current and input voltage. IC voltage regulators are versatile, relatively inexpensive and are available with features such as programmable output, current/voltage boosting, internal short circuit current limiting, thermal shunt down and floating operation for high voltage applications.

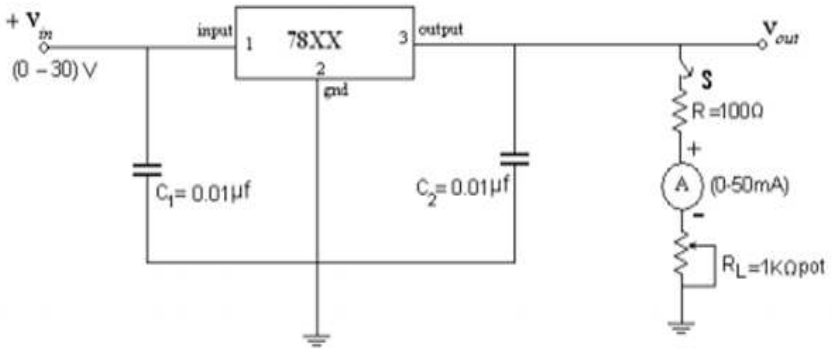
The 78XX series consists of three-terminal positive voltage regulators with seven voltage options. These IC's are designed as fixed voltage regulators and with adequate heat sinking can deliver output currents in excess of 1A.

The 79XX series of fixed output voltage regulators are complements to the 78XX series devices. These negative regulators are available in same seven voltage options.

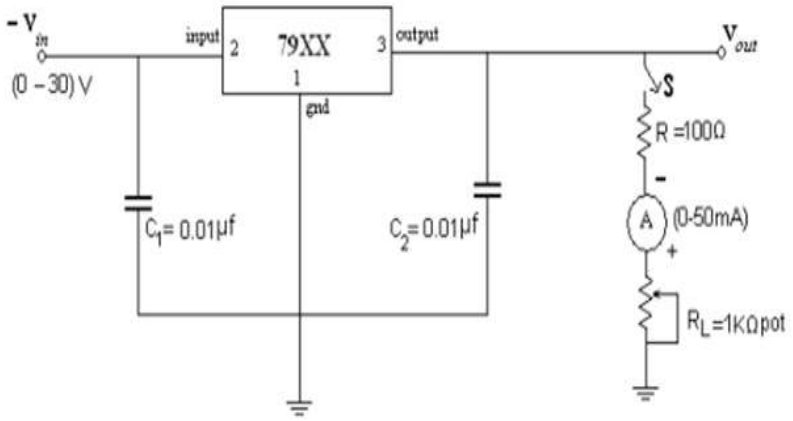
Typical performance parameters for voltage regulators are line regulation, load regulation, temperature stability and ripple rejection.

Circuit Diagrams:

1. Positive Voltage Regulator : Fig (1)



2. Negative Voltage Regulator : Fig. (2)



Procedure:

Line Regulation:

1. Connect the circuit as shown in Fig.1 by keeping S open for 7805.
2. Vary the dc input voltage from 0 to 10V in suitable stages and note down. The output voltage in each case as shown in Table1 and plot the graph between input voltage and output voltage.
3. Repeat the above steps for negative voltage regulator as shown in Fig.2 for 7912 for an input of 0V to -15V.
4. Note down the dropout voltage whose typical value = 2V and line regulation typical value = 4mV for V_{in} = 7V to 25V

Load Regulation:

1. Connect the circuit as shown in the Fig. 1 by keeping S closed for load Regulation.
2. Now vary R1 and measure current I_L and note down the output

voltage V_o in each case as shown in Table 2 and plot the graph between current I_L and V_0

3. Repeat the above steps as shown in Fig 2 by keeping switch S closed for Negative voltage regulator 7912.

Out put Resistance (R_0) = (V_{NL} - V_{FL})/ I_{FL} Ω

V_{NL} =No load voltage

V_{FL} = Full load voltage

I_{FL} = Full load current

Observations :

1. IC 7805

Line Regulation

Input Voltage V_i(V)	Output Voltage V_o(V)

Load Regulation

Load Current I_L(mA)	Output Voltage V_o(V)

2. IC 7912

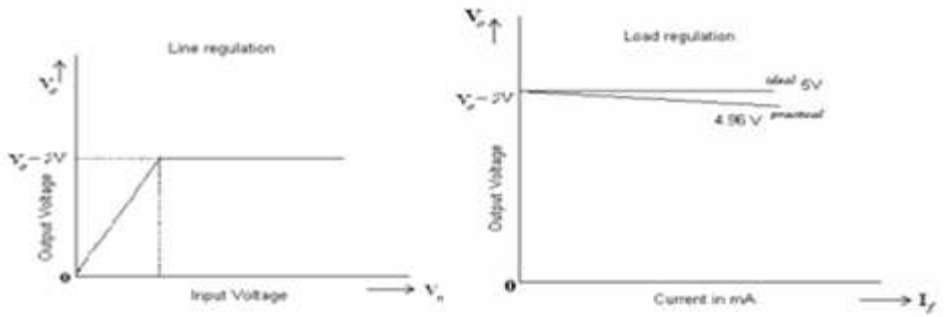
Line Regulation

Input Voltage V_i(V)	Output Voltage V_o(V)

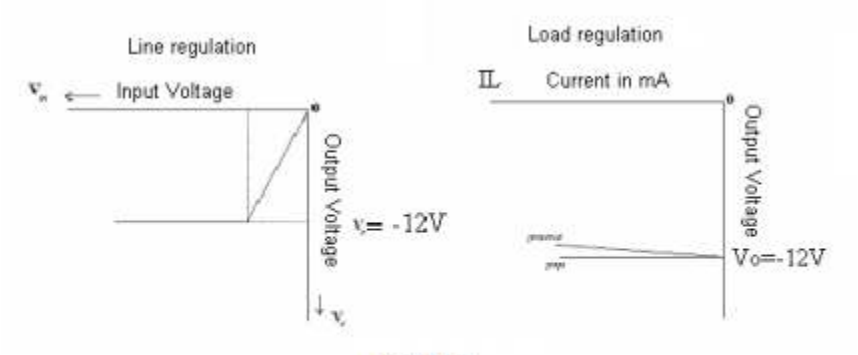
Load Regulation

Load Current I_L(mA)	Output Voltage V_o(V)

Model Graphs :



IC 7805



IC 7912

Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Result:

13. Design of Variable Voltage Regulator using IC723

Aim: To design a low voltage variable regulator of 2 to 7V using IC 723.

Apparatus required:

S. No.	Equipment/ Component name	Specifications/ Value	Quantity
1	IC 723	Refer appendix D	1
2	Variable Resistors	1KΩ, 5.6KΩ	Each one
3	Resistors	3.3kΩ , 4.7kΩ , 100Ω	Each one
4	RPS	30V , 1A	1
5	Digital Multimeter		1

Theory:

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load current and input voltage variations. Using IC 723, we can design both low voltage and high voltage regulators with adjustable voltages.

For a low voltage regulator, the output V_O can be varied in the range of voltages $V_o < V_{ref}$, whereas for high voltage regulator, it is $V_O > V_{ref}$. The voltage V_{ref} is generally about 7.5V. Although voltage regulators can be designed using Op-amps, it is quicker and easier to use IC voltage Regulators.

IC 723 is a general purpose regulator and is a 14-pin IC with internal short circuit current limiting, thermal shutdown, current/voltage boosting etc. Furthermore it is an adjustable voltage regulator which can be varied over both positive and negative voltage ranges. By simply varying the connections made externally, we can operate the IC in the required mode of operation. Typical performance parameters are line and load regulations which determine the precise characteristics of a regulator. The pin configuration and specifications are shown in the Appendix-A.

Design of Low voltage Regulator:

$$V_o = V_{ref} R_2 / (R_1+R_2) \quad , \quad V_{ref} = 7.15v$$

Procedure:

a) Line Regulation*:*

1. Connect the circuit as shown in fig 1.
2. Obtain R_1 and R_2 for V_o= 5V

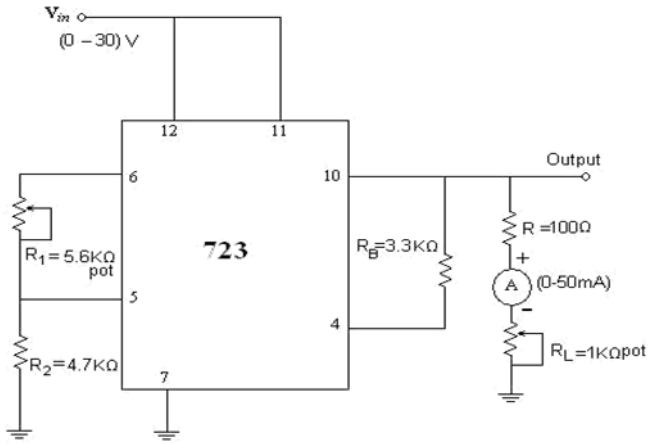
3. By varying V_{in} from 2 to 10V, measure the output voltage V_o.
4. Draw the graph between V_{in} and V_o as shown in model graph (a)
5. Repeat the above steps for V_o= 3V

b) Load Regulation*:* For V_o=5V

1. Set V_i such that V_O= 5 V
2. By varying R_L, measure I_L and V_o
3. Plot the graph between I_L and V_o as shown in model graph (b)
4. Repeat above steps 1 to 3 for V_O=3V.

Circuit Diagram:

Fig1: Voltage Regulator



Sample Readings:

a) LineRegulation:

Vo set to 5V

Vi(V)	Vo(V)

Vo set to 3V

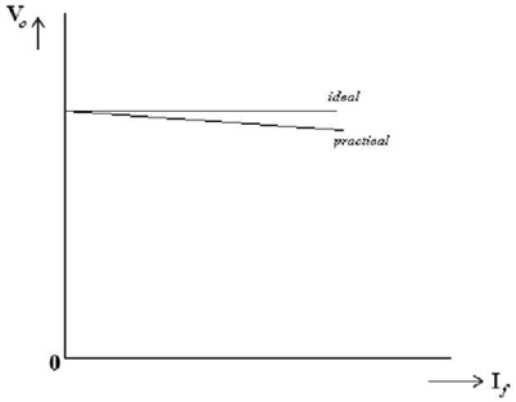
Vi(V)	Vo(V)

b) Load Regulation:

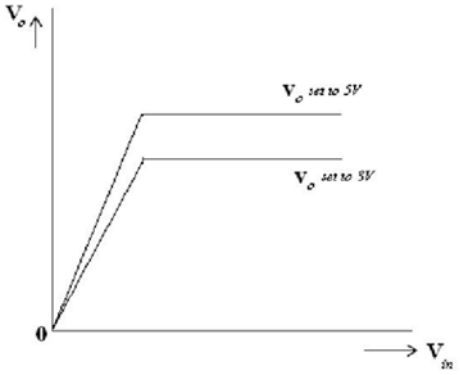
Vo set to 5V

I_L (mA)	Vo(V)

Model Waveforms:



Load Regulation



Line Regulation

Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Result:

14. DESIGN OF VCO USING IC 566

Aim: i) To observe the applications of VCO-IC 566
ii) To generate the frequency modulated wave by using IC 566

Apparatus required:

S.No	Equipment/ Component Name	Specifications/ Value	Quantity
1	IC	SE/NE 566	1
2	Resistors	10KΩ 1.5KΩ	2 1
3	Capacitors	0.1 μF 100 pF	1 1
4	RPS	0-30 V, 1 A	1
5	Dual Channel CRO	0-20 MHz	1
6	Function Generator	10 Hz -1 MHz	1

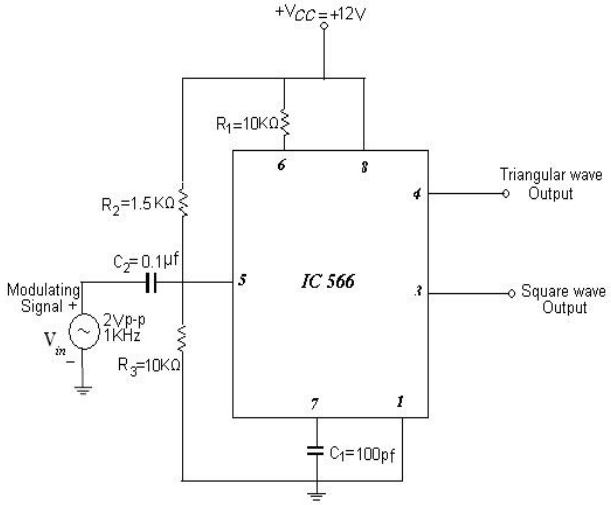
Theory:

The VCO is a free running Multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a d.c control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "voltage controlled oscillator" or, in short, VCO.
The output frequency of the VCO can be changed either by R_1, C_1 or the voltage V_C at the modulating input terminal (pin 5). The voltage V_C can be varied by connecting a R_1R_2 circuit. The components R_1 and C_1 are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{CC} which can produce a frequency variation of about 10 to 1.

Design:

1. Maximum deviation time period = T.
2. $f_{min} = 1/T$.
   Where f_{min} can be obtained from the FM wave
3. Maximum deviation, $\Delta f = f_o - f_{min}$
4. Modulation index $\beta = (\Delta f / f_m)$
5. Band width $BW = 2(\beta+1) f_m = 2 (\Delta f + f_m)$
6. Free running frequency, $f_o = 2(V_{CC} - V_c) / (R_1C_1V_{CC})$

Circuit Diagram:



Procedure:

1. The circuit is connected as per the circuit diagram shown in Fig1.
2. Observe the modulating signal on CRO and measure the amplitude and frequency of the signal.
3. Without giving modulating signal, take output at pin 4, we get the carrier wave.
4. Measure the maximum frequency deviation of each step and evaluate the modulating Index , $m_f = \beta = \Delta f / f_m$

Waveforms:

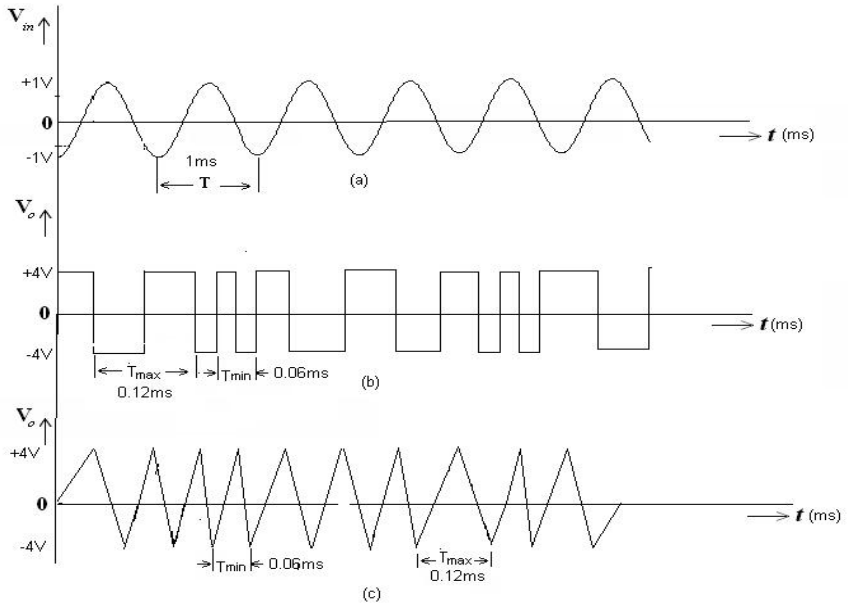


Fig (a): Input wave of VCO (b): Output of VCO at pin3 (c): Output of VCO at pin4

Sample readings:

V_{CC} = 12V; R_1= R_3 =10KΩ ; R_2=1.5KΩ; f_m=1KHz

Free running frequency, f_o = 26.1KHz

f_{min} = 8.33KHz

Δf= 17.77 KHz

β= $\Delta f/f_m$ = 17.77

Band width BW ≈ 36 KHz

Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Result:

15. Design of 4 bit DAC using OP AMP

Aim: To design a 4 bit DAC using IC 741 with R-2R ladder network.

Apparatus required:

S.No.	Equipment/ Component name	Specifications/ Value	Quantity
1	IC - μA741		1
2	Digital Multimeter		1
3	Digital Trainer Board		1
4	Resistors	1KΩ 2KΩ	4 5

Theory:

Digital systems are used in ever more applications, because of their increasingly efficient, reliable, and economical operation with the development of the microprocessor, data processing has become an integral part of various systems Data processing involves transfer of data to and from the microcomputer via input/output devices. Since digital systems such as microcomputers use a binary system of ones and zeros, the data to be put into the microcomputer must be converted from analog to digital form. On the other hand, a digital-to-analog converter is used when a binary output from a digital system must be converted to some equivalent analog voltage or current. The function of DAC is exactly opposite to that of an ADC.

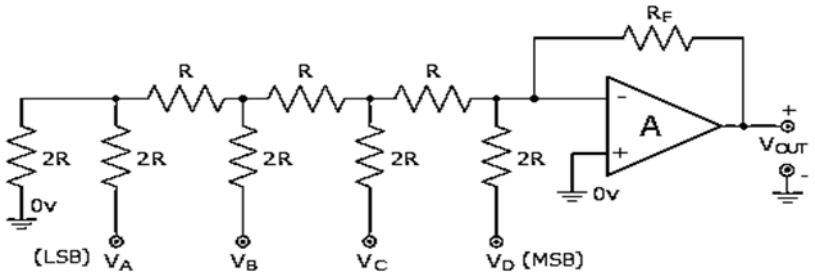
A DAC in its simplest form uses an op-amp and either binary weighted resistors or R-2R ladder resistors. In binary-weighted resistor op-amp is connected in the inverting mode, it can also be connected in the non-inverting mode. Since the number of inputs used is four, the converter is called a 4-bit binary digital converter. The analog output voltage is given by

$$V_o = -V_{ref}\, R_f \left(\frac{D}{2R} + \frac{C}{4R} + \frac{B}{8R} + \frac{A}{16R}\right)$$

$$V_{ref} = 5V, \quad R_f = R = 1K\Omega$$

So,
$$V_o = -5\left(\frac{D}{2} + \frac{C}{4} + \frac{B}{8} + \frac{A}{16}\right)$$

Circuit Diagram:



Procedure:

1. Connect the circuit as shown in Fig 1.
2. Vary the Digital inputs A, B, C, D from the digital trainer board and note down the output at pin 6 using Multimeter.
3. For logic '1', 5 V is applied and for logic '0', 0V is applied.

Observations:

S.No	D (MSB)	C	B	A (LSB)	Theoretical Voltage(V)	Practical Voltage(V)
1	0	0	0	0	0.0000	
2	0	0	0	1	-0.3125	
3	0	0	1	0	-0.6250	
4	0	0	1	1	-0.9375	
5	0	1	0	0	-1.2500	
6	0	1	0	1	-1.5625	
7	0	1	1	0	-1.8750	
8	0	1	1	1	-2.1875	
9	1	0	0	0	-2.5000	
10	1	0	0	1	-2.8125	
11	1	0	1	0	-3.1250	
12	1	0	1	1	-3.4375	
13	1	1	0	0	-3.7500	
14	1	1	0	1	-4.0625	
15	1	1	1	0	-4.3750	
16	1	1	1	1	-4.6875	

Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

RESULT:

APPENDIX – A

IN4007

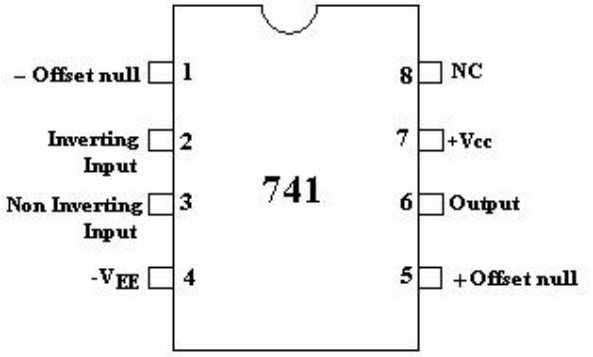
Diode:

Type No	IN4007
Max. Peak Inverse Volts	50
Max RMS Supply Volts	35
Maximum Forward Voltage	1.1 Volts, Peak
@ 1Ampere, DC @ 75^0 C	
Maximum Reverse DC Current	10μA
@PIV @ 25^0 C	
Maximum Dynamic Reverse Current	30μA, Average
@PIV @75^0 C	

APPENDIX – B

IC μA741

Pin Configuration:



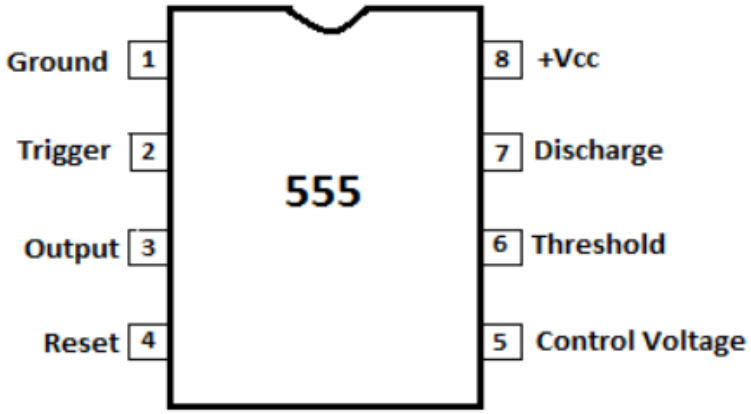
Specifications:

1. Voltage gain A = typically 2,00,000
2. I/P resistance R_L = practically 2M
3. O/P resistance R_1 = 0, practically 75Ω
4. Bandwidth = Hz. It can be operated at any frequency
5. Common mode rejection ratio = α (Ability of op amp to reject noise voltage)
6. Slew rate (SR) in V/μsec = (Rate of change of O/P voltage)
7. When $V_1 = V_2$, V_0 = 0V
8. Input offset voltage (V_{io})= max 6 mv (Rs≤ 10K)
9. Input offset current (I_{io}) = max 200nA
10. Input bias current(I_B) : 500nA
11. Input capacitance : type value 1.4PF
12. Offset voltage adjustment range : ± 15mV
13. Input voltage range : ± 13V
14. Supply voltage rejection ratio(SVRR or PSRR) : 150 μV/V
15. Output voltage swing: + 13V and – 13V for R_L> 2K
16. Output short-circuit current (I_{sc}) : 25mA
17. supply current: 28mA
18. Power consumption: 85MW
19. Transient response: rise time= 0.3 μs
20. Overshoot= 5%

APPENDIX – C

IC 555

Pin Configuration:



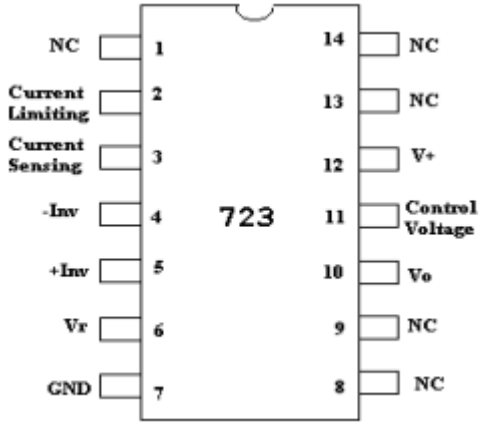
Specifications:

Operating temperature	:	SE 555 -55°C to 125°C
	:	NE 555 0° to 70°C
Supply voltage	:	+5V to +18V
Timing	:	µSec to Hours
Sink current	:	200mA
Temperature stability	:	50 PPM/°C change in temp or 0-005% /°C.

APPENDIX – D

IC723

Pin Configuration:

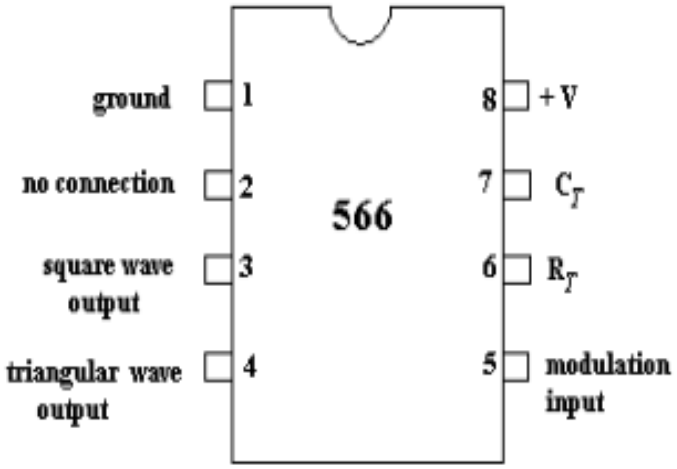


Specifications of 723:

Power dissipation	:	1W
Input Voltage	:	9.5 to 40V
Output Voltage	:	2 to 37V
Output Current	:	150mA for Vin-Vo = 3V
		10mA for Vin-Vo = 38V
Load regulation	:	0.6% Vo
Line regulation	:	0.5% Vo

APPENDIX – E
IC566

Pin Configuration:

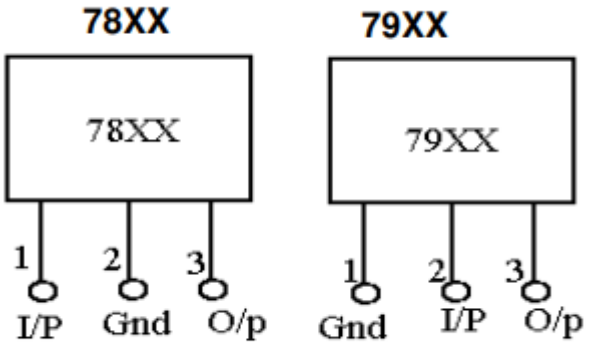


Specifications of 723

Maximum operating Voltage	---	26V
Input voltage	---	3V (P-P)
Storage Temperature	---	-65°C to + 150°C
Operating temperature	---	0°C to +70°C for NE 566
		-55°C to +125°C for SE 566
Power dissipation	---	300mv

APPENDIX – F

Pin Configuration:



Plastic package

Typical Parameters at 25^{0}C:

Parameter	LM 7805	LM 7809	LM 7912
Vout,V	5	9	-12
Imax,A	1.5	1.5	1.5
Load Reg,mV	10	12	12
Line Reg,mV	3	6	4
Ripple Rej,dB	80	72	72
Dropout	2	2	2
Rout,mΩ	8	16	18
I_{SL},A	2.1	0.45	1.5

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